
Imperial College HiPEDS Research Centre presents:
NANDA Workshop
Novel Architecture and Novel Design Automation
5-6 September, 2022
Imperial College London
http://cc.doc.ic.ac.uk/nanda

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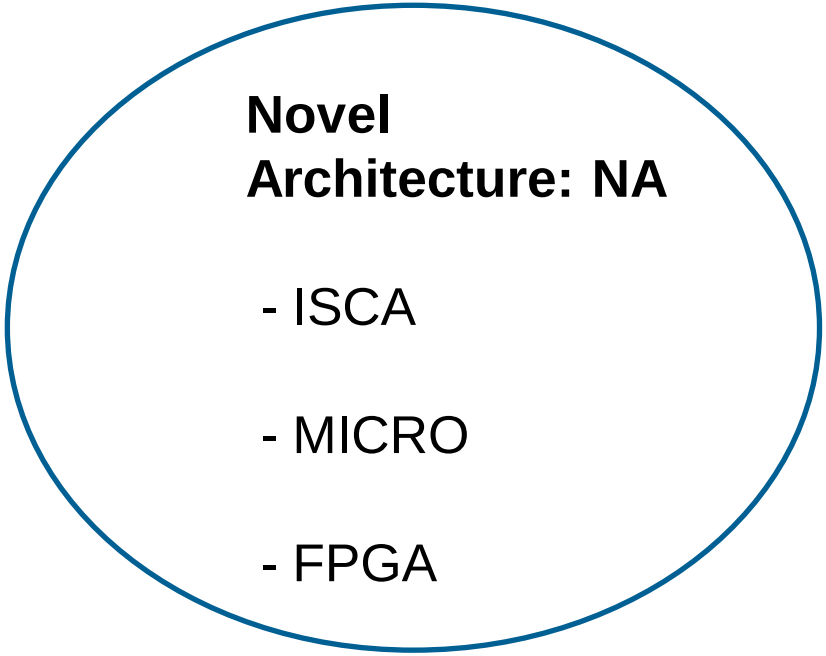
Why NANDA?



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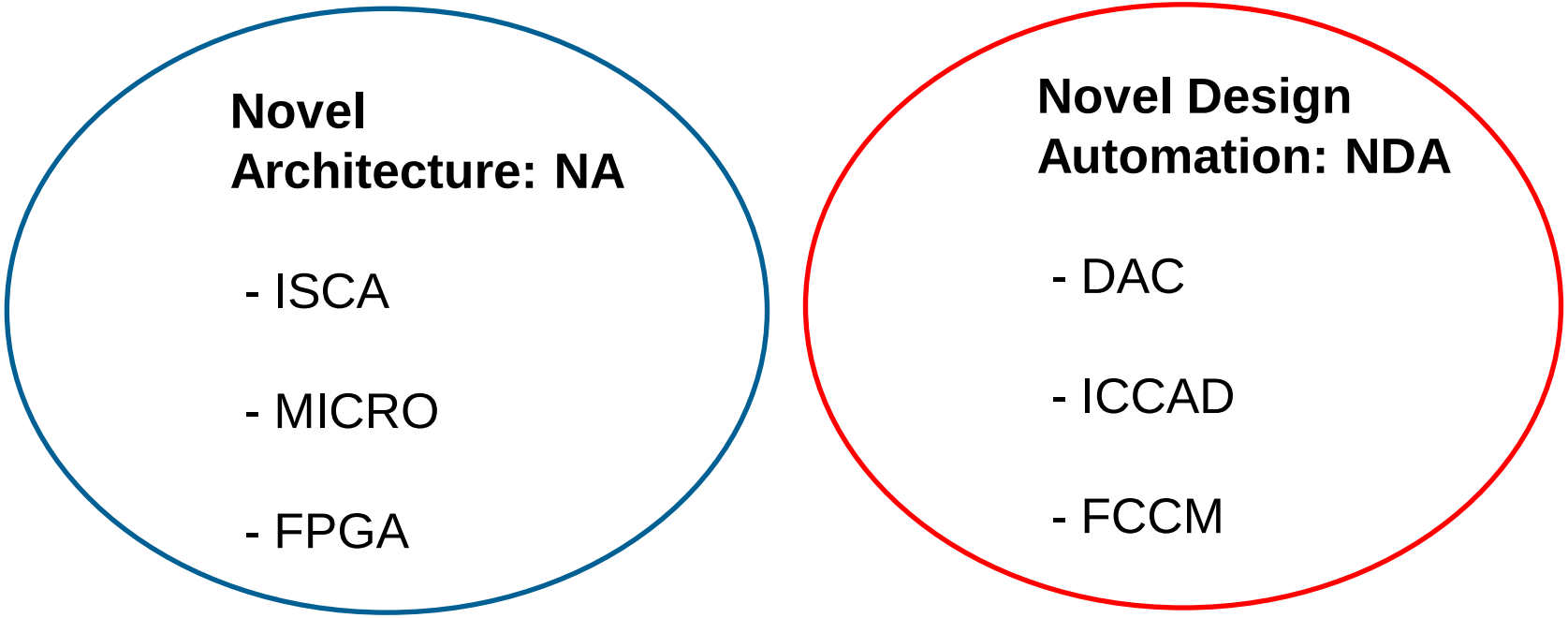
Novel Architecture: NA
- ISCA
- MICRO
- FPGA
Novel Design Automation: NDA
- DAC
- ICCAD
- FCCM

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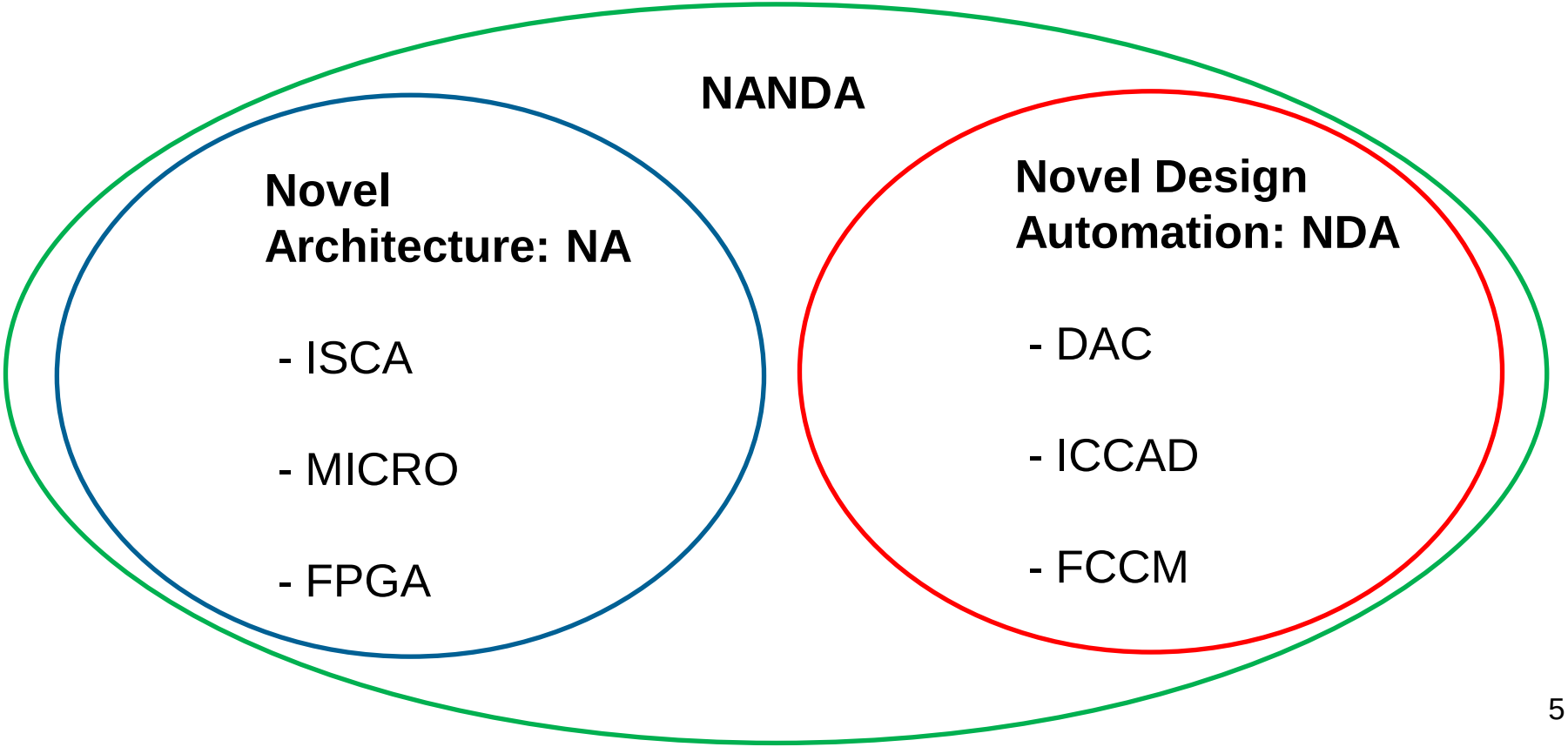
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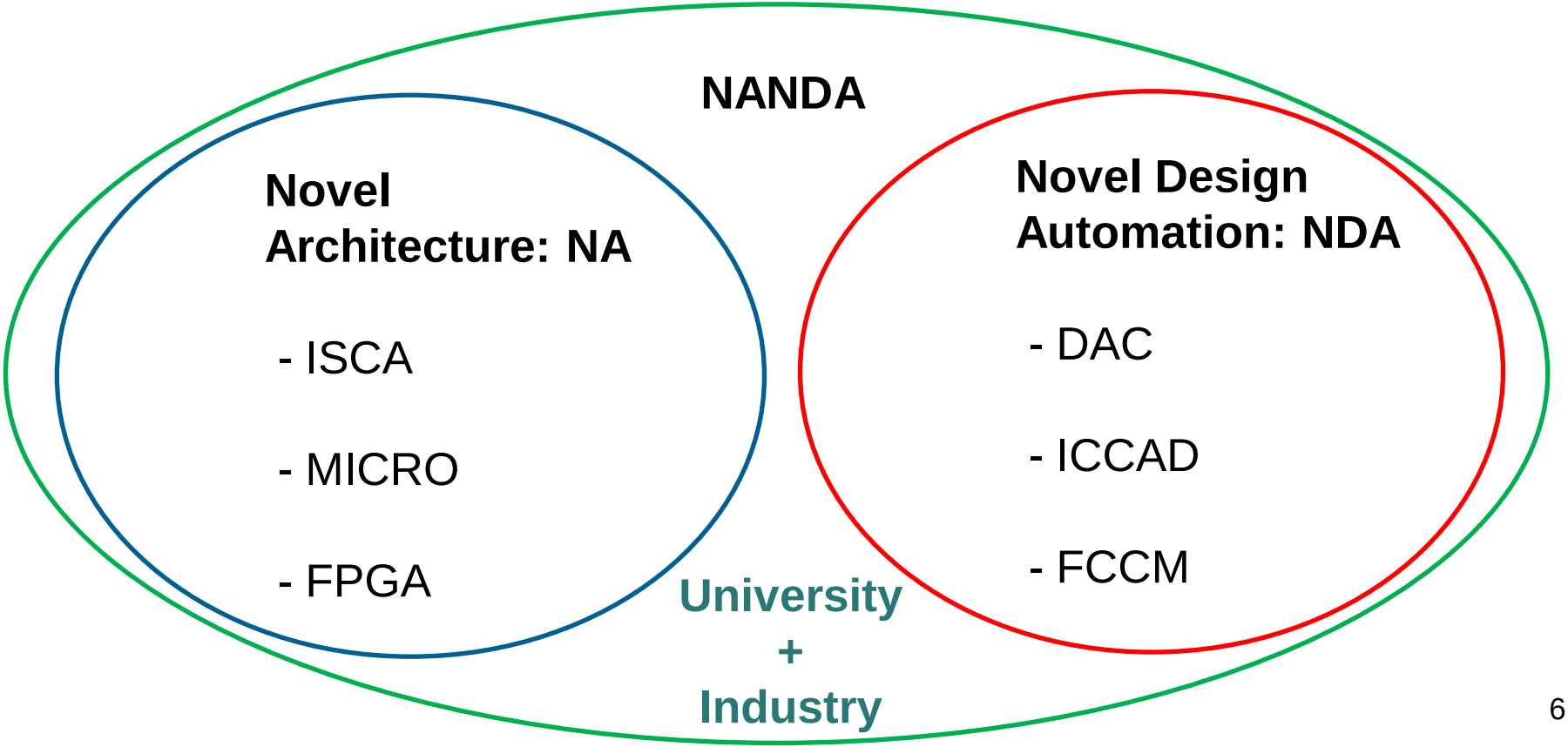
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University + Industry

Agenda: 5 September

09:00 - Wayne Luk, Imperial College. NANDA: the Next Frontier
09:30 - Boris Grot, University of Edinburgh (online). When Serverless Meets Servers
10:00 - Kentaro Sano, RIKEN (online). Dedicated Inter-FPGA Networks for Scalable Reconfigurable Computing
10:30 – Break: Huxley Building Room 315
11:00 - John Wickerson, Imperial College. Bringing Formal Methods to FPGAs
11:30 - Andreas Lööw, Imperial College.
What Interactive Theorem Proving Can Do for Verilog Hardware Development
12:00 - Samuel Coward, Imperial College and Intel. ROVER: RTL Optimisation via Verified E-graph Rewriting
12:30 – Lunch: Huxley Building Room 315
14:00 - David Thomas, University of Southampton.
Co-designing a Language, Tool-chain, and Architecture: Lessons Learnt from the POETS Project
14:30 - Christos-Savvas Bouganis, Imperial College. Efficient Deployment of CNNs under Resource Constraints
15:00 - Alastair Reid, Intel (online). Towards a Formal Specification of Intel's x86 Architecture
15:30 – Break: Huxley Building Room 315
16:00 - Azalea Raad, Imperial College.
Extended Consistency and Persistency Semantics of Intel-x86 Architectures
16:30 - Didem Unat, Koç University. Precise-Event Sampling on x86 Architectures and Its Uses in Profiling Tools
17:00 - Yiying Zhang, UCSD (online). Clio: A Hardware-Software Co-Designed Disaggregated Memory System

Agenda: 6 September

09:00 - Lana Josipović, ETH. From C/C++ to Dynamically Scheduled Circuits
09:30 - William Wang, Arm. Architectural Support for Persistent Memory
10:00 - Sam Ainsworth, University of Edinburgh (online). Vector Runahead for Indirect Memory Accesses

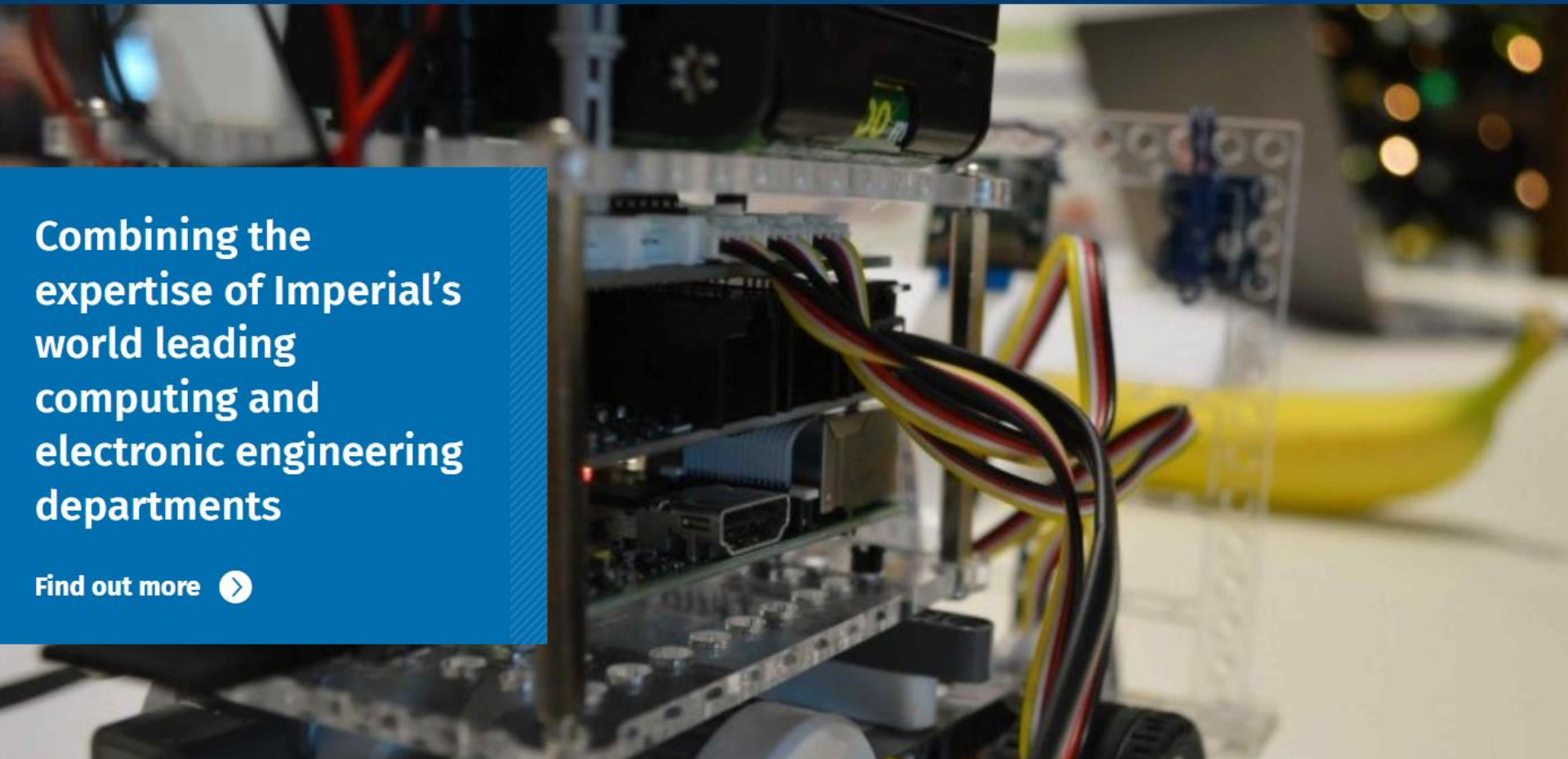
10:30 – Break: Huxley Building Room 315

11:00 - Thomas Chau, Samsung AI Centre (online).
Neural Processing Unit for Transformers and Hardware-Neural-Network Co-Design
11:30 - Tobias Grosser, University of Edinburgh (online). Compiler IRs: The Gold of Computer Systems
12:00 - Carl-Johan Seger, Chalmers University of Technology (online).
Integrated Design and Verification: An Ounce of Prevention is Worth a Pound of Cure
12:30 - Mikel Luján, University of Manchester. Towards Ubiquitous Accelerators

12:30 – Lunch: Huxley Building Room 315

14:00 - Paul Kelly, Imperial College (online). Towards Cross-Domain Domain-Specific Compiler Architecture
14:30 - Lluis Vilanova, Imperial College (online).
Security as a Performance Principle: a Tale on Hardware/Software Codesign
15:00 - Alexandra Jimborean, University of Murcia (online). The Entangling Instruction Prefetcher

HiPEDS Centre



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