The Entangling Instruction Prefetcher

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DATA CENTERS

GOAL: BOOSTING DATA SERVERS' PERFORMANCE AND ENERGY EFFICIENCY

- Data centers serve most devices
  - Daily online activities
  - Internet of things, smartphones, self-driving cars, etc.
  - Energy costs expected to reach 8% of the global consumption by 2030[1]

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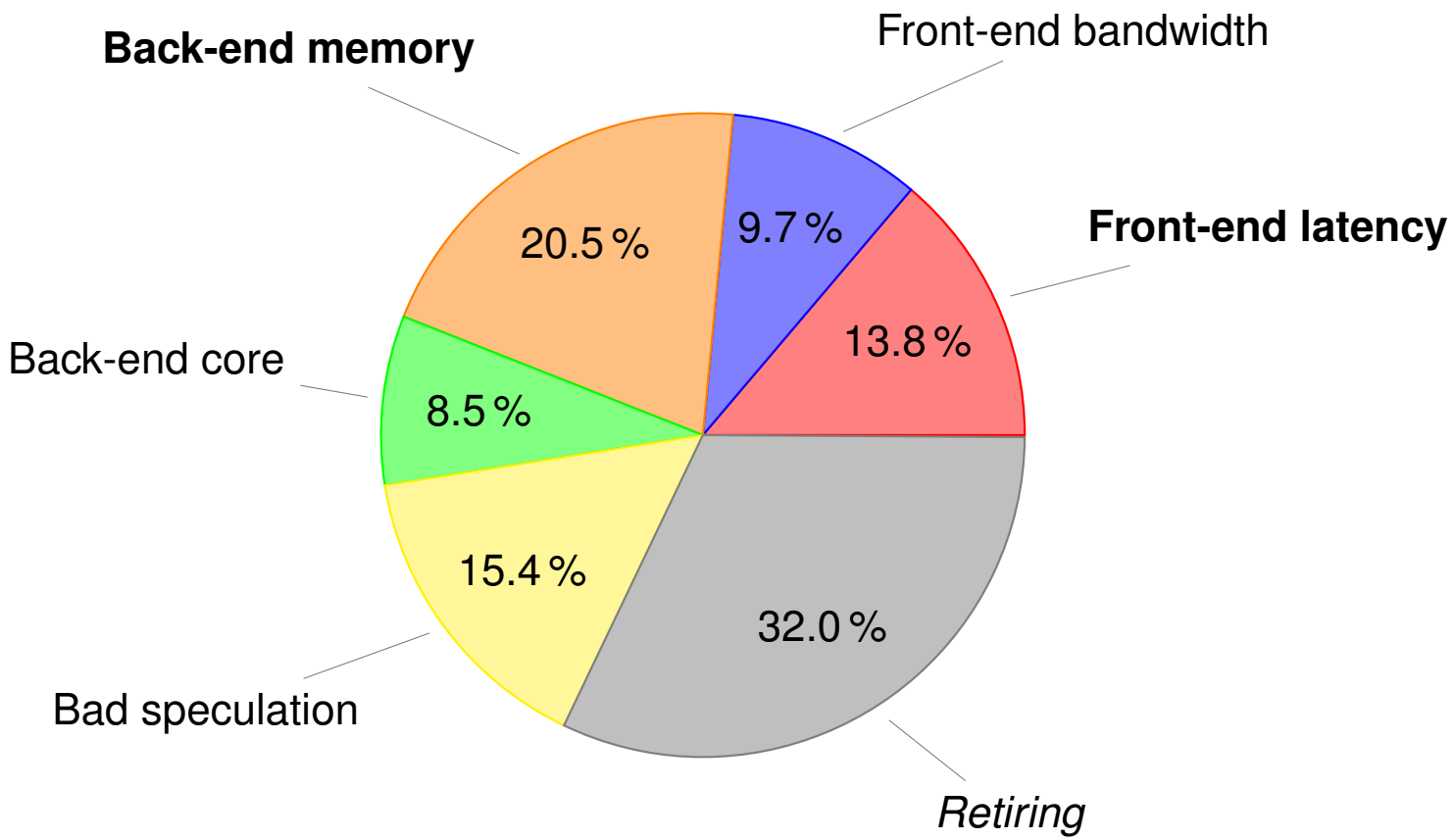
  - Internet of things, smartphones, self-driving cars, etc.
  - Energy costs expected to reach 8% of the global consumption by 2030[1]
- They run increasingly complex applications
  - Deep software stacks
- Instruction footprint constantly growing
  - Far from fitting in small instruction caches (L1I)
  - And growing by 20% per year![2]

[1] Andrae et al. *On Global Electricity Usage of Communication Technology: Trends to 2030*, Callenges 2015.

[2] Kanev et al. *Profiling a warehouse-scale computer*, ISCA 2015.

DATA CENTERS BOTTLENECKS[3]



[3] Ayers et al. *AsmDB: Understanding and Mitigating Front-End Stalls in Warehouse-Scale Computers*, ISCA 2019.

Data centers bottlenecks

Front-end latency (13.8%)

- Dominated by instruction cache (L1I) misses
  - Hiting in the second level cache (L2) or last level cache (LLC)
- Latency more important than bandwidth
- Critical as processors need to keep the pipeline full

Back-end memory (20.5%)

- Due to data cache (L1D) misses
  - Many of them reaching main memory
- Cause significant stalls and late detection of bad speculation (15.4%)

PREFETCHING TO THE RESCUE

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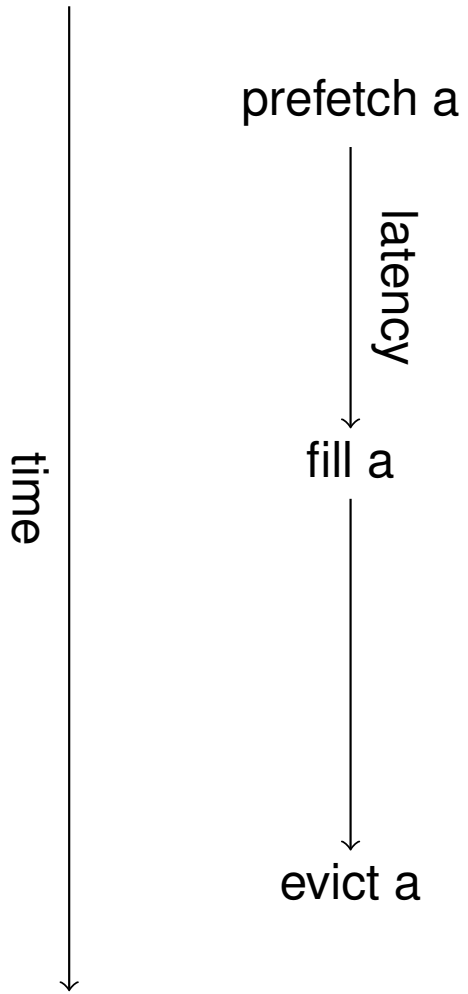
PREFETCHING

Predict which memory addresses will be accessed by the processor and fetch them before the processor requests them

TIMELINESS IS THE KEY PROPERTY



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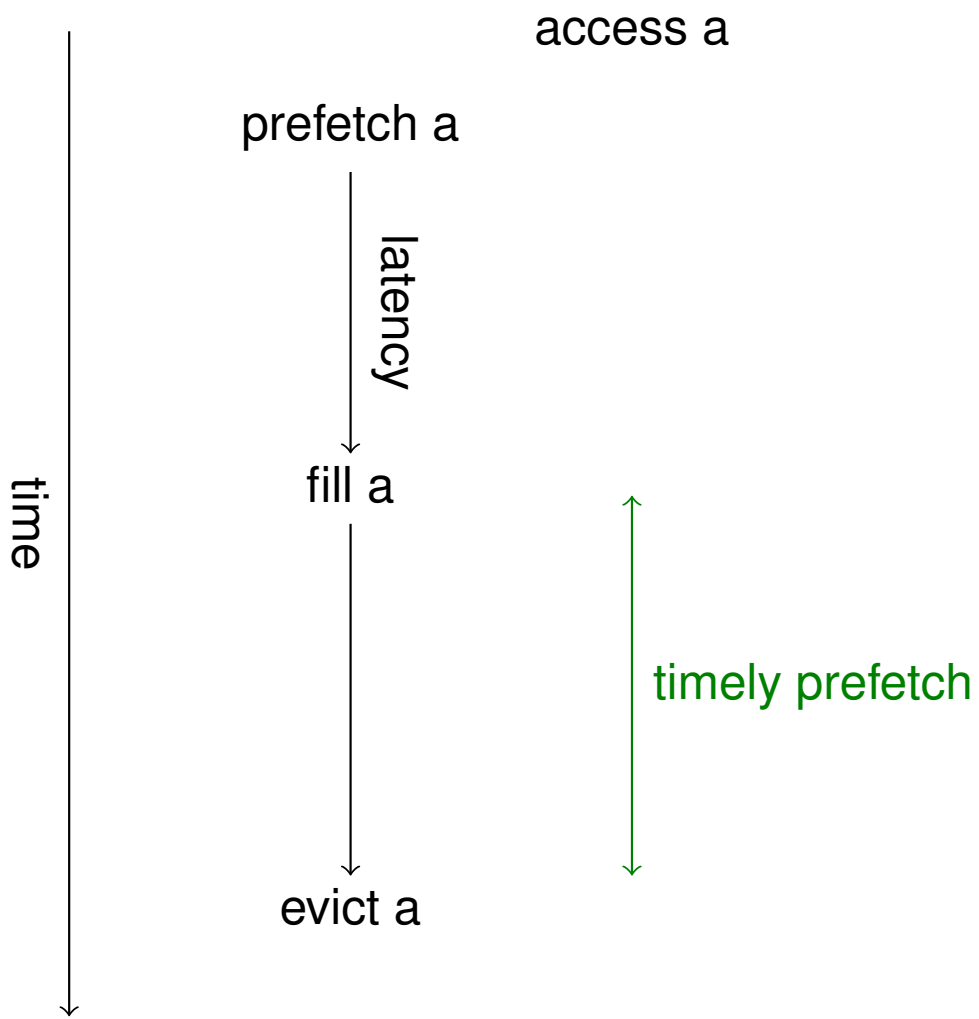

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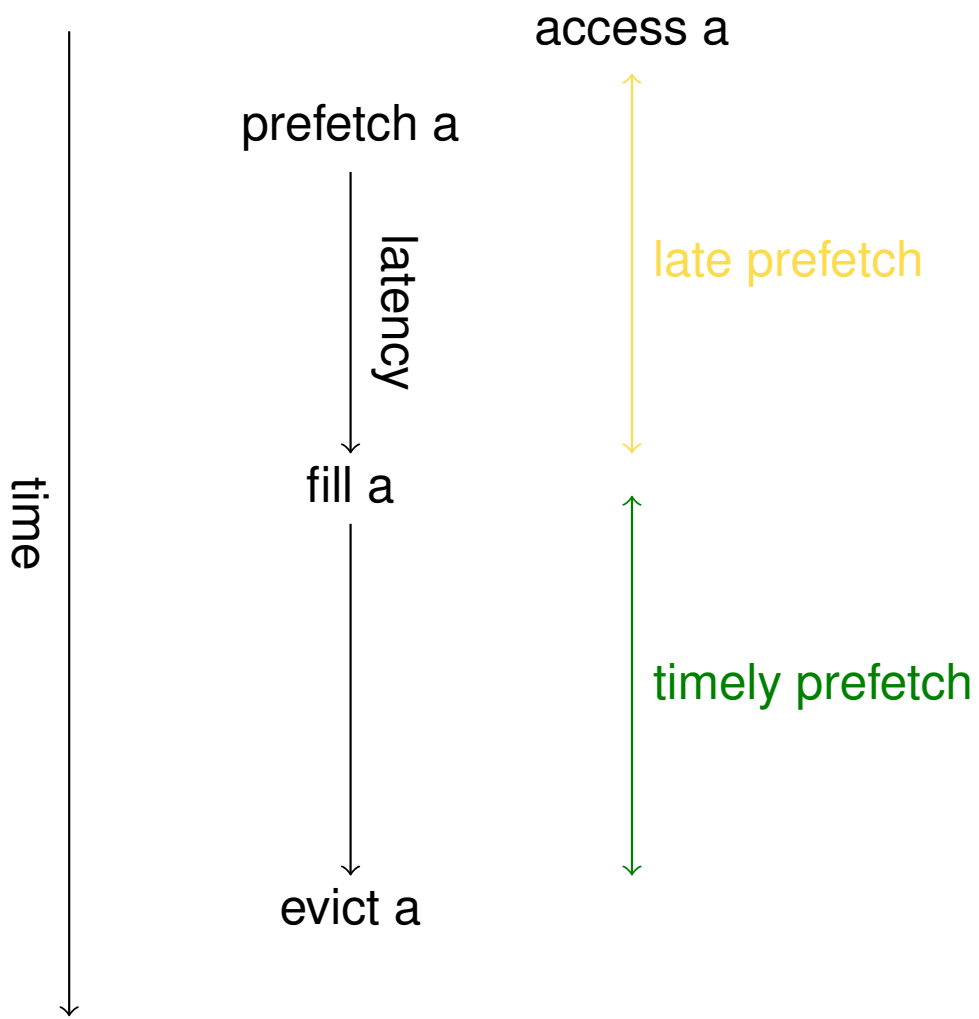

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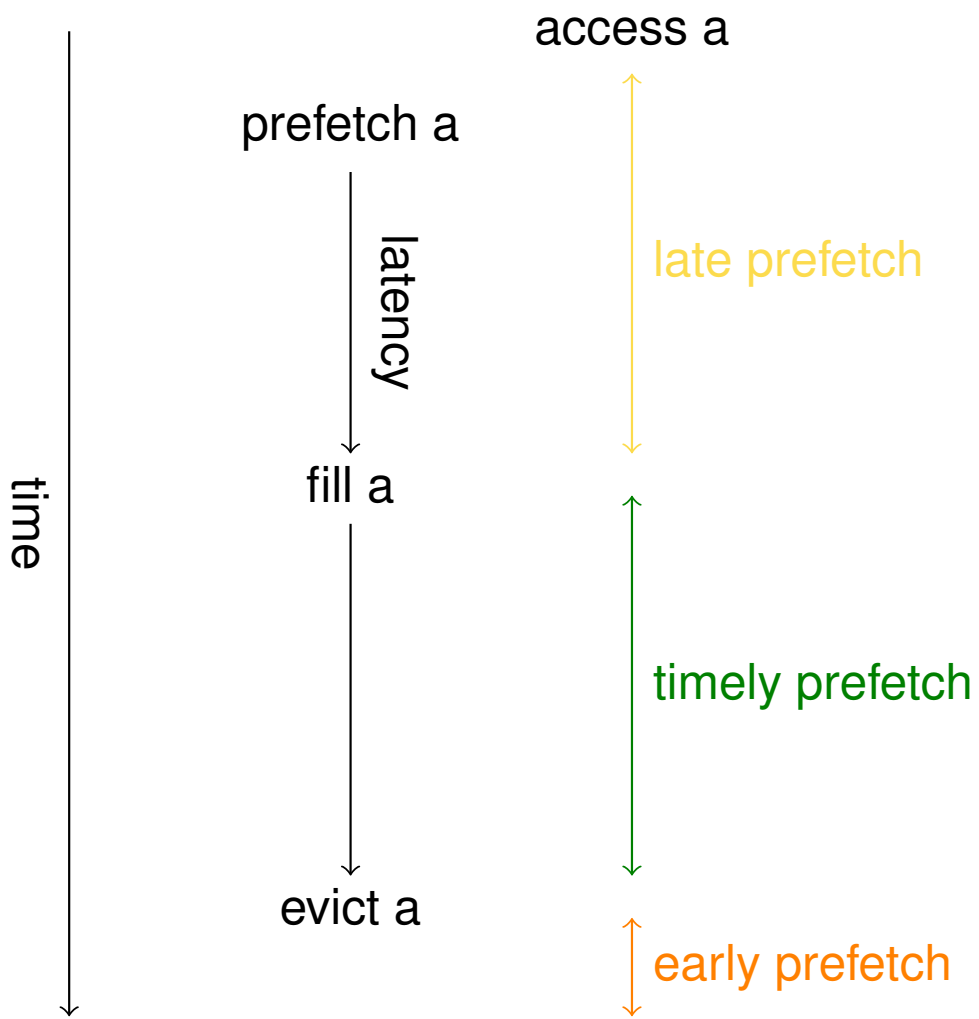

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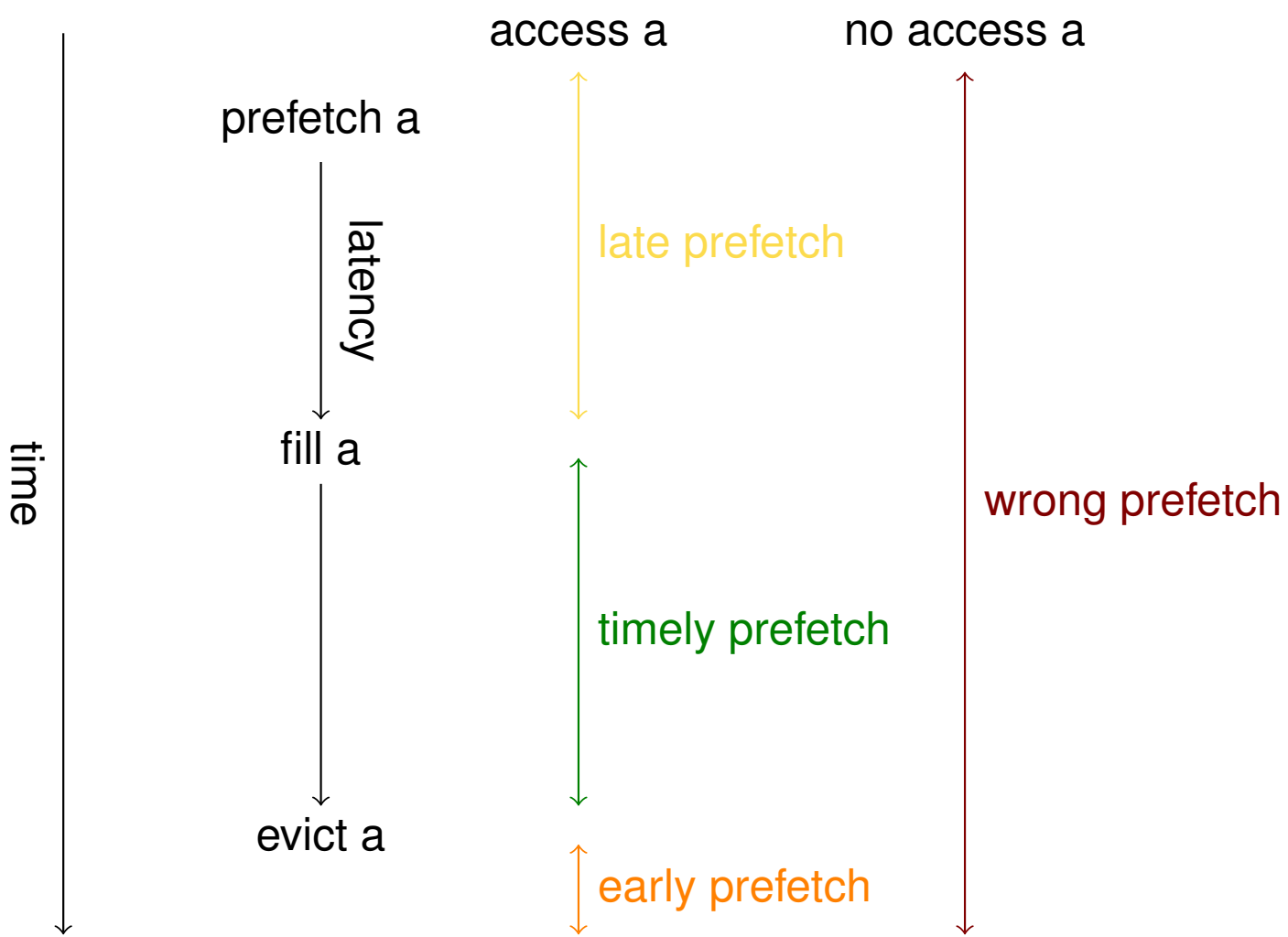

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[5] Ros and Jimborean, *The Entangling Instruction Prefetcher*, IPC-1 2020

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- An L1I prefetcher
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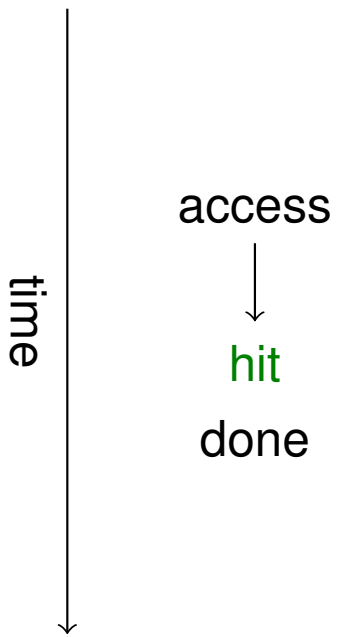
THE ENTANGLING INSTRUCTION PREFETCHER

- Server and cloud apps getting larger, far from fitting in L1I
  - $\Rightarrow$ stalls processor front-end, performance degradation
- Prefetching instructions is fundamental for performance
  - Even when a decoupled front-end is implemented
- Solution: The ENTANGLING instruction prefetcher[6]
  - ENTANGLING: adaptive correlation based on latency
  - A cost-effective prefetcher
  - Prefetcher code is available[7]

[6] Ros and Jimborean, *A Cost-Effective Entangling Prefetcher for Instructions*, ISCA 2021

[7] `https://github.com/alberto-ros/EntanglingInstructionPrefetcher`

MOTIVATION: TIMELINESS



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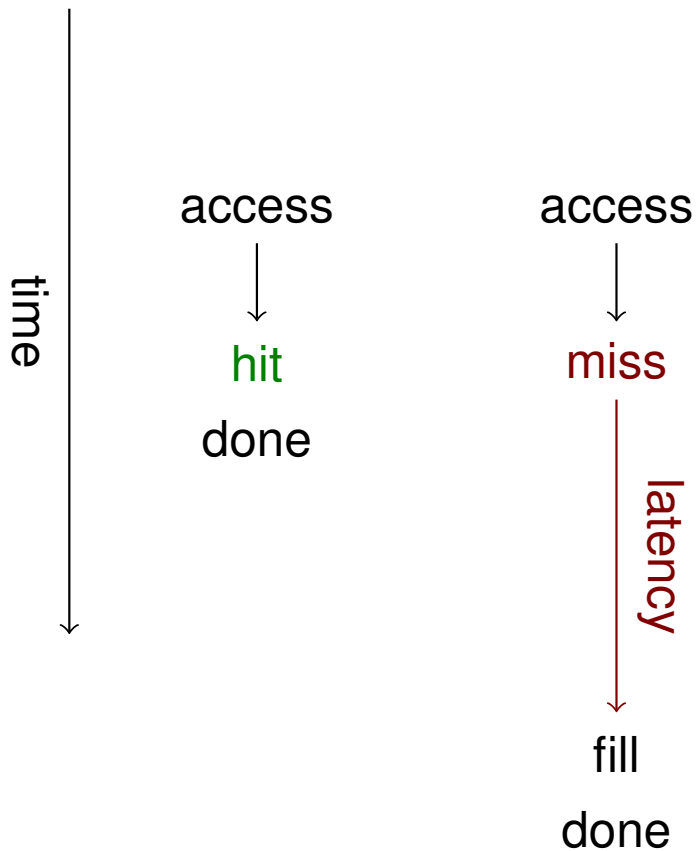

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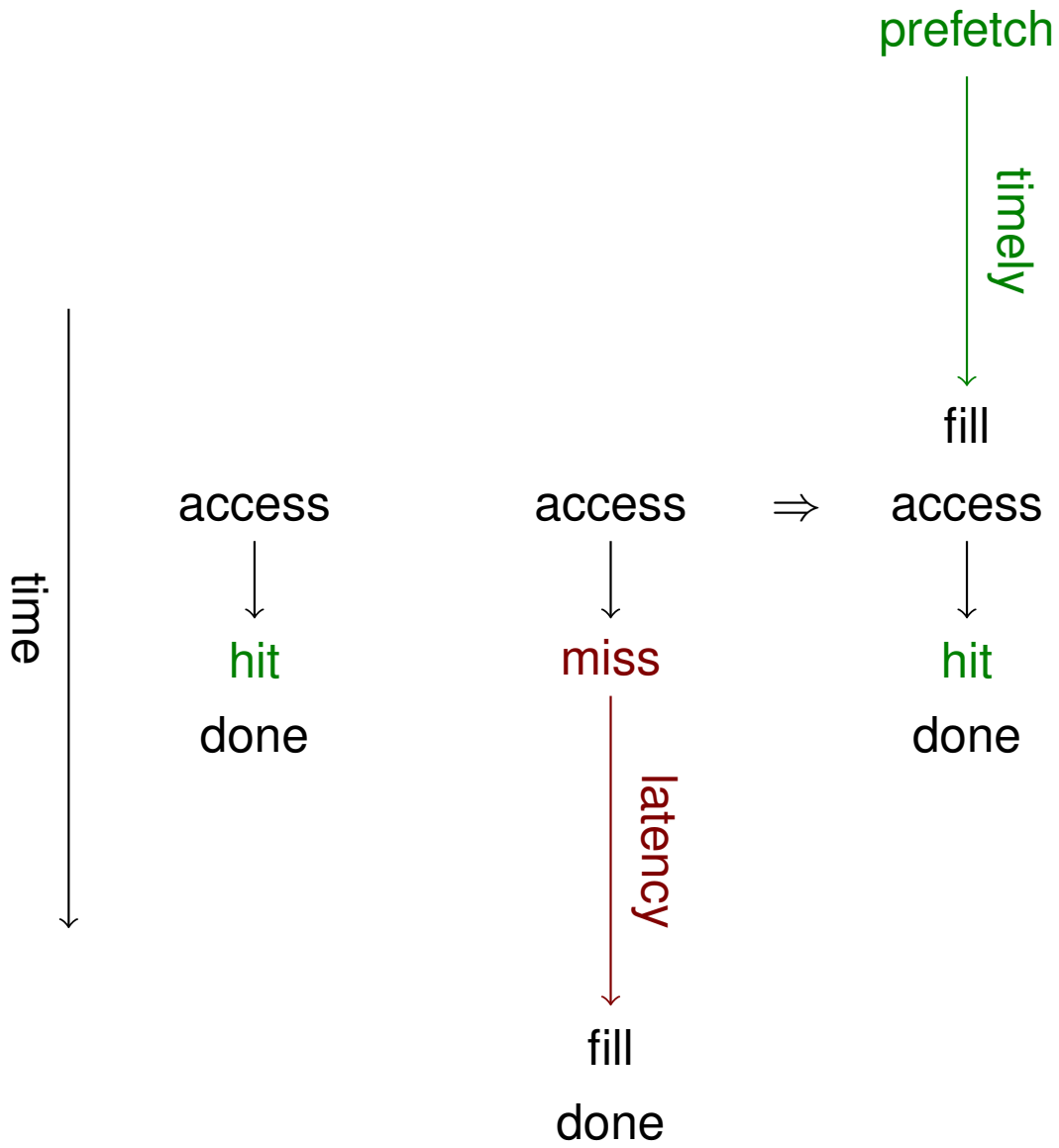

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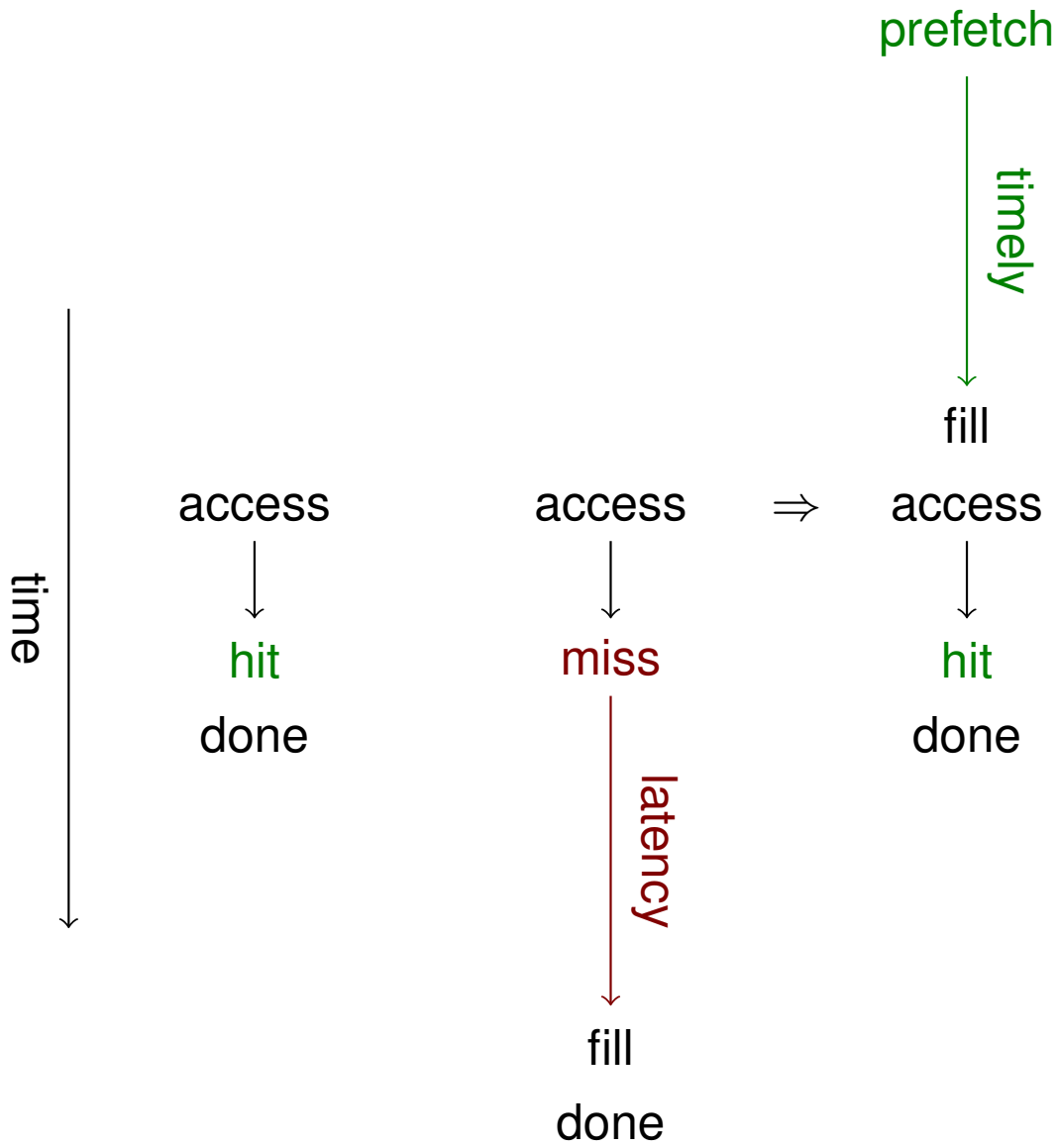

Timely prefetches for all misses:
Coverage 100%

And only for misses:
Accuracy 100%

CONCEPT OF ENTANGLED ACCESSES

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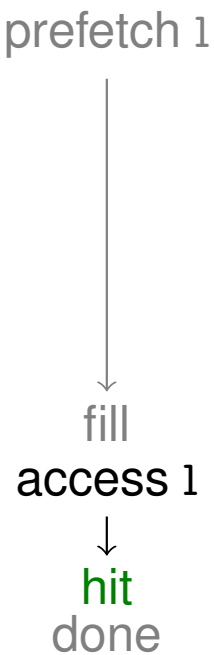

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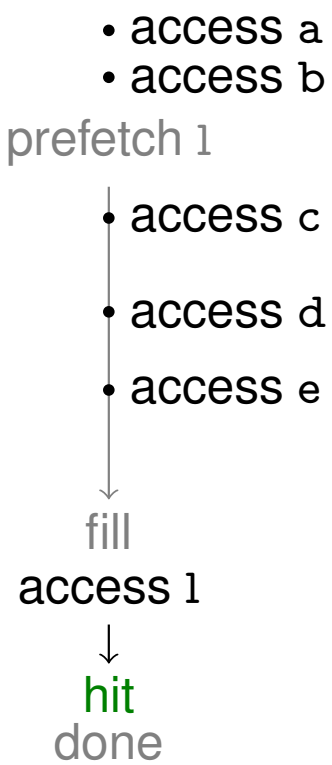

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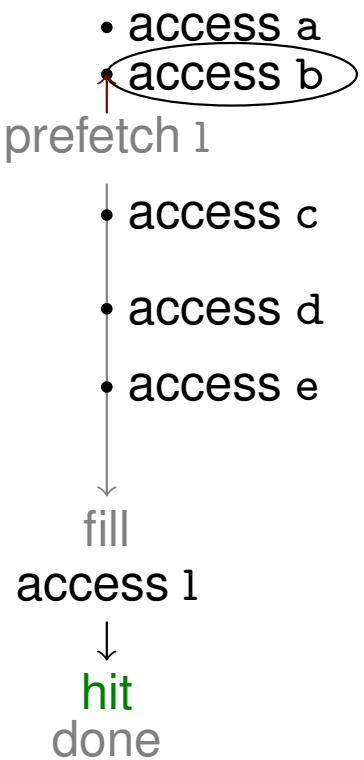

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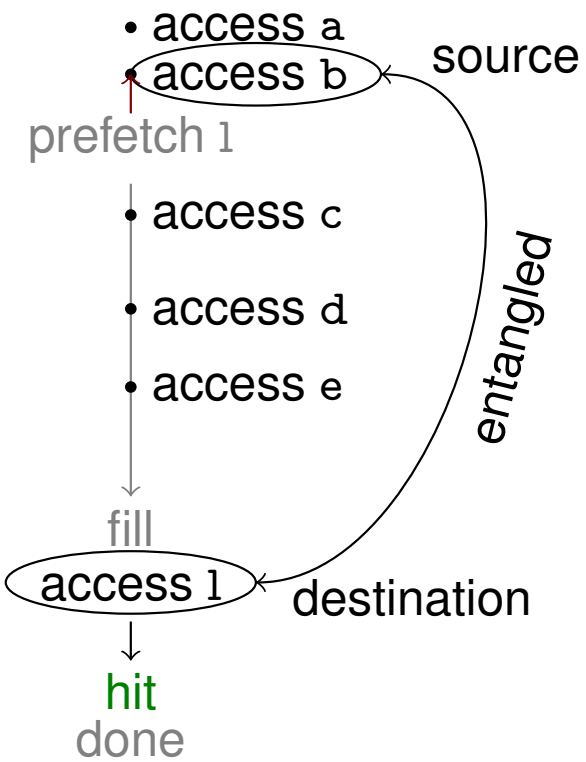

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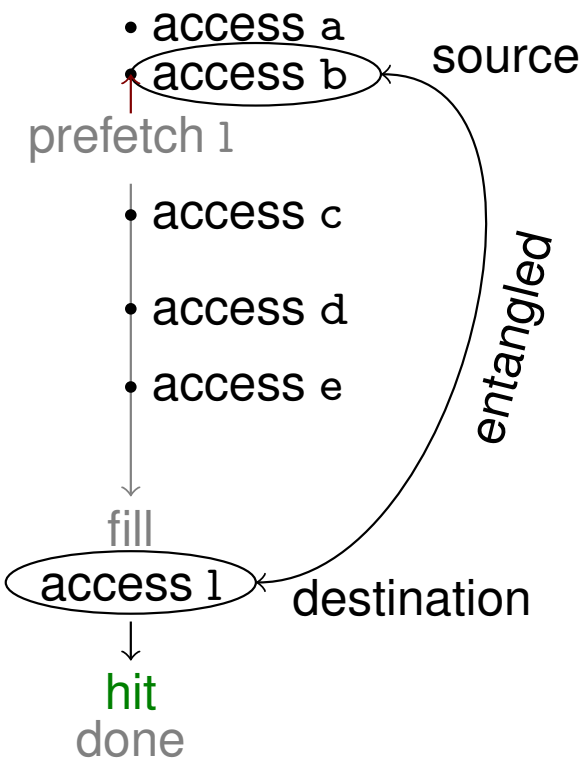

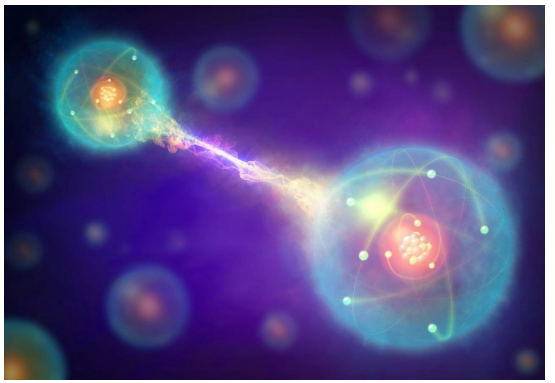

Quantum entanglement

(Image: © MARK GARLICK/SCIENCE PHOTO LIBRARY/Getty)

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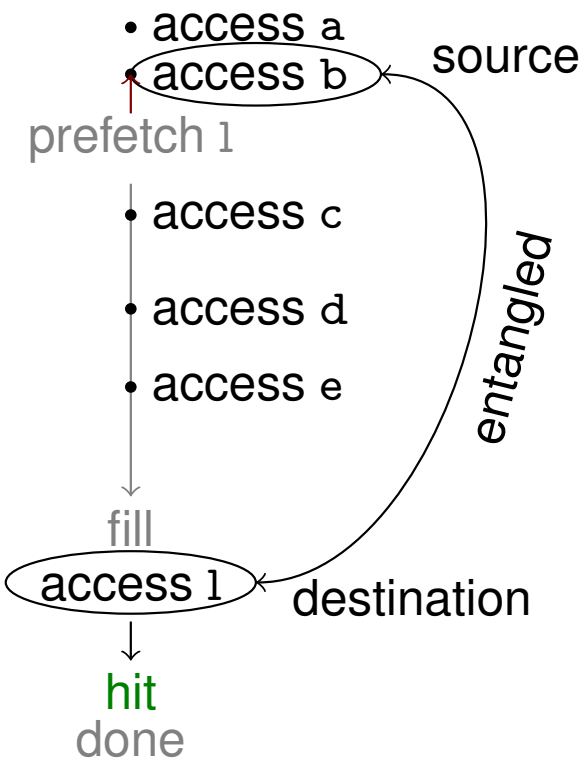

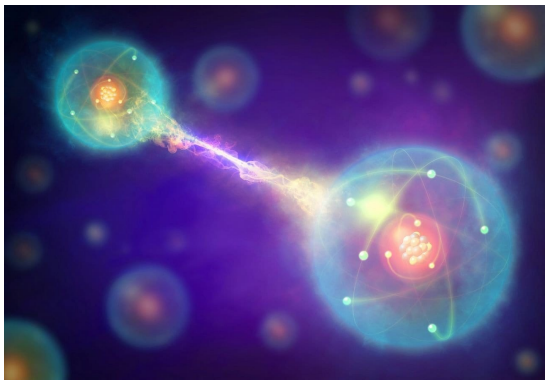

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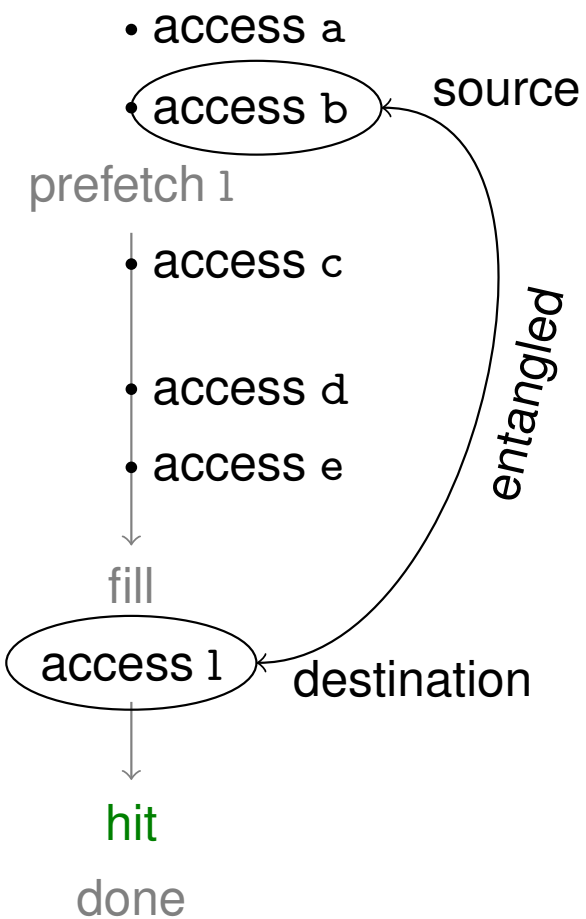
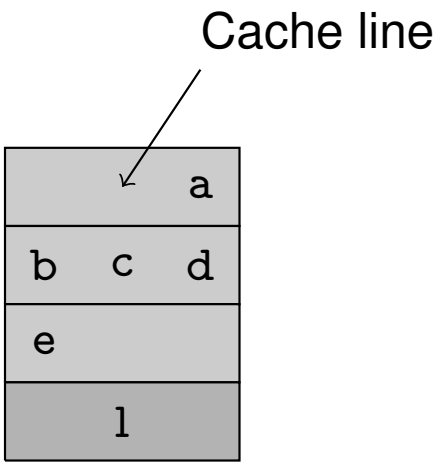
THE ENTANGLING PREFETCHER FOR INSTRUCTIONS

ENTANGLING CACHE LINES HEAD OF BASIC BLOCKS





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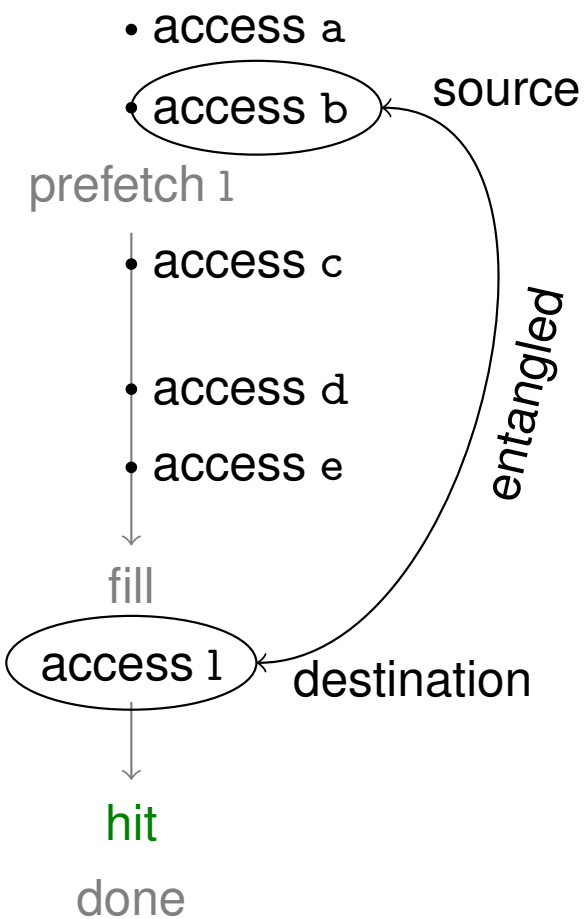

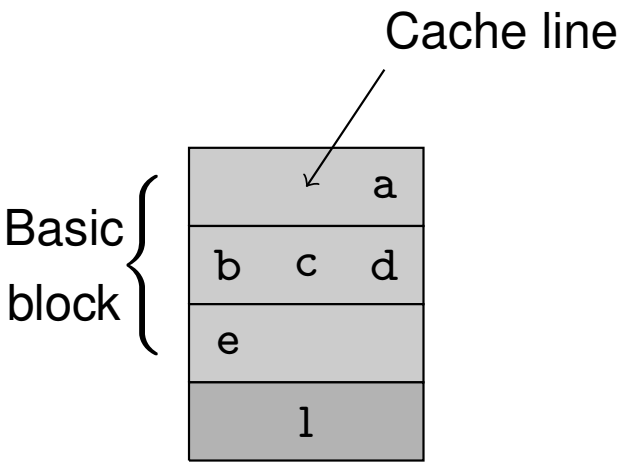

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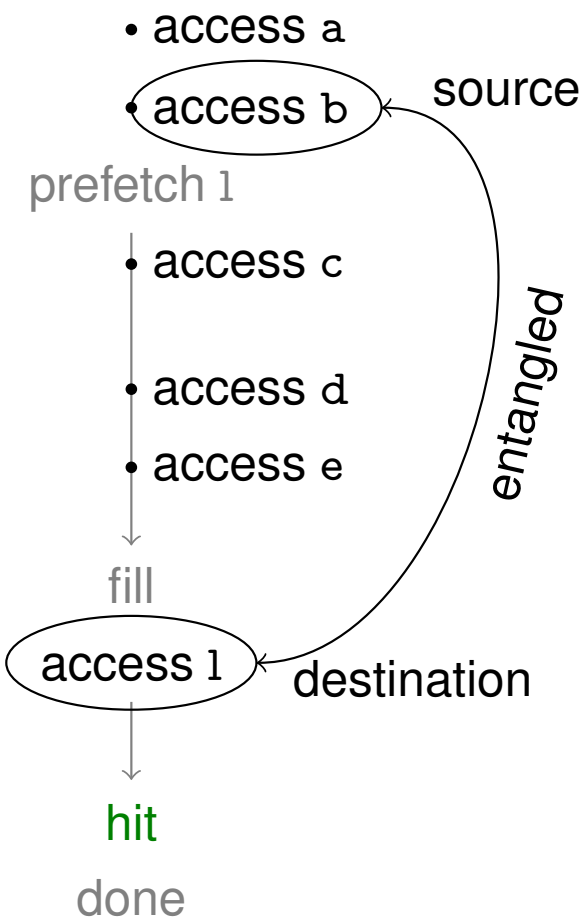

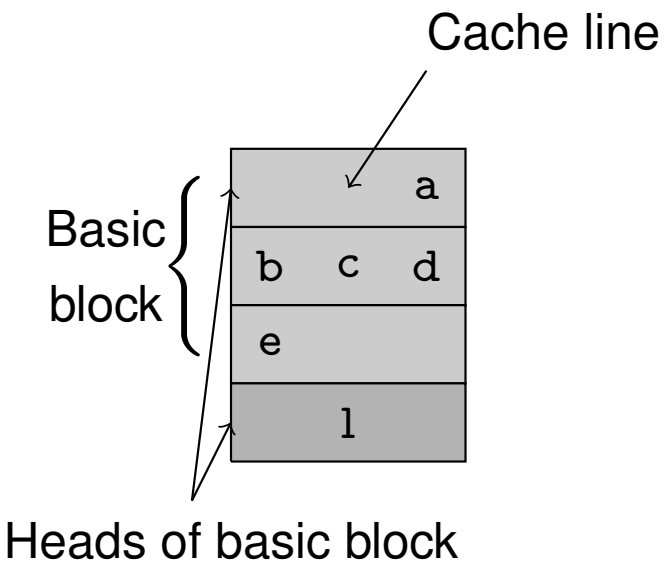

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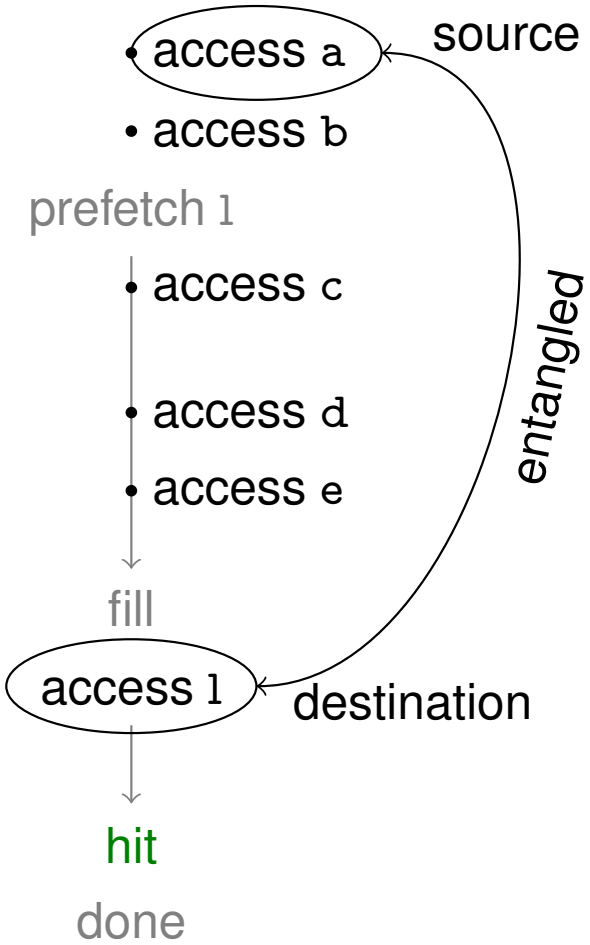
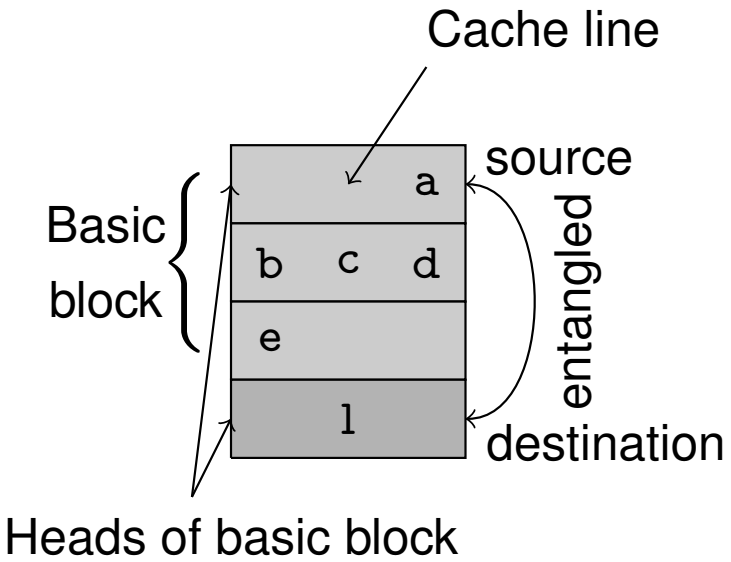
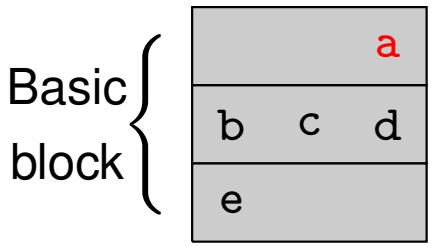




WHAT TO PREFETCH ON AN ACCESS TO a?



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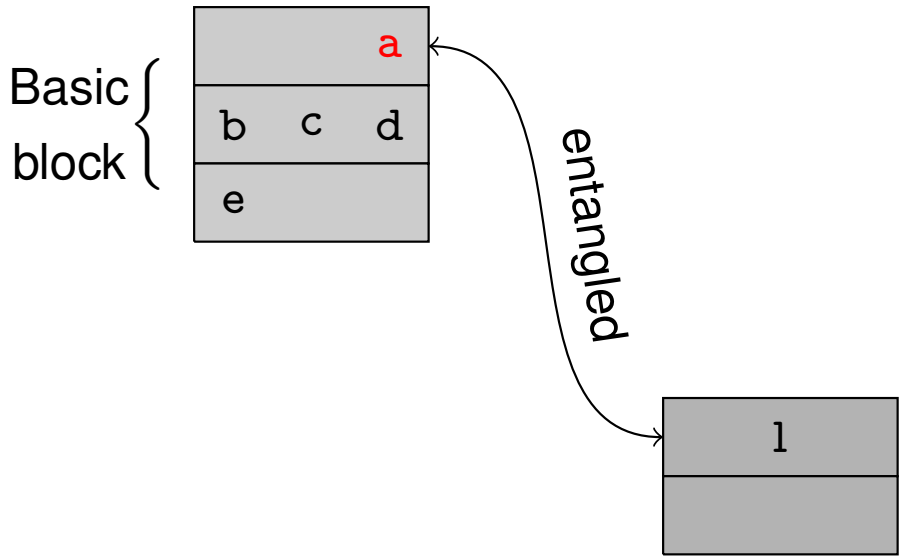

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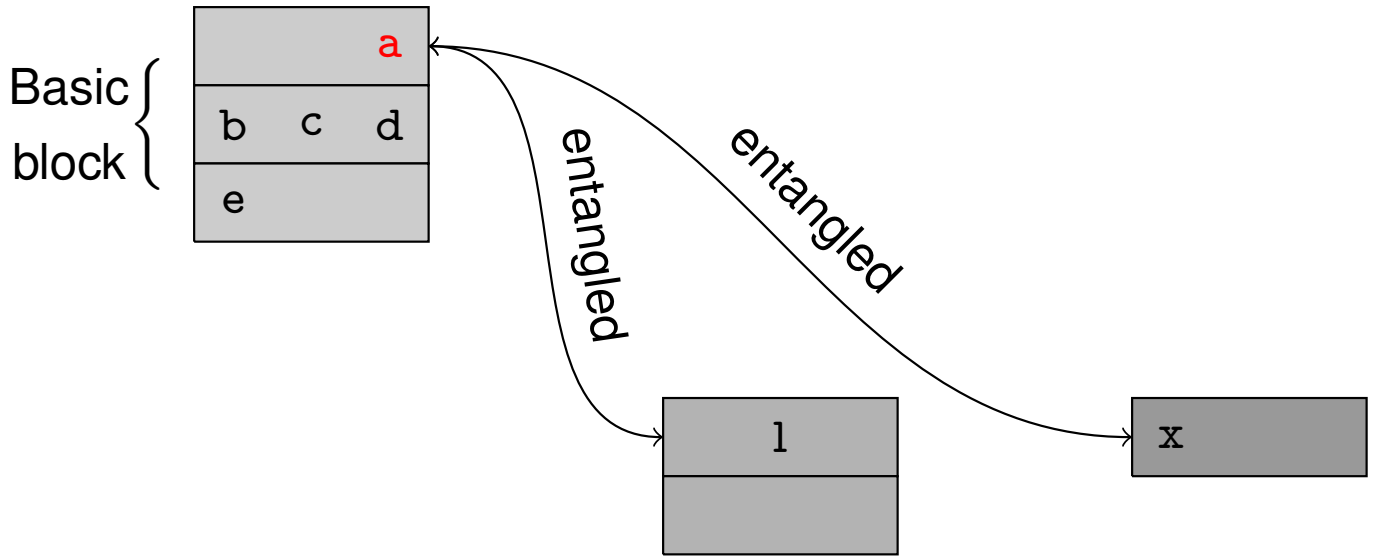

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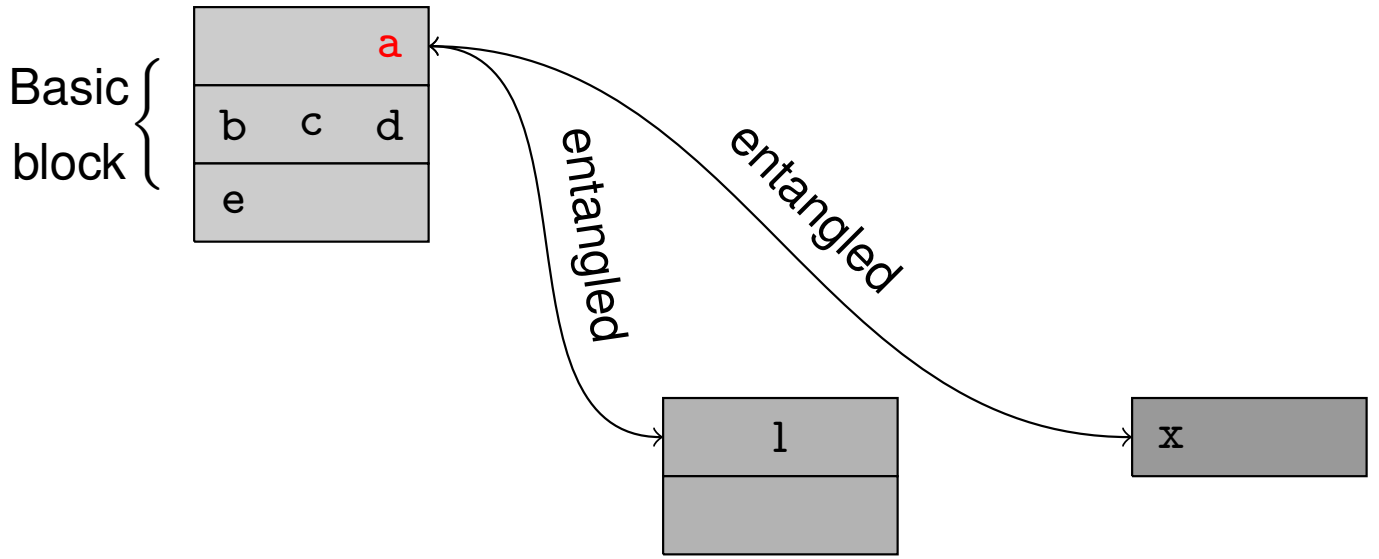

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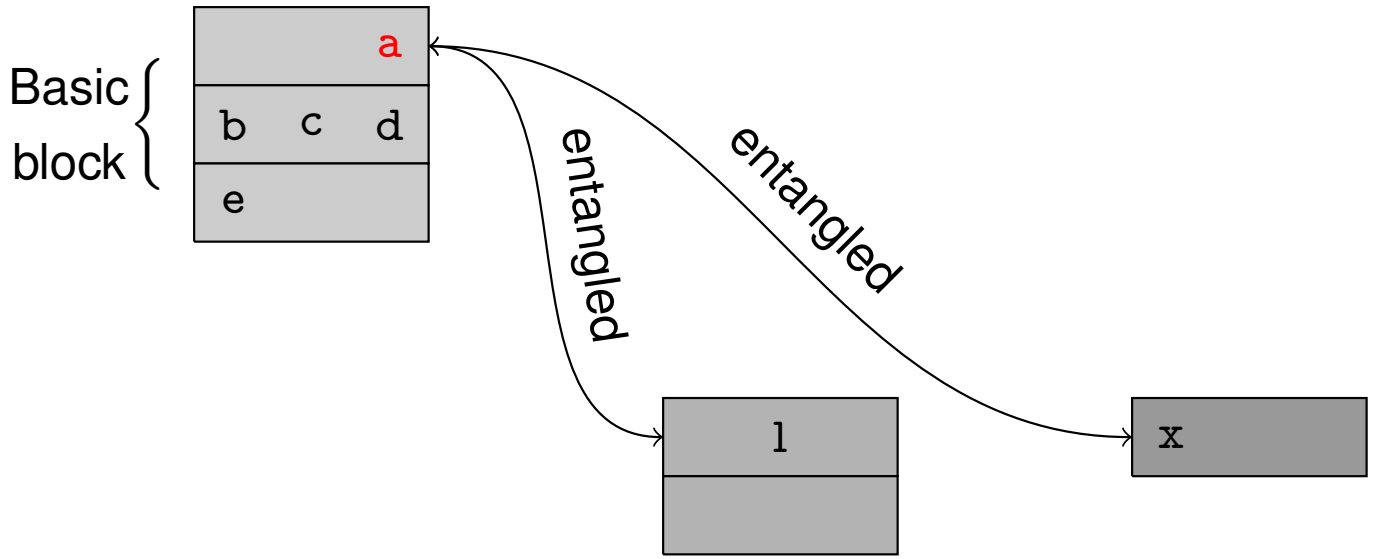

- Too much? (Max entangled = 6, Max BB size = 64)
  - Most of the time no prefetches are issued (no head of basic block)
  - Average number of prefetches per access to head of basic block ranging from ≈9 to ≈17
  - Remember: Front-end latency more imporant than bandwidth[8]

[8] Kanev et al. *Profiling a warehouse-scale computer*, ISCA 2015.

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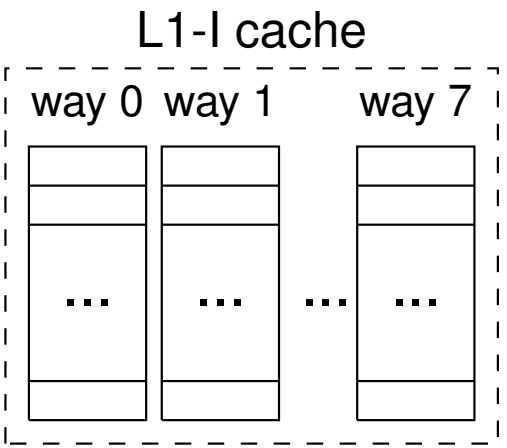

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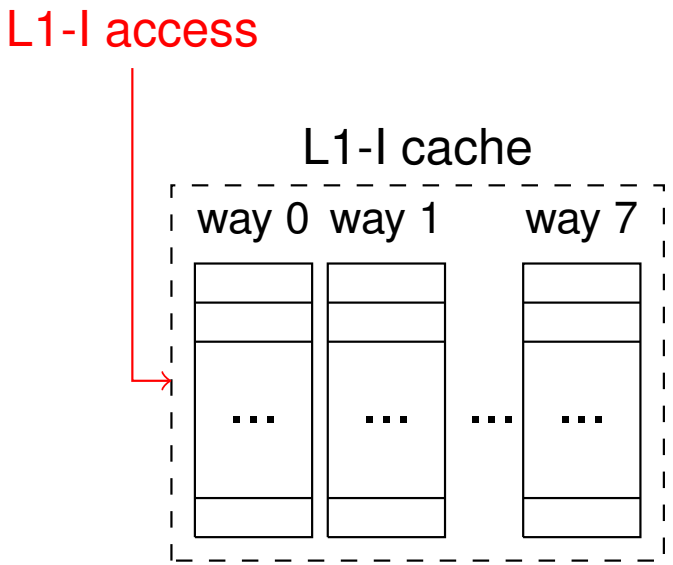

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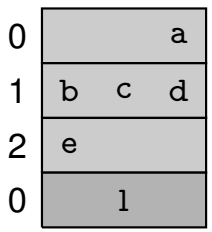

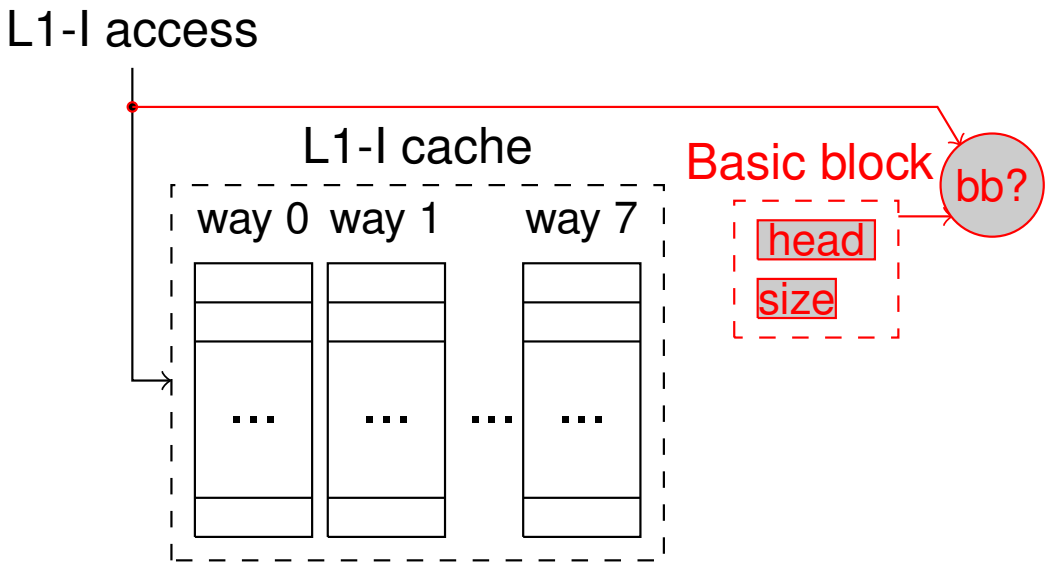

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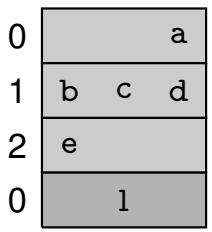

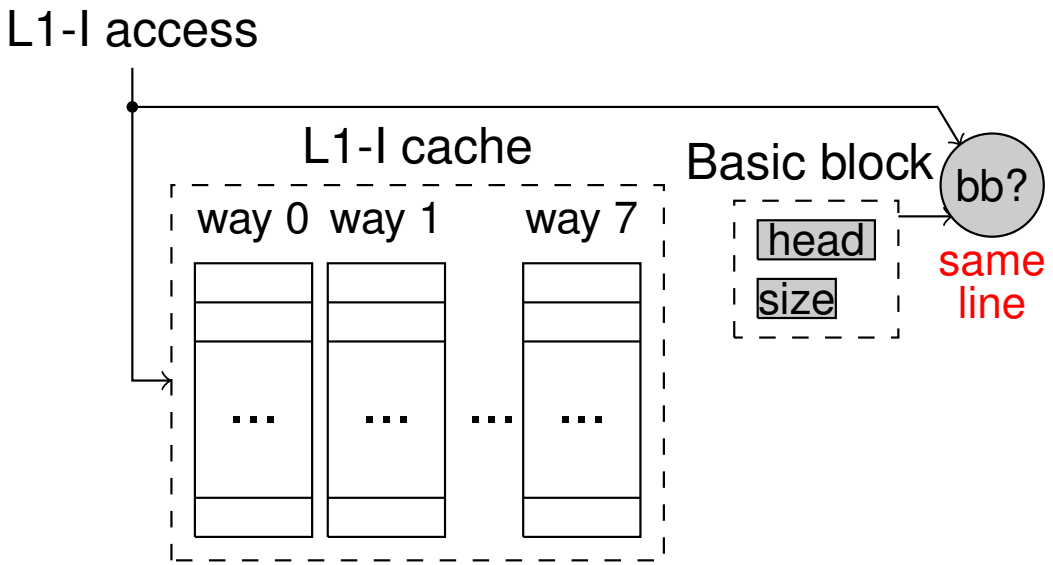

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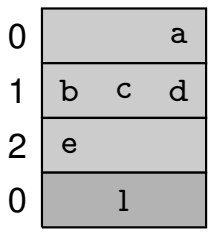

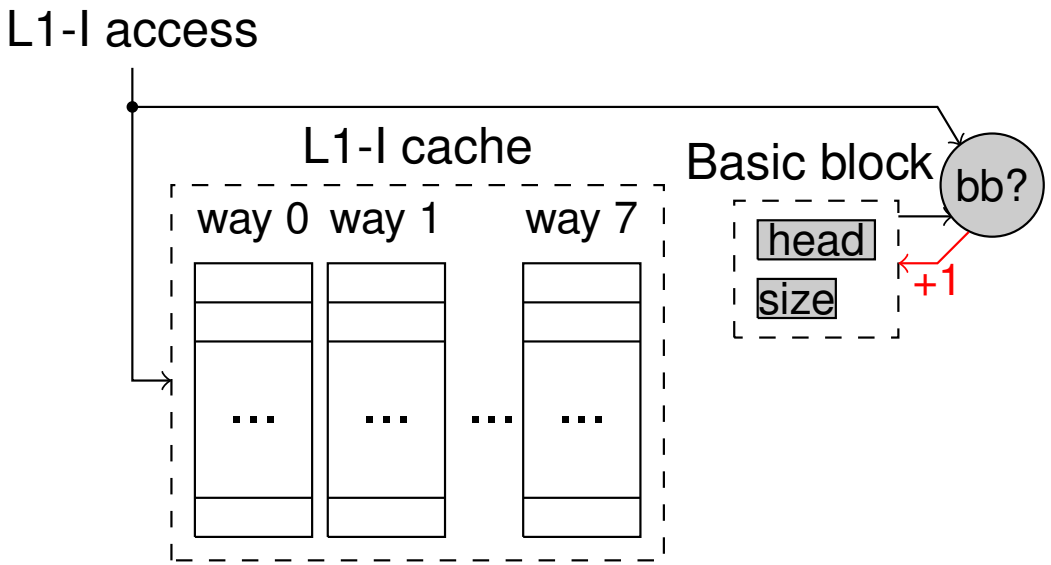

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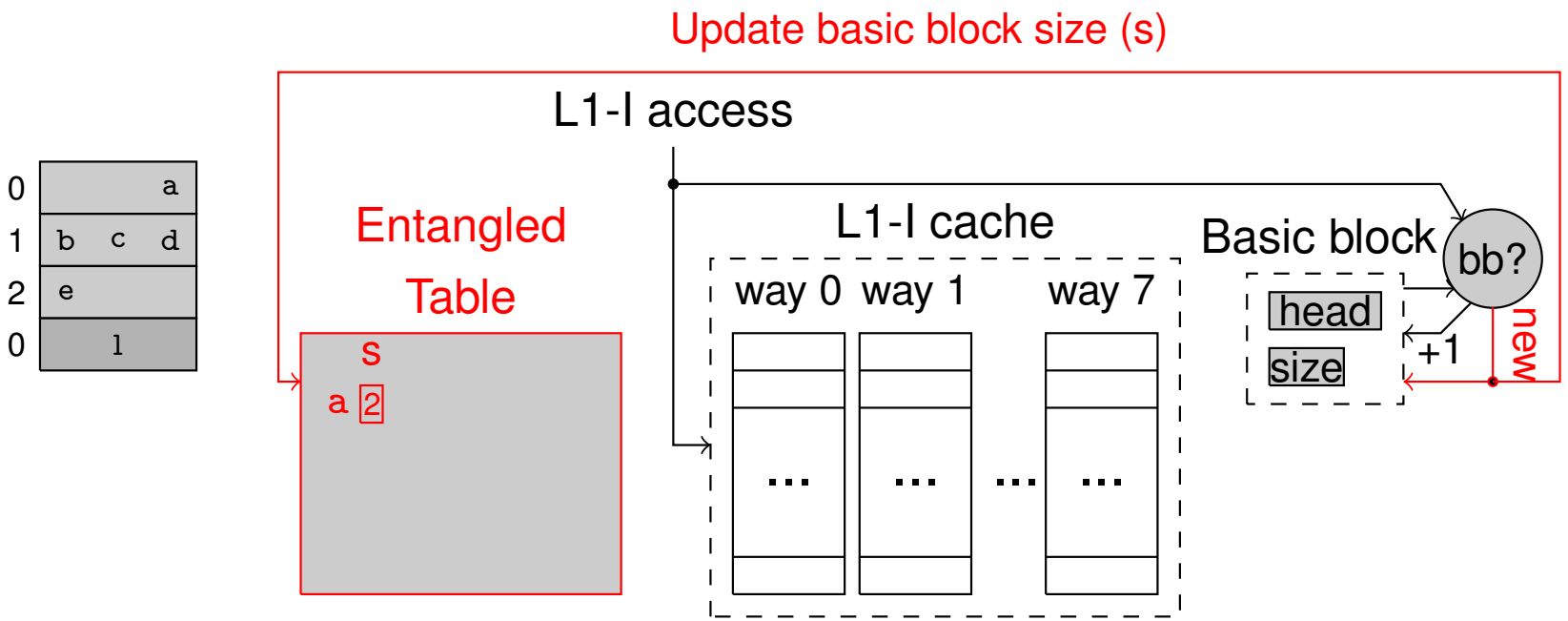

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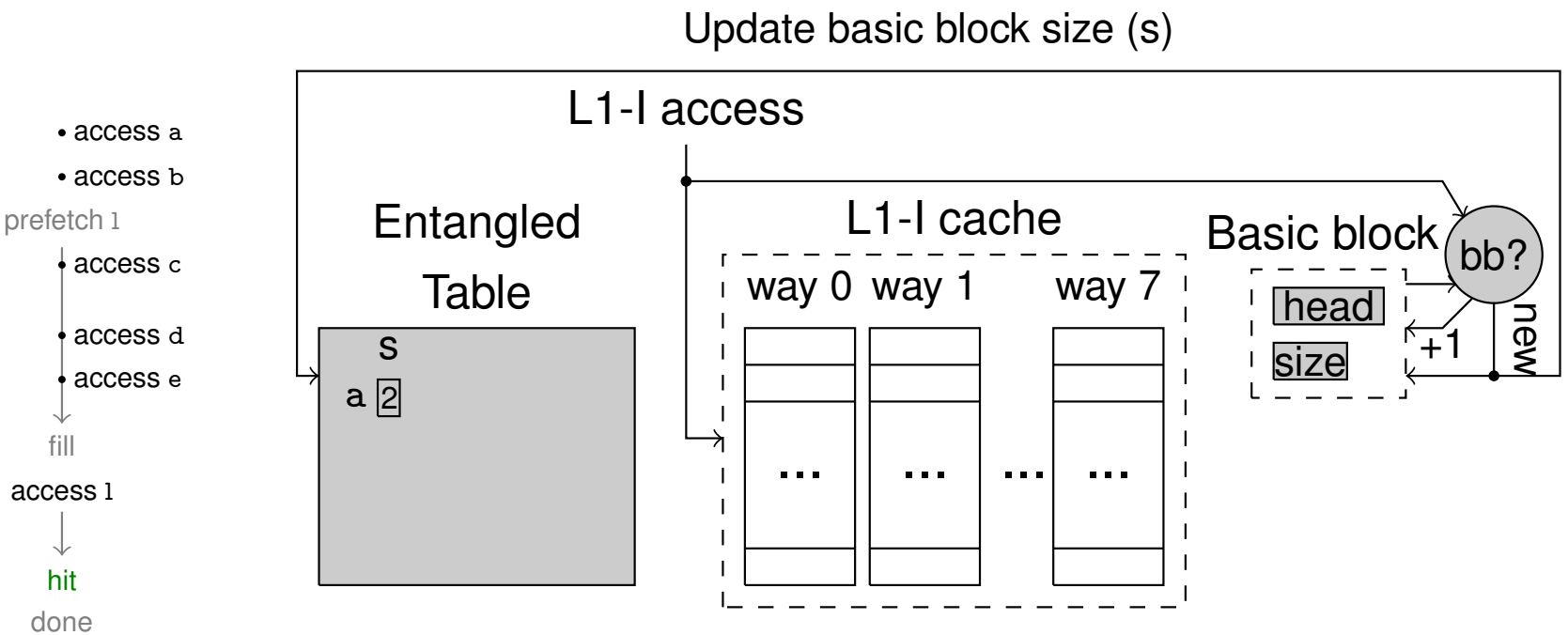

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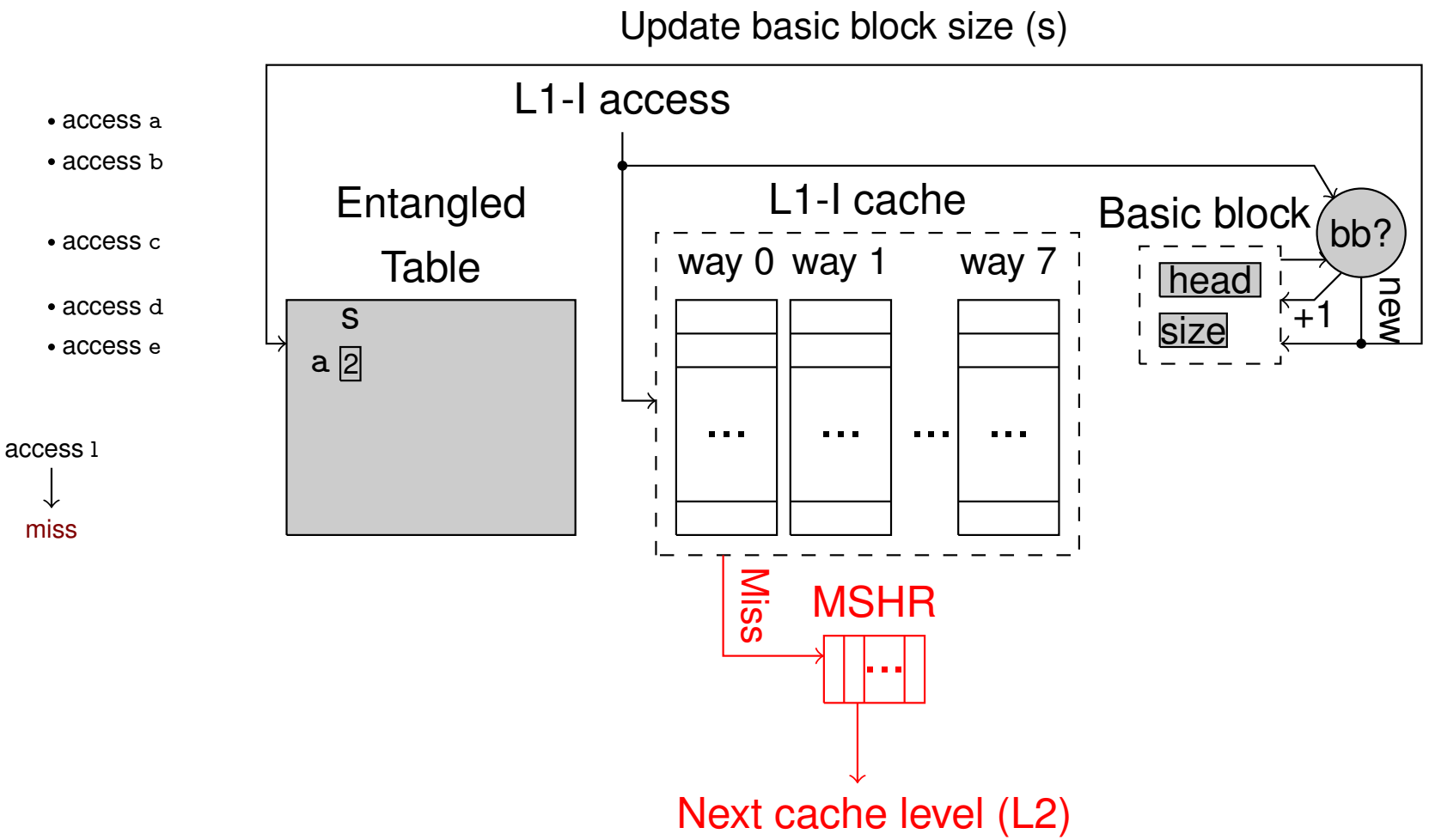

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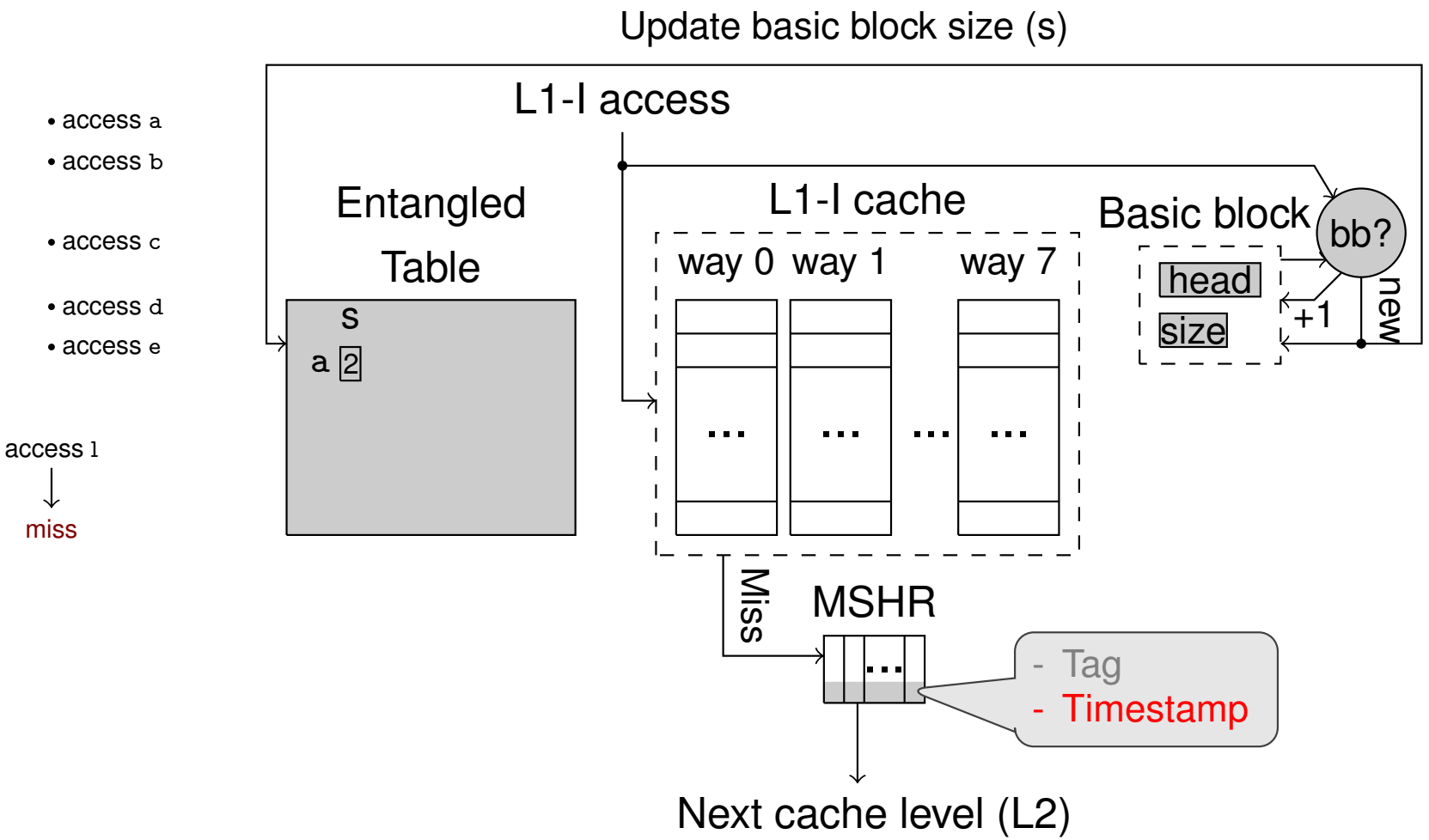

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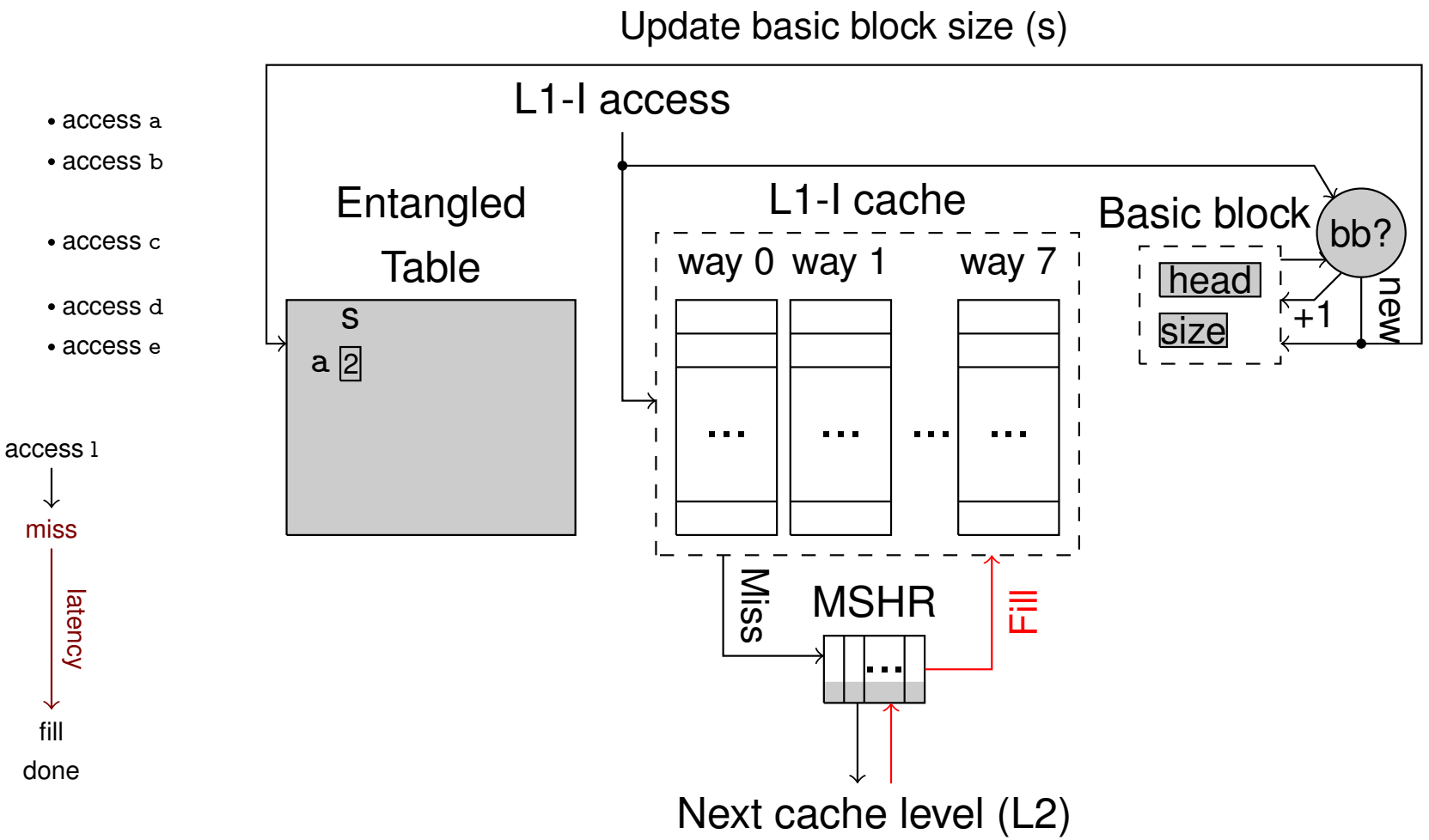

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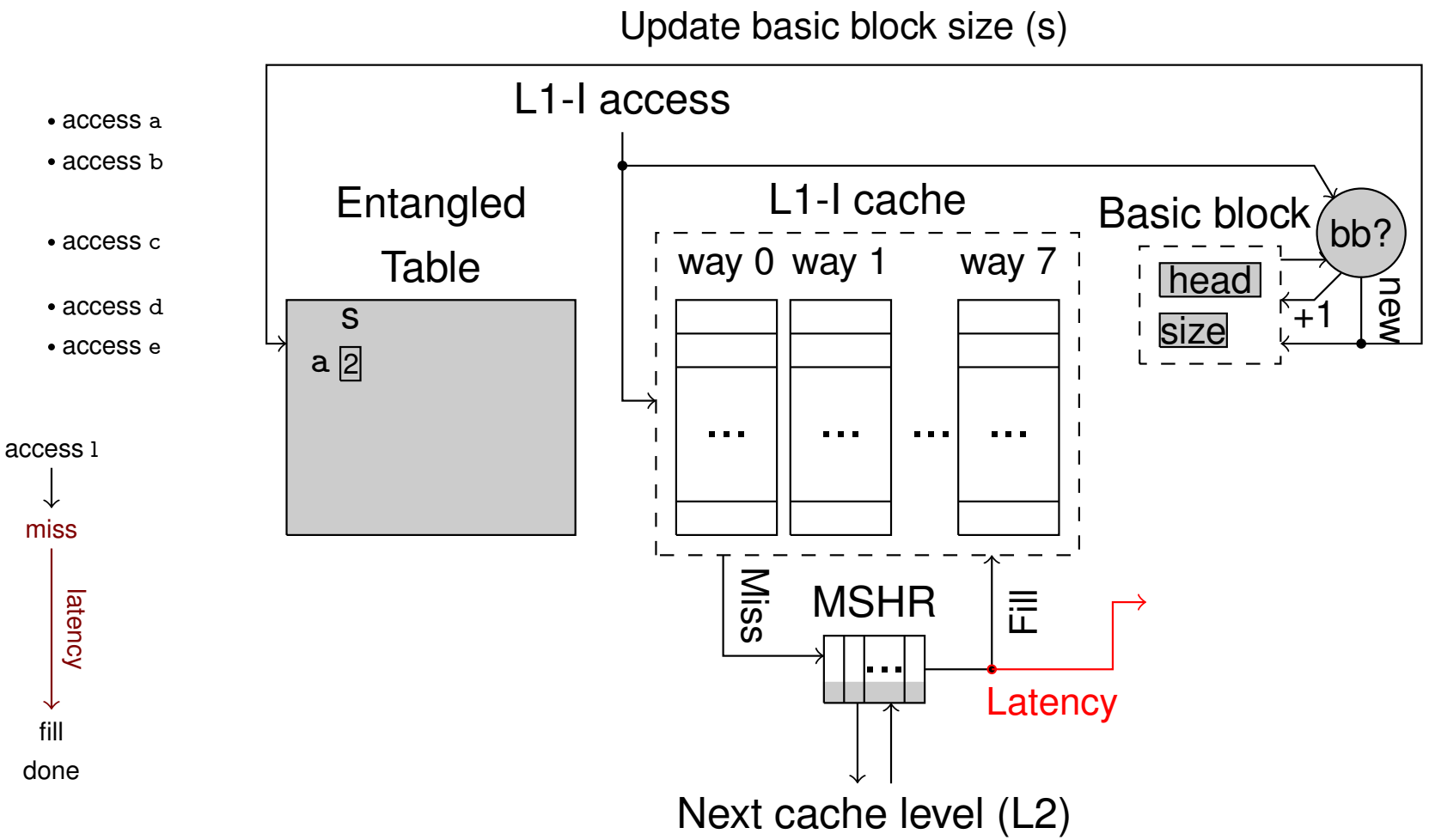

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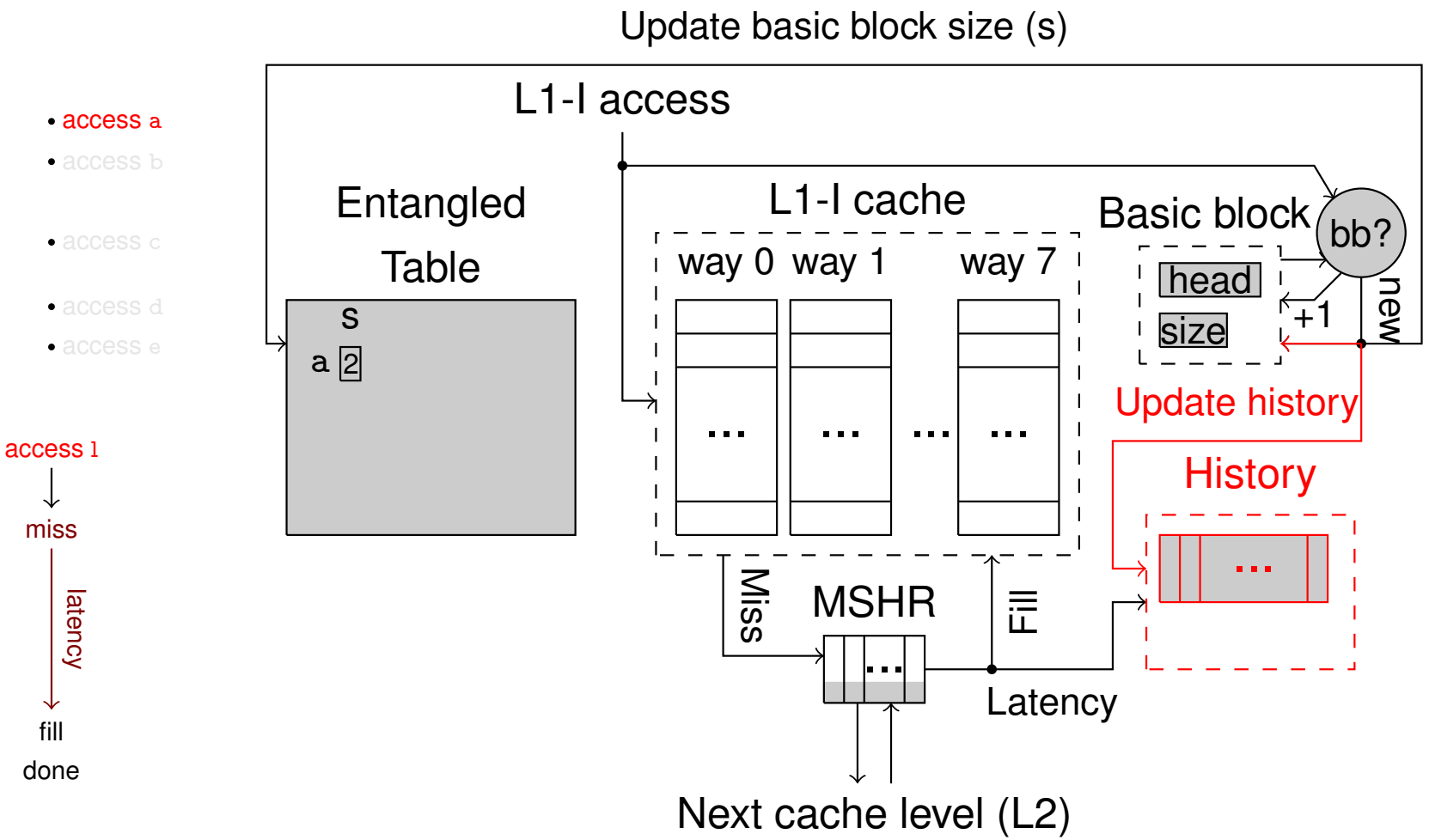

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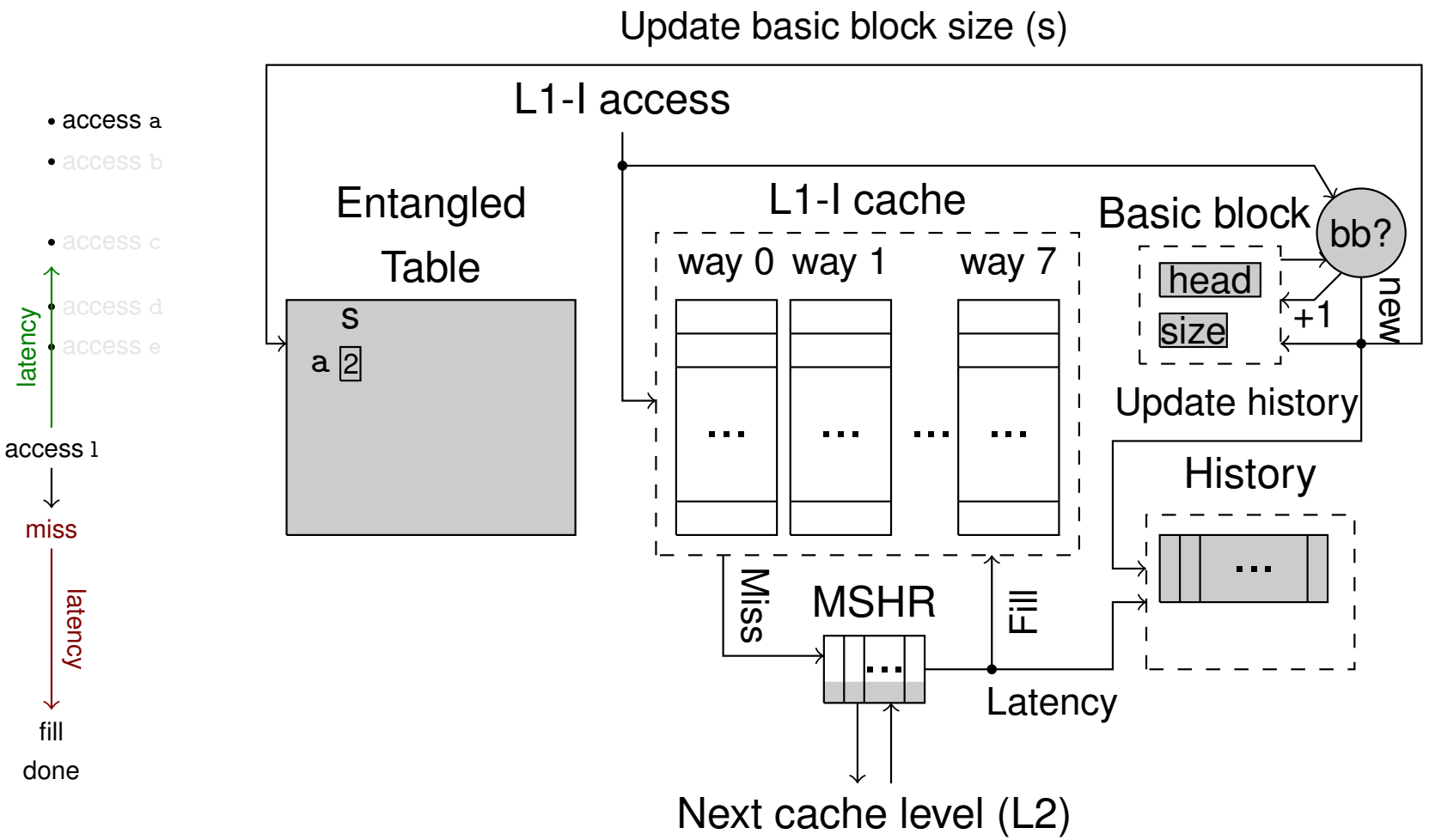
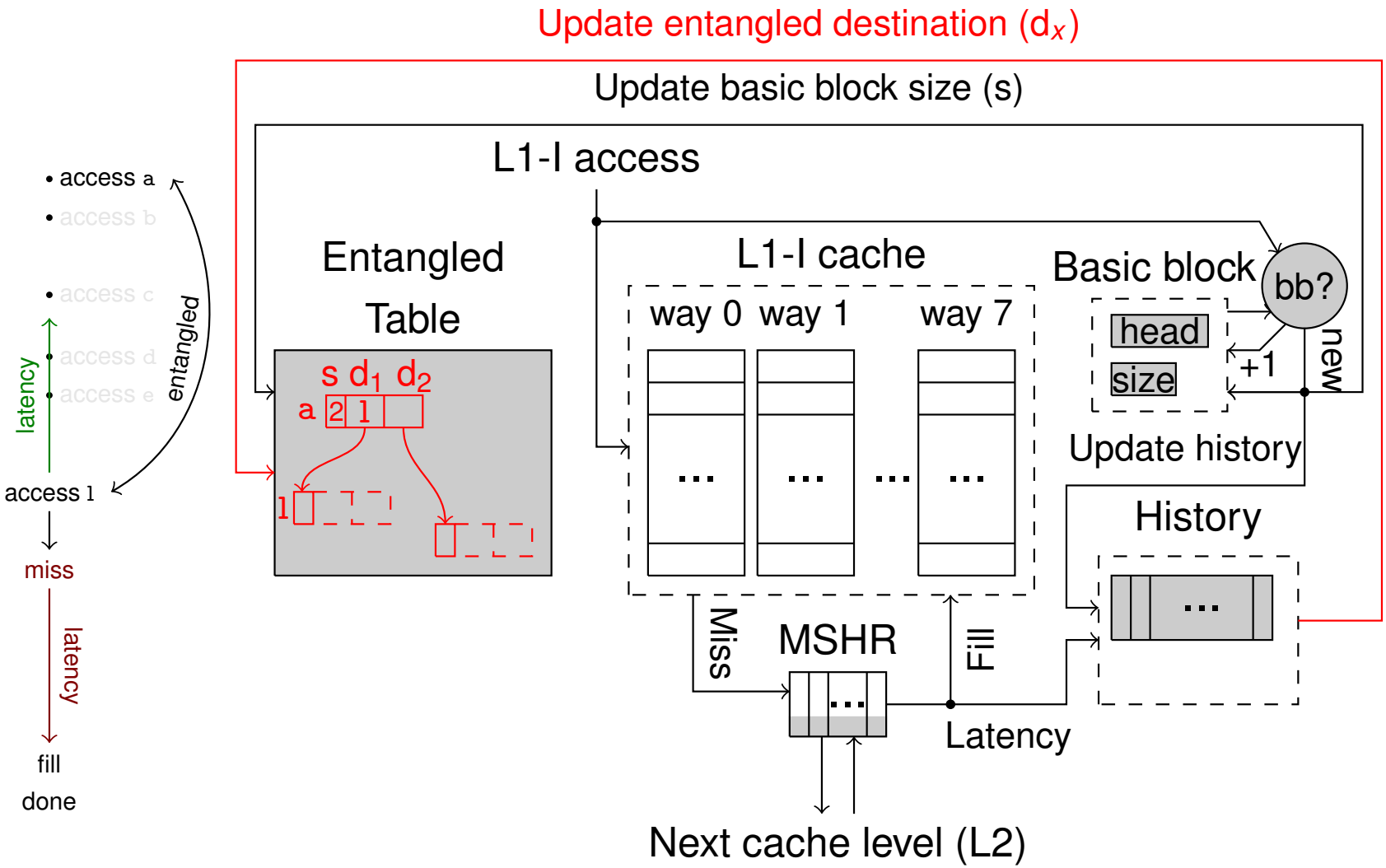
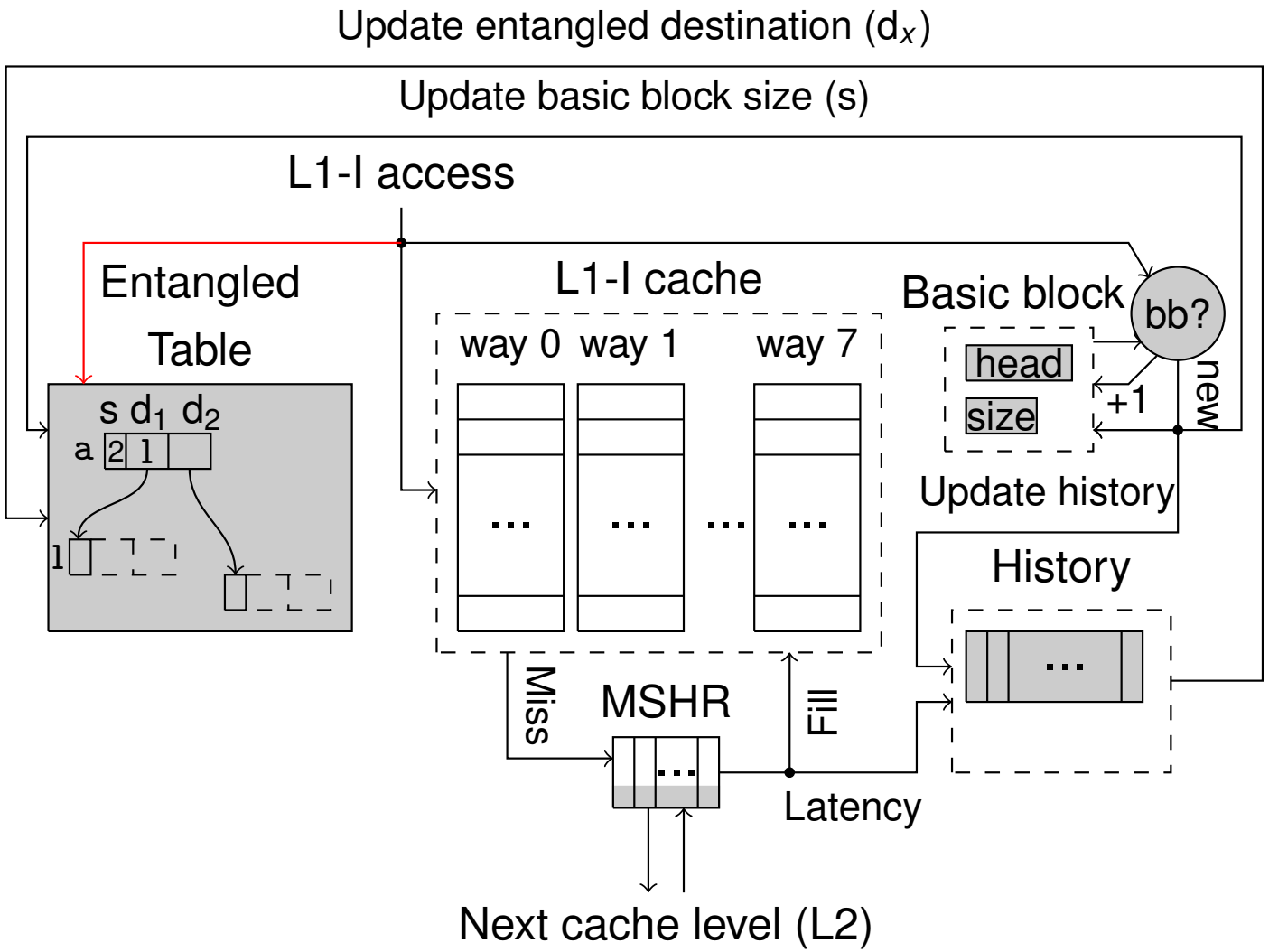


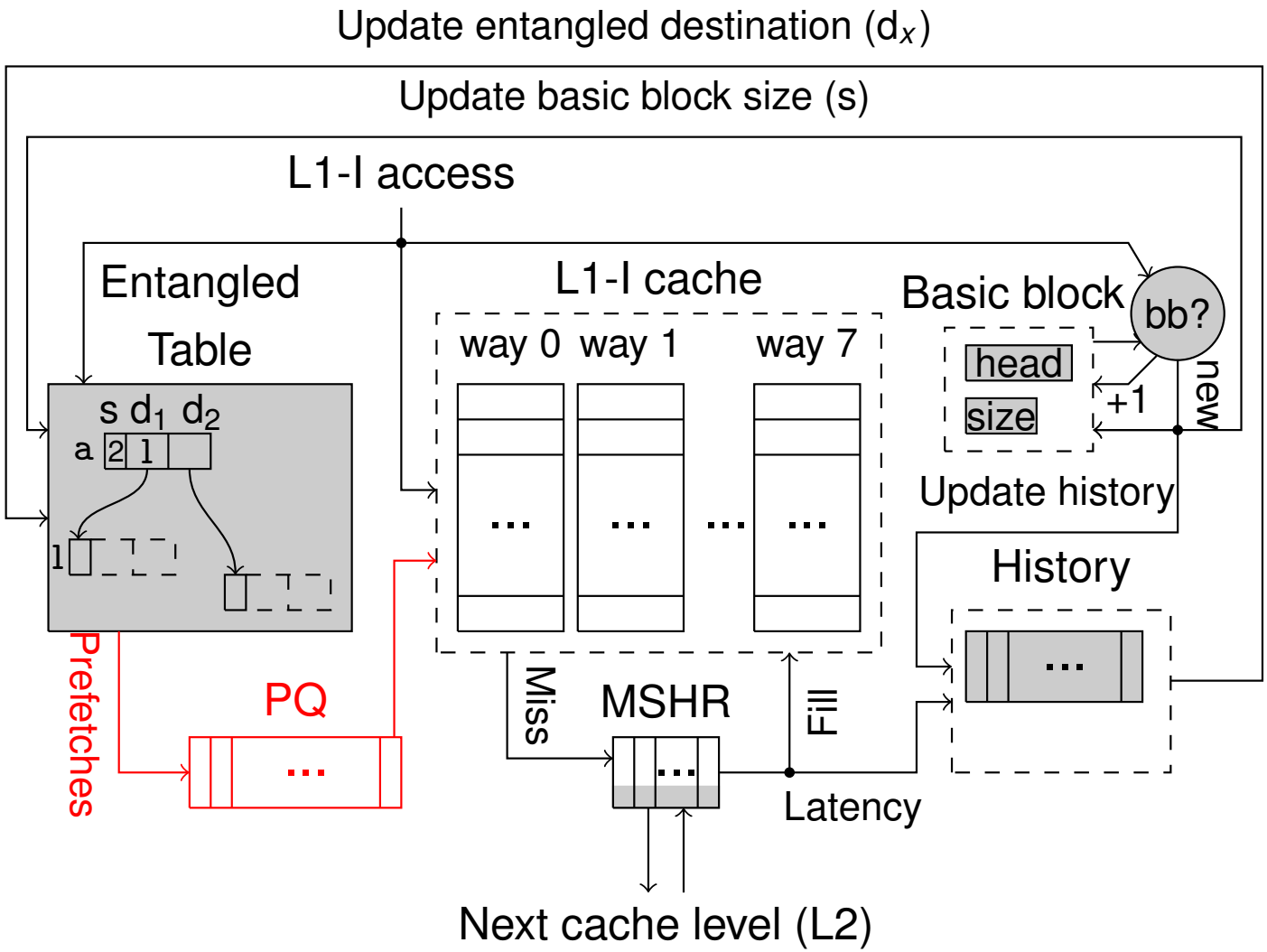
Design of the Entangling Prefetcher - Entangling cache lines



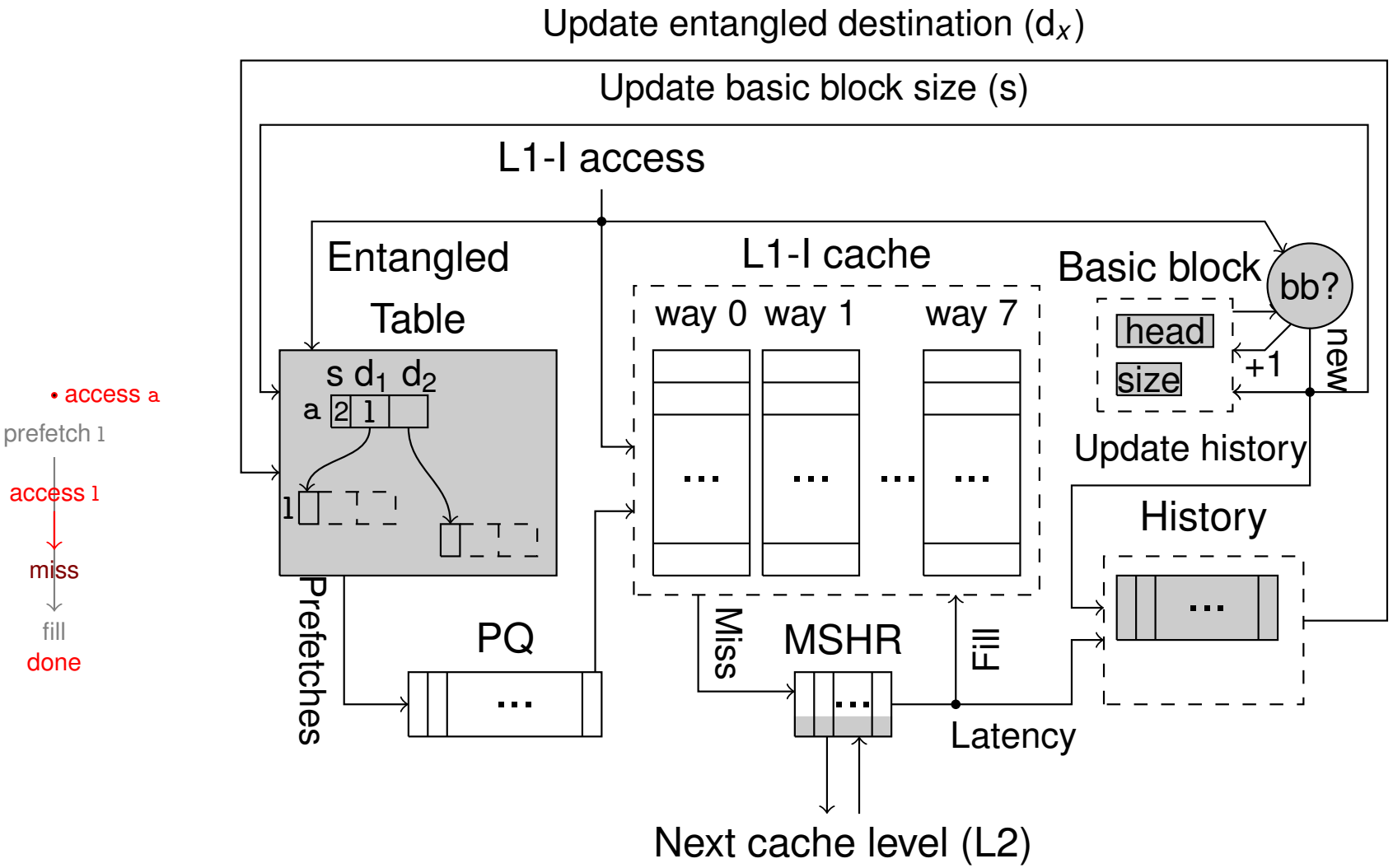
Design of the Entangling Prefetcher - Issuing prefetches



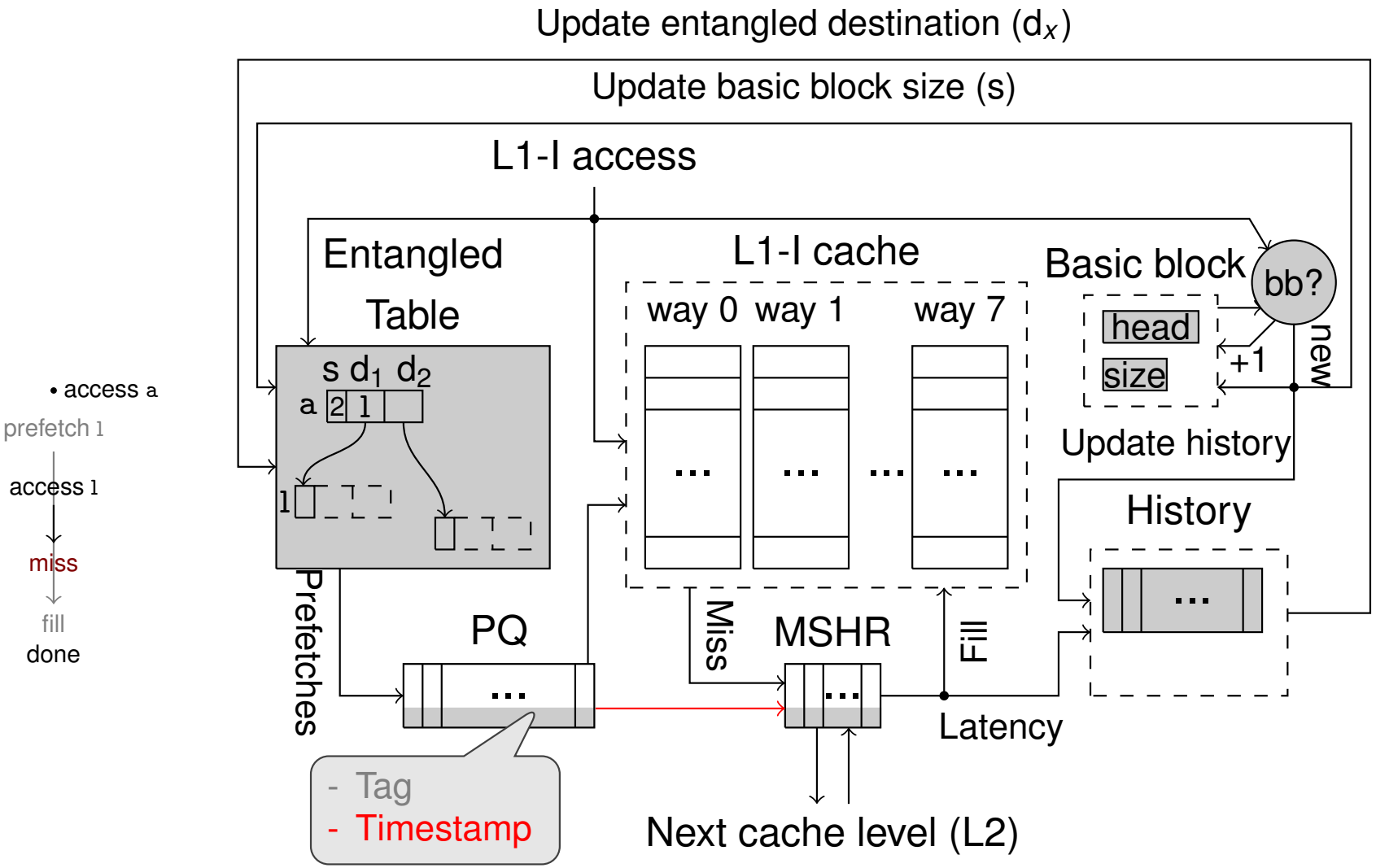
Design of the Entangling Prefetcher - Issuing prefetches



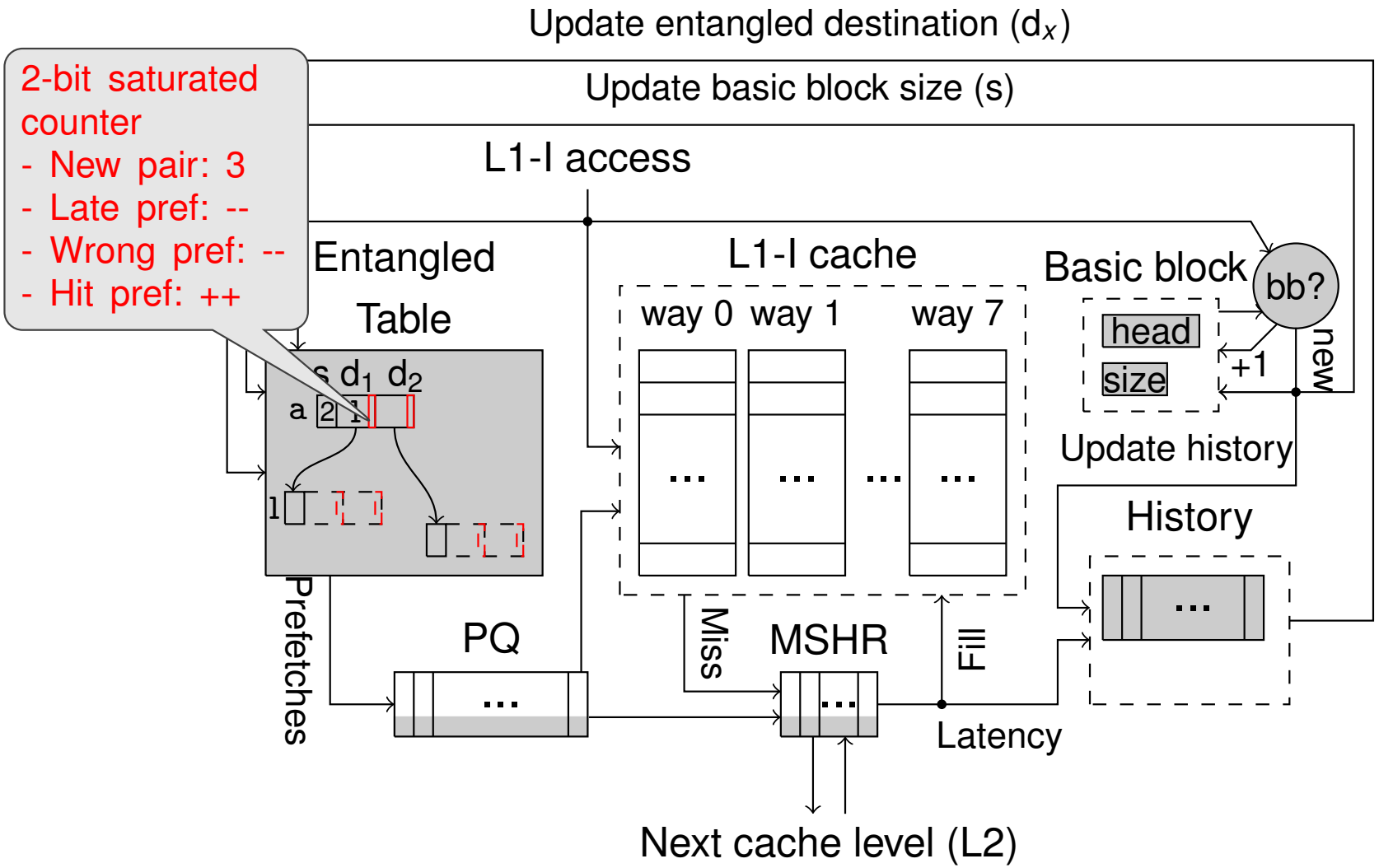
Design of the Entangling Prefetcher - Fixing Late Prefetches



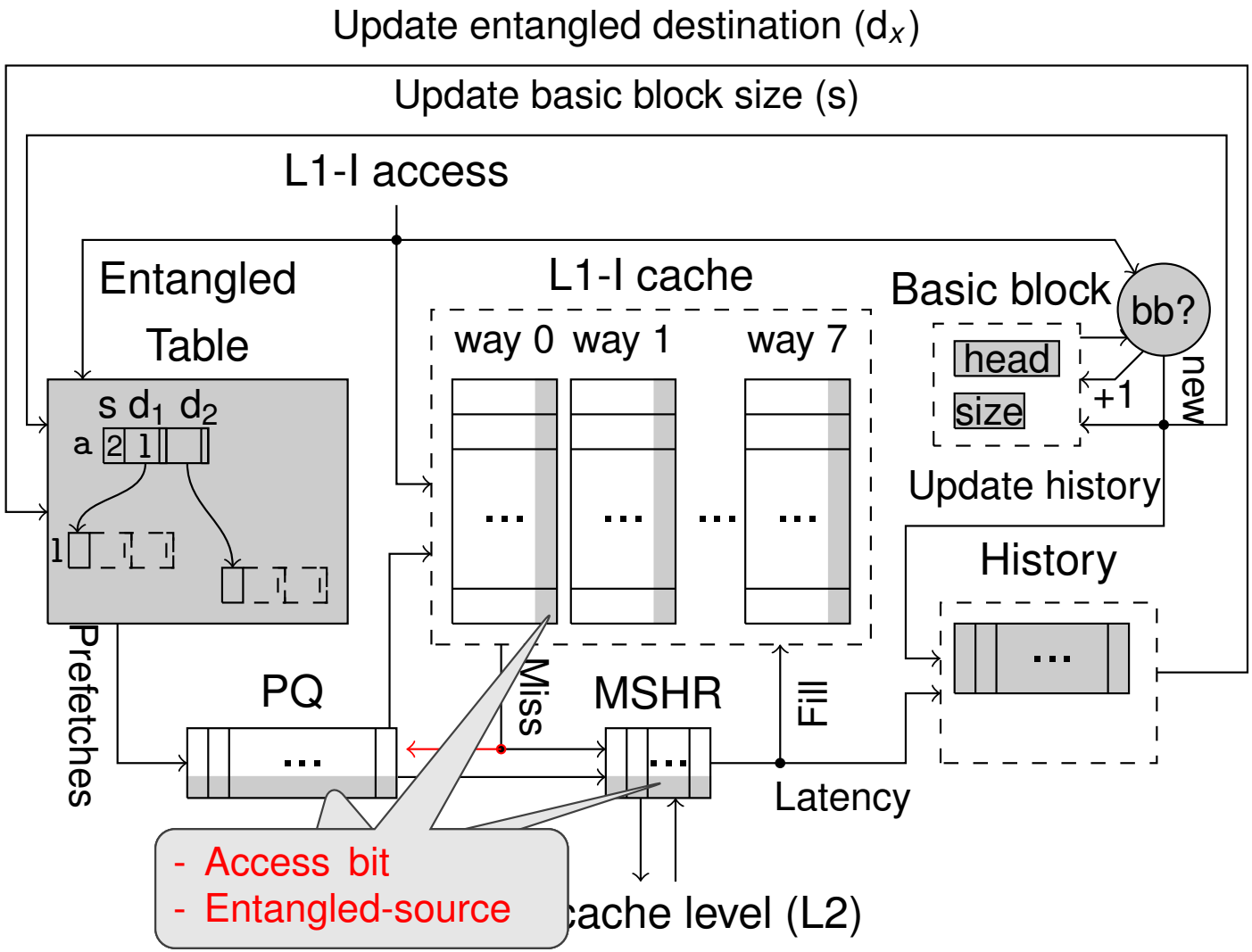
Design of the Entangling Prefetcher - Fixing late prefetches



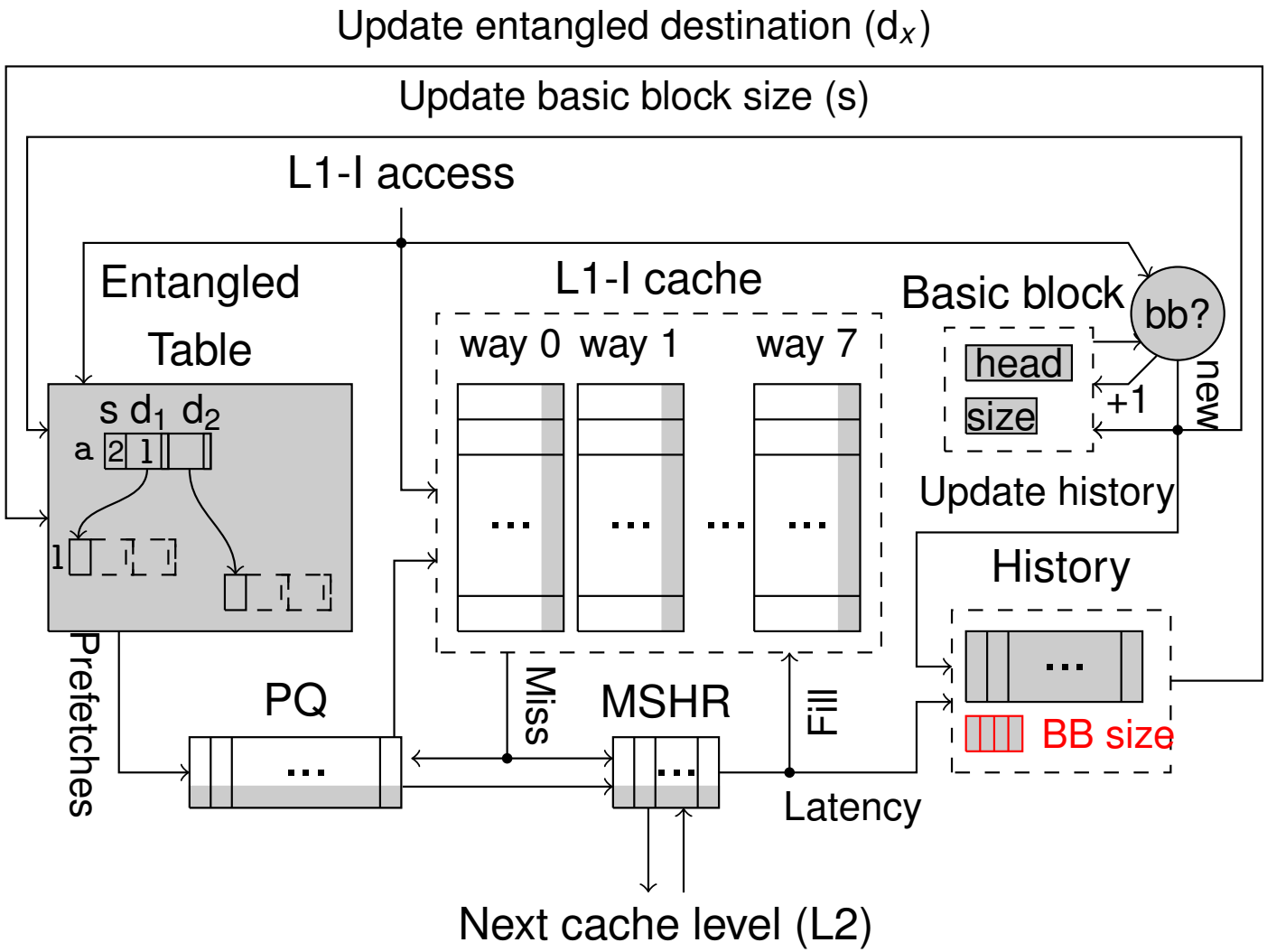
Design of the Entangling Prefetcher - Confidence for entangled pairs



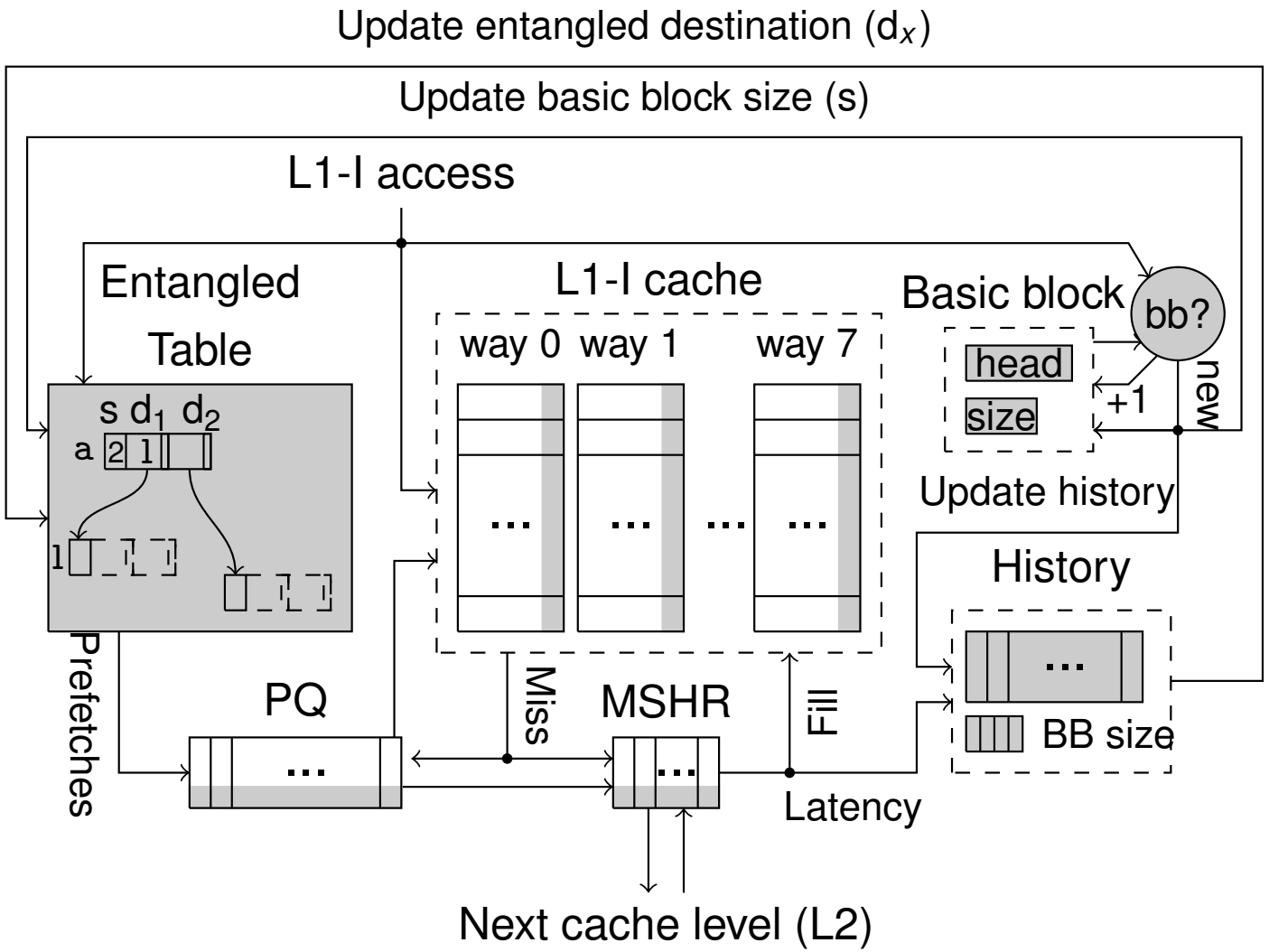
Design of the Entangling Prefetcher - Confidence for entangled pairs



Design of the Entangling Prefetcher - Merging Basic Blocks



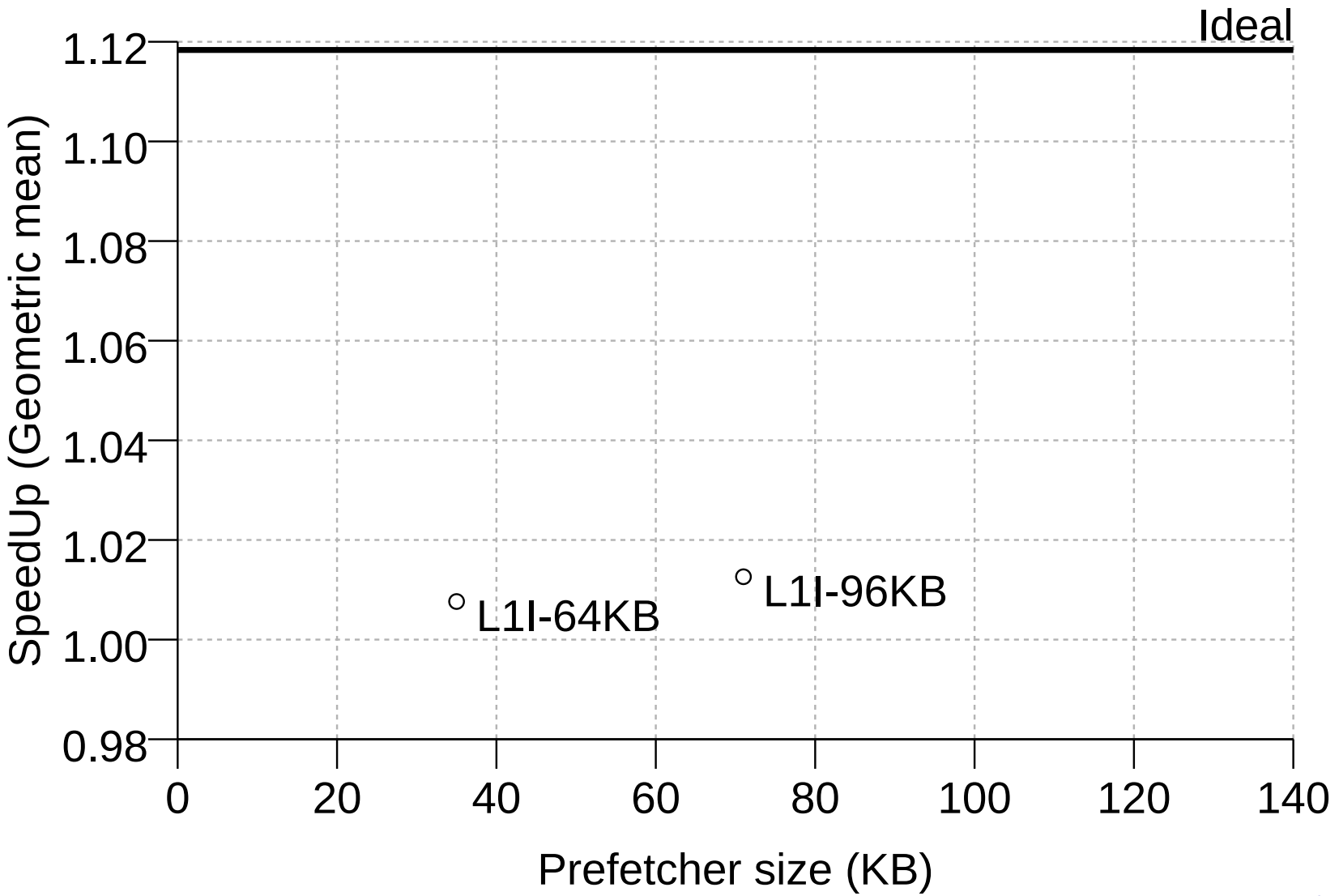
Design of the Entangling Prefetcher



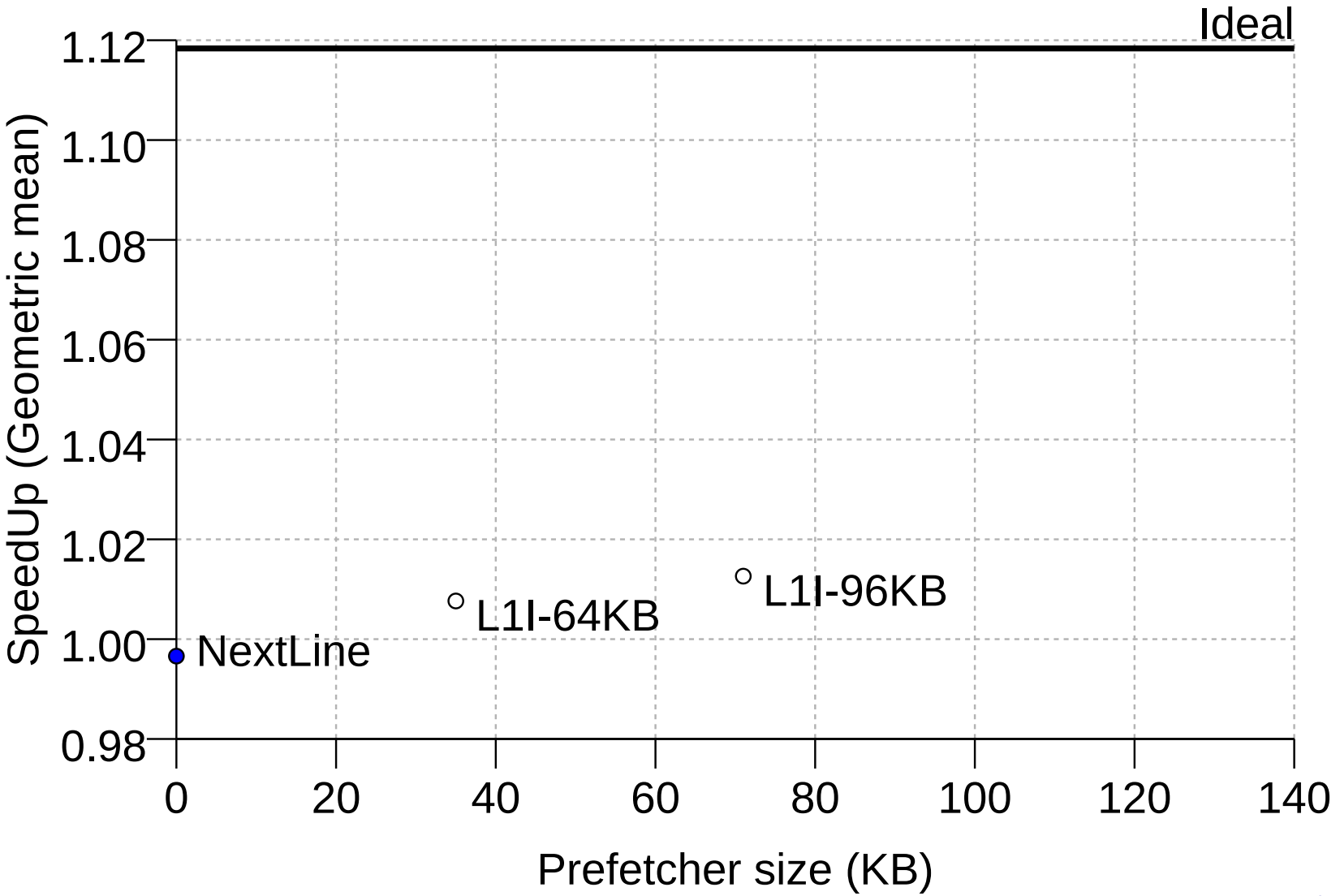
METHODOLOGY

- ChampSim develop branch (nov 2020)
- Baseline:
  - Sunny Cove-like system
  - Decoupled front-end (64-entry fetch queue)
  - 32KB L1I
- ENTANGLED:
  - *History buffer*: 16 entries
  - *Entangled table*: 2K, 4K and 8K entries
- Applications
  - 959 traces from the Championship Value Prediction (provided by Qualcomm)
  - Cloud Suite
- Analysis both for virtual and physical prefetching

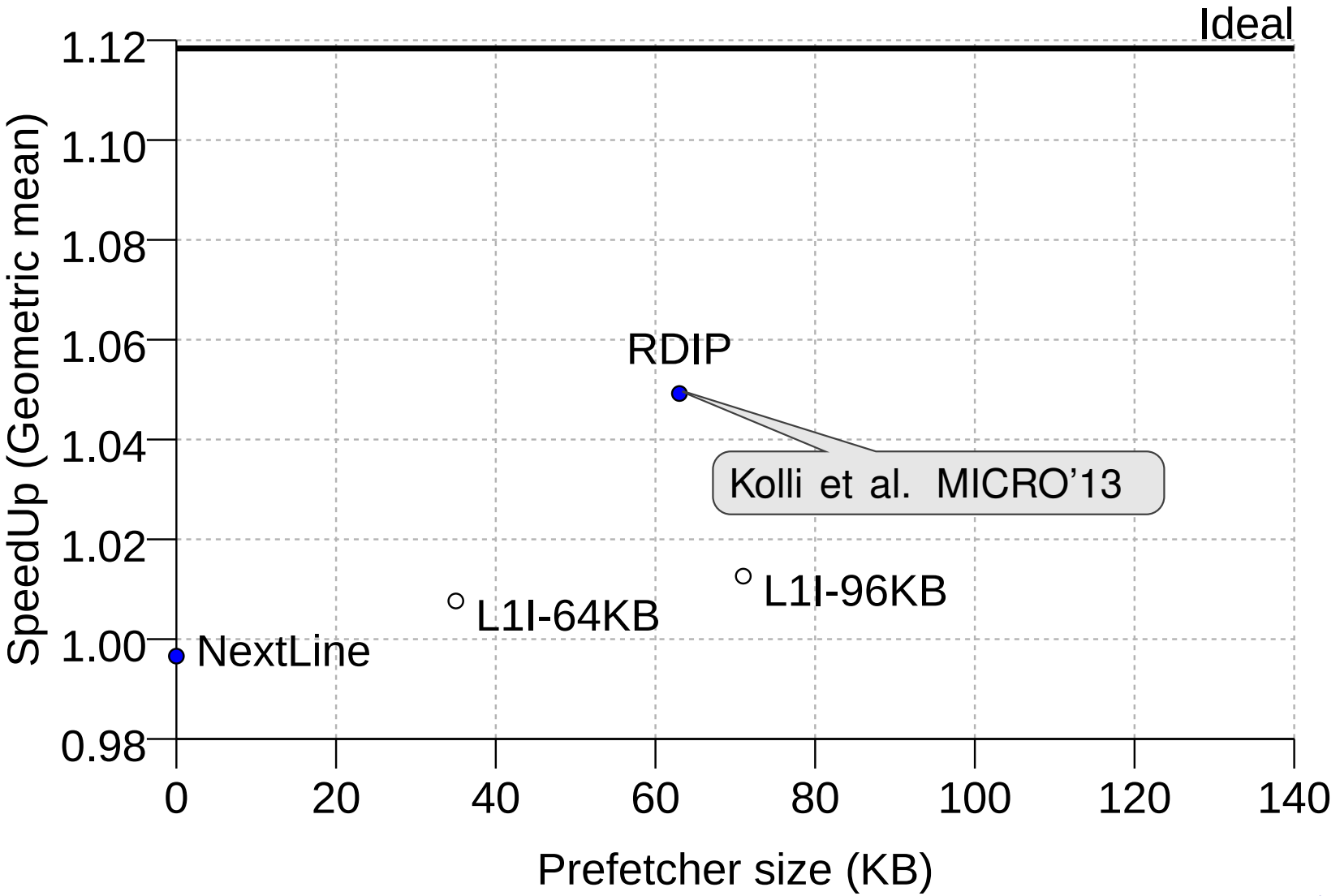
RESULTS: IPC VS MEMORY OVERHEAD



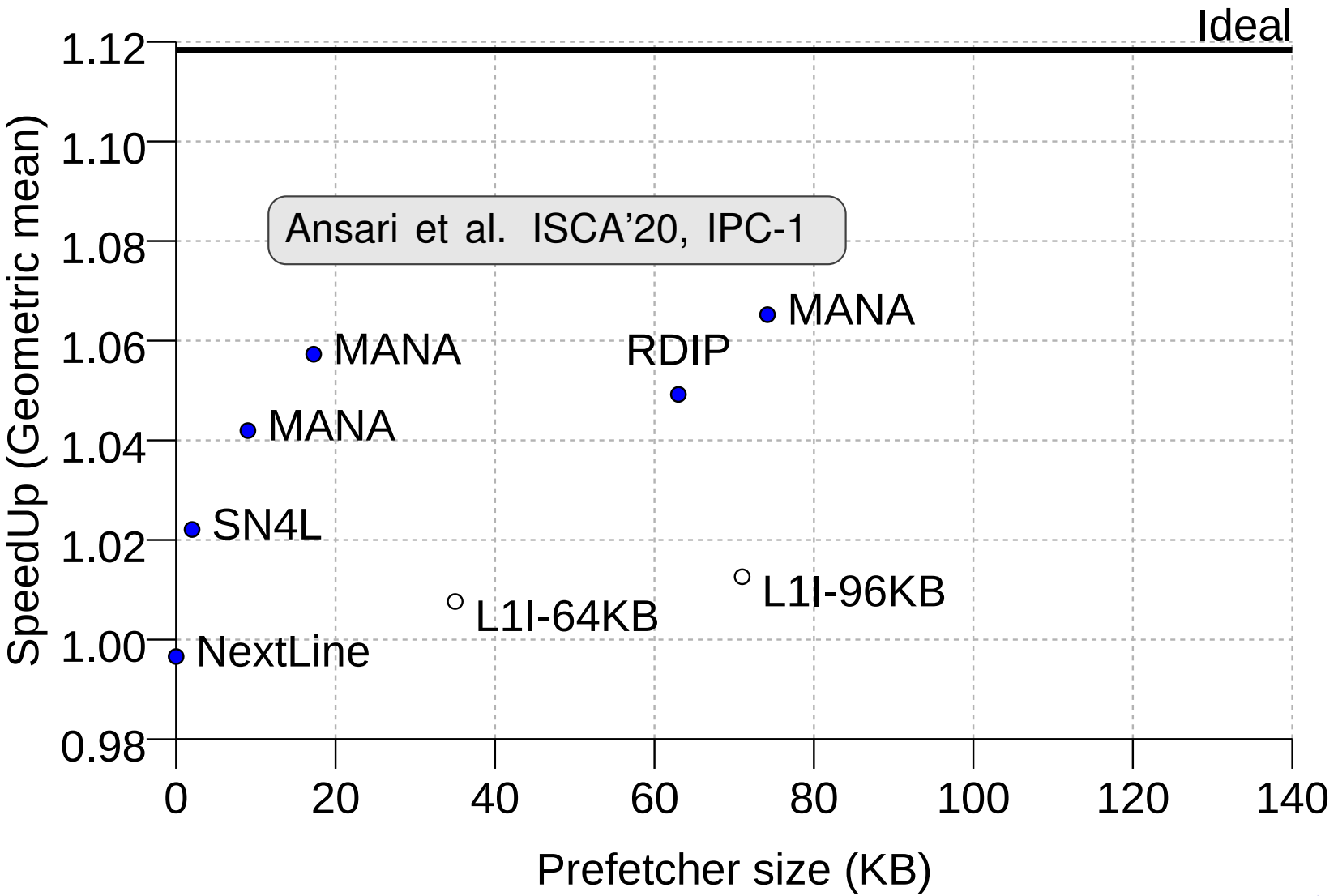
RESULTS: IPC VS MEMORY OVERHEAD



RESULTS: IPC VS MEMORY OVERHEAD



RESULTS: IPC VS MEMORY OVERHEAD



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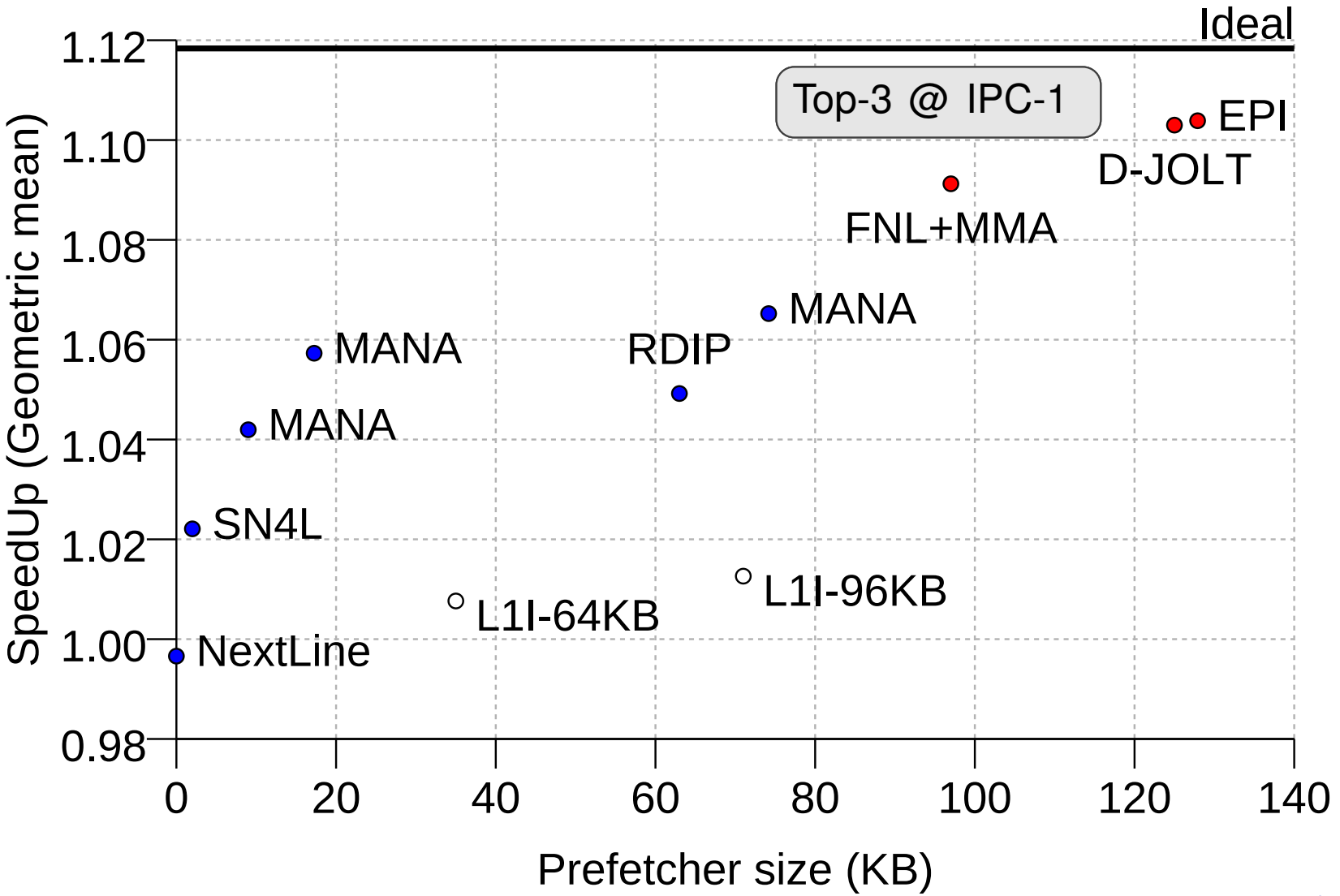
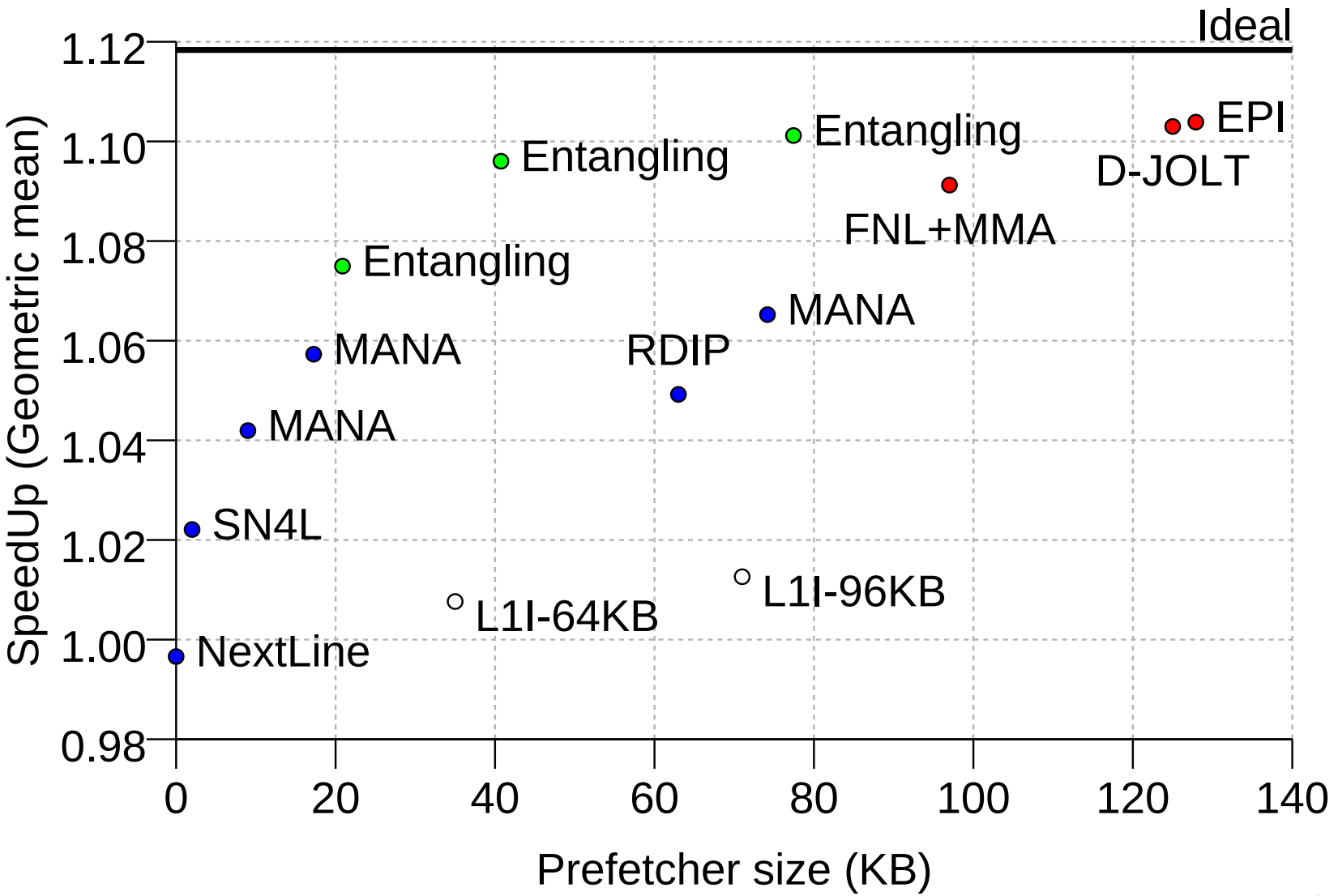
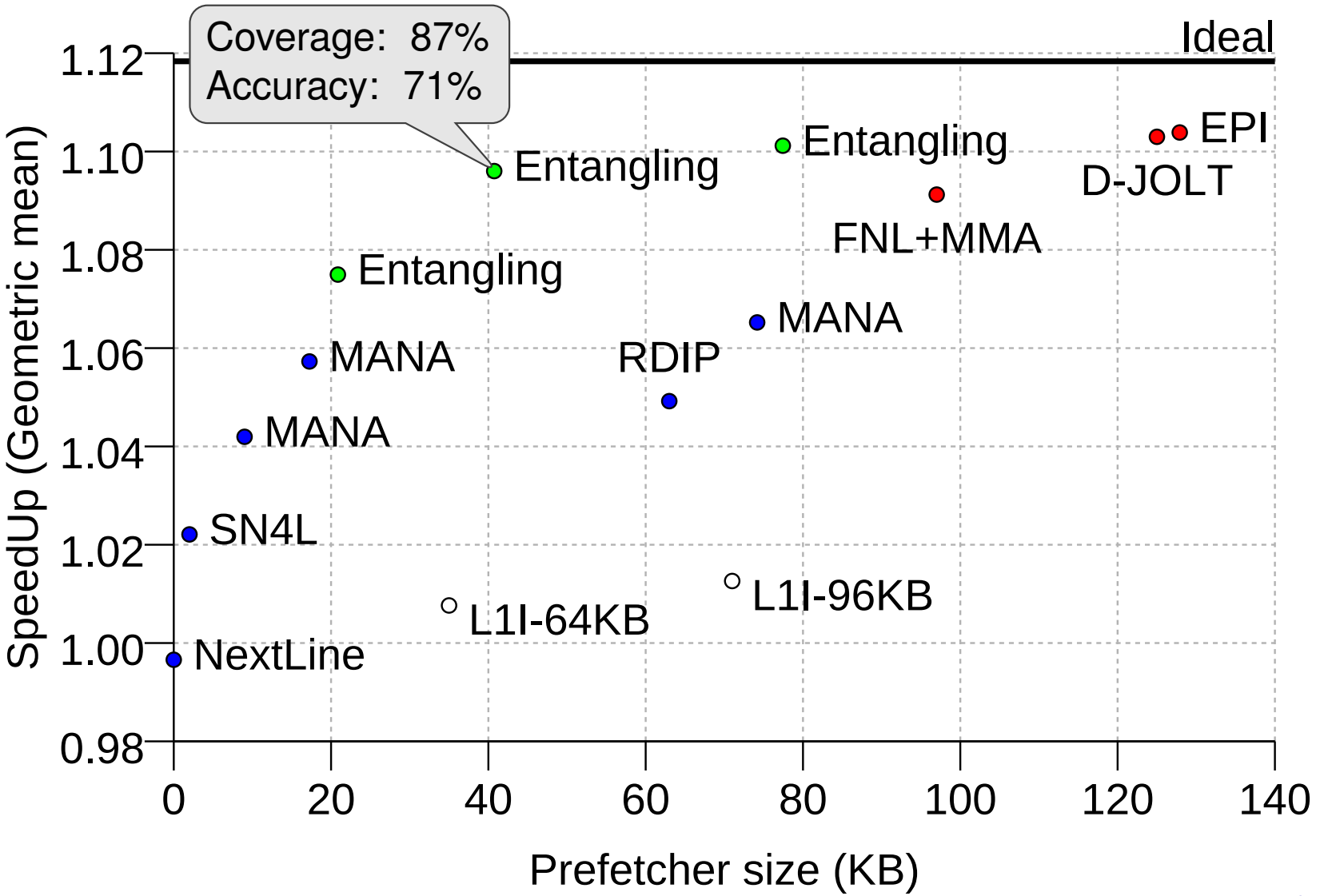


RESULTS: IPC VS MEMORY OVERHEAD



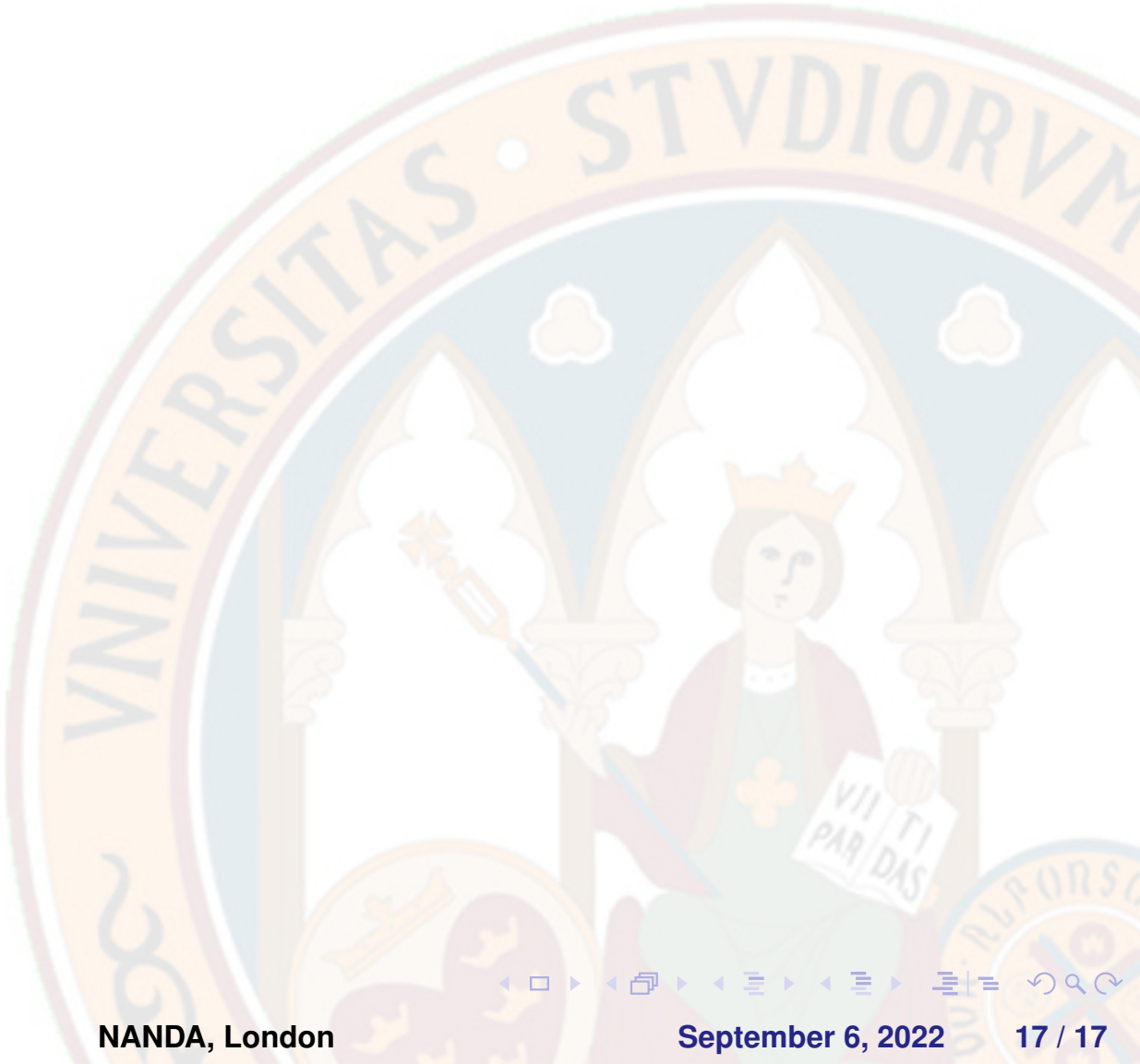
RESULTS: IPC VS MEMORY OVERHEAD



CONCLUDING REMARKS

- Data centers need good prefeteching techniques
- Timeliness as a key property for a prefetcher
- Entangle heads of basic blocks to trigger timely prefetches
- Near ideal L1I performance with just 40KB

Thank you!



THE ENTANGLING INSTRUCTION PREFETCHER

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September 6, 2022