Radiation and Temperature Effects on the APV25 Readout Chip for the CMS Tracker

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Abstract

The Compact Muon Solenoid (CMS) is one of four particle detectors designed for use at the Large Hadron Collider (LHC) currently under construction at CERN, the European Laboratory for Particle Physics in Geneva. The LHC will accelerate two counter-rotating beams of protons to energies of 7 TeV and produce 10^9 proton-proton collisions per second at a bunch-crossing frequency of 40 MHz. These collisions occuring at the centre of CMS will generate a very hostile radiation environment.

The CMS sub-detector system closest to the collision point is the highly segmented Tracker, consisting of a silicon pixel detector with 45 million channels and a silicon microstrip detector with 10 million channels. The microstrip detector will be read out by the APV25, a custom-made chip manufactured in a commercial 0.25 μm CMOS microelectronics process. Radiation and temperature studies are required to ensure that the APV25 can operate reliably in the CMS environment.

The radiation effects to which the APV25 could be susceptible are total dose effects and single event effects (SEE), such as single event upsets (SEU), single event gate ruptures (SEGR) and single event latchups (SEL). Approximately 75 000 chips will be used in CMS and confidence in total dose radiation tolerance will come from irradiating a subset of these chips to the radiation levels expected at CMS. For this purpose, a total dose radiation testing procedure was set up and the results obtained on a set of chips are presented, along with a detailed analysis of effects on discrete transistors. The need to periodically reset the chip during operation at CMS was determined from SEU tests. Along with transistor measurements, these also demonstrate immunity to SEGR and SEL.

The APV25 will be operated at –10 ^{o}C in CMS. Until recently, all testing of the chip was carried out at room temperature. An environmental chamber with a temperature range of 130^{o}C to –40^{o}C was used to investigate temperature effects on the APV25.

The measurements performed provide strong evidence that the APV25 will be fully functional throughout the lifetime of the CMS experiment. This is largely due to a combination of special design rules and intrinsic total dose radiation tolerance attributed to the thin gate oxide of the 0.25 μm CMOS process.

Acknowledgements

My stay in the HEP group is coming to an end and I am now slowly realising just how much I have benefited from working in it. I would like to thank Geoff Hall for his continuous support and for the trust he gave me throughout. Mark Raymond deserves a special mention for all the help he provided in every aspect of the work I undertook. His 'do it with a smile' approach will always be remembered.

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I would like to dedicate this thesis to my 'second family', Steve, Fiona, Michele, Dean and Aubrey Thomas, who supported me during my first year in Christchurch and to my mum, dad, Melena, Monti and two grans. I would like to thank Jane for her love, support and patience.

I have had a lot of fun working in the 'Silicon lab', and enjoying the occasional one down Finnegans with Barry, Greg, Jon, Emlyn, Rob and Mat. I wrote this section in a hurry as is probably customary and it therefore does not do justice to all the many great friends I have, from the early years in Cameroon right through to the present, via Bournemouth, Bath and Geneva. You all deserve a big thank you.

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Introduction

In the early part of the twentieth century, the period extending through to the mid-1930s, a few fundamental particles were known to physicists; the proton, neutron, electron, positron and photon. This picture was believed to be complete though a rather difficult question remained to be answered: how did multiple positively charged protons co-exist in a nucleus without being repelled by the electromagnetic force between them? The search for the answers to this question and the discovery of many new unstable particles in the 1940s mark the birth of the subject of modern particle physics. By the end of the twentieth century, this field of physics had made tremendous progress in understanding the fundamental constituents of matter and their interactions, leading particle physicists to the currently held view that matter consists of two fundamental groups of particles, quarks and leptons, distinguished by the interactions in which they take part.

Four types of interactions are known to exist: the strong, electromagnetic, weak and gravitational forces, mediated by force carriers called gauge bosons. The gravitational force, which is the most familiar in the observable world and which affects large bodies separated by large distances, is by far the weakest and is usually considered negligible in particle physics. At the 1 fm scale, the strongest interaction is the strong force, responsible for the interactions between quarks. The weak force is responsible for processes such as nuclear beta decay that are forbidden by the conservation rules constraining the much stronger electromagnetic and strong forces. Another fundamental feature of particle physics is the existence of antimatter. Every particle has a corresponding antiparticle whose mass and spin are the same but whose charge and subset of internal quantum numbers take the opposite sign.

The six known leptons are usually paired up into three generations, each containing a charged member and a neutral member. All leptons are subject to weak interactions and, in addition, the charged leptons can interact via the electromagnetic force.

Six types of quarks exist, namely the up, down, strange, charmed, bottom and top. These spin ½ particles are also grouped into three generations. One peculiar feature of quarks (antiquarks) is that they carry a fractional charge of $+2e/3$ ($-2e/3$) and $-1e/3$ ($+1e/3$). Free quarks have never been observed in nature and are thought to be confined in quark-composite particles collectively known as hadrons. Hadrons can be split into two subgroups, mesons, which consist of a quark-antiquark pair, and baryons, which consist of three quarks. Hadrons participate in strong interactions, a property that

distinguishes them from leptons. Some hadrons consisting of identical quarks with parallel spins would violate the Pauli exclusion principle. To solve this anomaly, it was proposed that quarks possess a new property called colour. The six quark flavours can each have three "colours". The strong force therefore has six charge states (the three colours and their corresponding anticolours), in contrast with the electromagnetic force which has two, + and −.

Quarks and leptons have spin ½ and are therefore fermions whereas the force carriers have integer spin and are bosons. The well known massless, chargeless photon mediates the electromagnetic interaction. The $W^{\pm}$ and Z bosons which have mass are responsible for carrying the weak interaction. Massless particles called gluons are the carriers of the strong force. For completeness, the gravitational force is thought to be mediated by gravitons.

Many theories have been developed to explain the plethora of observations made in particle physics. The quantum theory of electromagnetism is expressed in the theory of quantum electrodynamics (QED). The main features of QED are those of renormalisability and gauge invariance. The theory of the strong force is called quantum chromodynamics (QCD). Particle physicists ultimately believe that at very high energies, all four forces are the same. This has led to the development of further theories attempting to progressively unify the forces such as the electroweak theory, which essentially makes no distinction between electromagnetic and weak forces at very high energies. Other important theories are the Standard Model, and Supersymmetric models which predict the existence of a superpartner for every particle.

Interestingly, the electroweak theory is at the heart of one of the most controversial questions in particle physics today, that of the origin of particle masses. Whilst the photon has no mass, the $W^{\pm}$ and Z bosons do and this leads to the difference between electromagnetic and weak forces at low energies. The change in force properties from low to high energies is called symmetry breaking and can be explained within the framework of the electroweak theory by the existence of a particle called the Higgs boson, whose mass should be no more than 1 TeV.

The tools used by particle physicists in their quest for a better understanding of nature are accelerators and detectors. A new accelerator, the Large Hadron Collider (LHC), is currently under construction at the European Laboratory for Particle Physics (CERN) in Geneva, Switzerland. Four detectors will study the full range of physics made available by the high-energy collisions at the LHC. One of these is a general-purpose detector, called the Compact Muon Solenoid (CMS), which is constructed from a variety of

subdetector systems. Each sub-system performs a specific task, measuring one or more particle properties. For example, tracking detectors measure particle trajectories whilst calorimeters measure energy. Information from all systems is collected, analysed and used to identify particles and reconstruct events of interest.

At the LHC, two counter-rotating beams of protons will interact with a frequency of 40 MHz, generating up to 10^9 collisions per second. This rate, combined with the 14 TeV centre-of-mass collision energy will create a very hostile radiation environment. The CMS subdetector closest to the collision region is the Tracker, which must employ sophisticated on-detector readout electronics to condition signals from its silicon sensors, and to store and reduce the large amounts of data for an off-line analysis rate of 100 Hz. The survival against radiation effects of the readout electronics poses one of the many technological challenges of the CMS detector.

The Tracker is designed to provide position information and it achieves this by recording hits in several layers of silicon detectors, thus reconstructing the trajectory of particles. It is required to have high spatial resolution which leads to a large number of detector channels. In total, just under 10 million silicon microstrip channels will be read out by approximately 75 000 APV25 chips. These are Application Specific Integrated Circuits (ASICs) designed and manufactured in a commercial 0.25 μm CMOS (Complimentary Metal Oxide Semiconductor) process. It is the evaluation of the APV25, prompted by concerns over the use of a commercial CMOS process in a hostile radiation environment on such a large scale for the first time that forms the basis of this thesis.

Chapter 1 presents the basic functional principles of the LHC and CMS, and it also provides a discussion of the main features of the APV25. The building block of the APV25 is the Metal Oxide Semiconductor Field Effect Transistor (MOSFET). Chapter 2 presents an account of the operating principles of the MOSFET, followed by the various radiation effects it is susceptible to and the consequences of operation at low temperature. The encouraging progress made in the adoption of the 0.25 μm CMOS process for Tracker electronics has had a large impact on other sub-detector systems reviewed in Chapter 3.

Radiation testing results are presented in Chapters 4 and 5. The APV25 chips will be operated at −10 ^{o}C because of issues related to radiation damage in the silicon sensors. Chapter 6 presents results from low temperature studies conducted on the APV25.

Chapter 1

The LHC, CMS and the APV25 Readout Chip

A brief discussion of the LHC and CMS serves as a good starting point in understanding some of the challenges that the operation of the APV25 will present.

1.1 The Large Hadron Collider

The CERN council approved the LHC project in 1994 and, when completed, the LHC will be the most powerful particle accelerator in the world. To appreciate the scale of the LHC, it is useful to consider its predecessor at CERN, the Large Electron Positron (LEP) collider. The LEP ring was 27 km in circumference and the accelerator was designed to achieve centre-of-mass energies of 200 GeV. LEP revealed a few candidates for the Higgs boson, pointing to a possible mass of 114 GeV, before being decommissioned in 2000. LHC will explore physics beyond LEP by achieving centre-of-mass collisions with energies in the TeV range.

In circular accelerators, particles are constrained in a vacuum pipe with the help of electromagnets. The relation between the proton momentum p in GeV/c and the magnetic field B is

$$p = 0.3Br \qquad \text{..... eq. (1.1).}$$

where r is the ring radius in metres. At the LHC the ring radius is defined by the cost-effective approach of CERN requiring that the new accelerator be housed in the existing LEP tunnel, so the only parameter left to determine the maximum beam energy is B. The most advanced superconducting magnets with a maximum field of 8.33 T will be required to accelerate each proton beam to achieve collisions with centre-of-mass energies of 14 TeV.

The LHC bunch-crossing frequency is 40 MHz and it will start operating with a luminosity[1] of 10^{33} $cm^{-2}s^{-1}$, increasing to its full design luminosity of 10^{34} $cm^{-2}s^{-1}$ over a few years, and producing up to 10^9 proton-proton events per second.

The four detectors built to exploit LHC physics are optimised for various searches. Two general purpose detectors, CMS and ATLAS (A Toroidal LHC Apparatus) will identify and analyse the properties of the Higgs should it exist at LHC energies. A smaller

[1] Luminosity in circular accelerators is given by $L = fn\frac{N_1 N_2}{A}$, where N_1 and N_2 are the numbers of particles in each bunch, n is the number of bunches in either beam around the ring, A is the cross-sectional area of the beams and f is the revolution frequency.

detector, LHCb, is optimised for the study of charge-parity (CP) violation, a mechanism that, if it exists, could provide insight into the dominance of matter over antimatter in the present universe. In addition to proton-proton collisions, LHC is designed to collide heavy ions such as lead with total collision energies in excess of 1250 TeV. The ALICE (A Large Ion Collider Experiment) detector is optimised to explore the physics of the quark-gluon plasmas generated with these heavy ion collisions. The nominal luminosity of the LHC, 10^{34} $cm^{-2}s^{-1}$, combined with the 7 TeV beam energy will create an extremely hostile radiation environment.

1.2 The Compact Muon Solenoid

Although CMS [1] is optimised to detect the Higgs boson, it is actually a general-purpose detector, designed to identify and precisely measure muons, electrons and photons over a large energy range and at high luminosity. In addition to searches for the Standard Model Higgs boson mentioned previously, CMS will address topics such as searches for the various Minimum Supersymmetric Standard Model (MSSM) Higgs bosons, gluino and squarks searches, CP-violation measurements in the B sector, observations of B_s^0 oscillations, and possible signals for QCD deconfinement in heavy ion collisions.

The position, arrival time, and identity of particles are properties that all have to be determined by particle detectors, usually with a combination of sub-detector systems. Detection principles have remained the same over the past couple of decades and if one is searching for fundamental departures from old detector technologies, it is to be found in the adoption of increasingly complex electronics and computing systems. In this respect, CMS is typical of the new generation of particle detectors.

The CMS design is based around its 4 T solenoid magnet. Its strong field increases bending of charged particle tracks, thus enabling the determination of their momentum within a relatively small detector volume, hence the “compact” in CMS. In comparison, ATLAS is eight times the volume of CMS, but only half its mass.

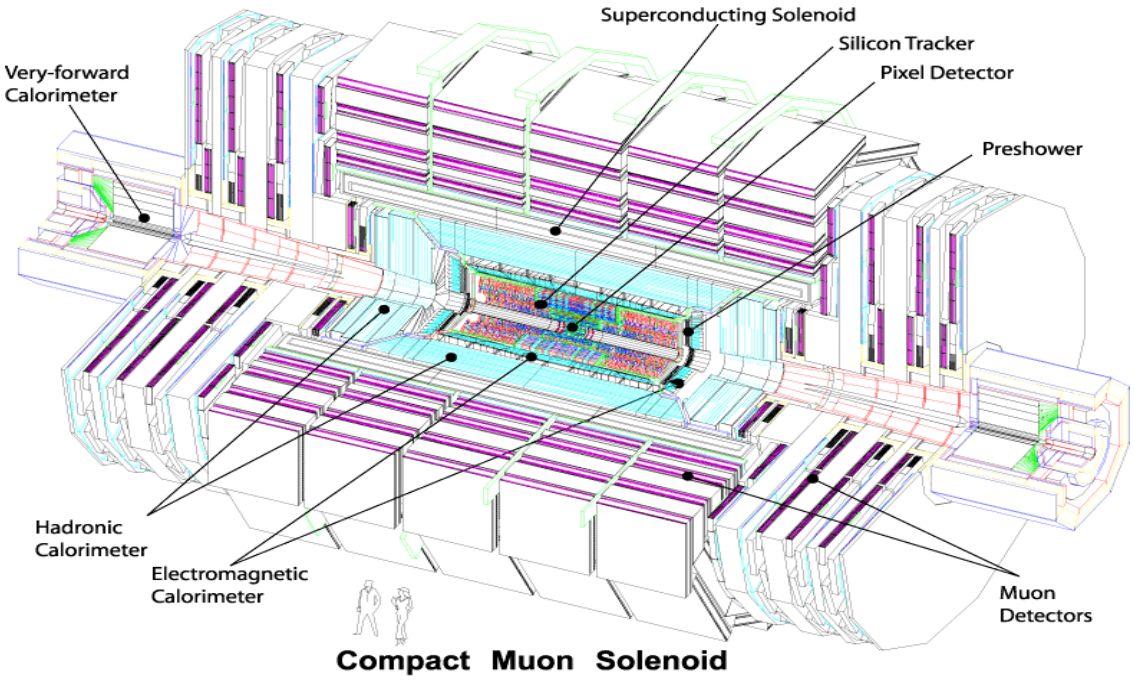


Figure 1.1: CMS and its subdetectors.

The detector sub-system closest to the collision point is the Tracker, which is followed by the electromagnetic calorimeter (ECAL), the hadronic calorimeter (HCAL) and the Muon detector, Fig. 1.1. These four main sub-detector systems consist of central sections, sometimes referred to as barrel regions, and sections at both ends of the solenoid, the endcaps. The solenoid itself has a length of 13 m and its inner radius of 2.95 m allows the full barrel calorimetry and Tracker to be located within it. The muon chambers lie outside the solenoid.

1.3 The CMS Tracker

The central tracking system [2] will play a major role in all physics searches. Its aims are to reconstruct muon tracks with an efficiency better than 98 % over the full pseudorapidity[2] range $|\eta| < 2.6$; charged hadron tracks (whose transverse momentum is above 10 GeV/c) with an efficiency of 95 %; and high-energy electron tracks with an efficiency of 90 %.

1.3.1 Tracker Layout

The Tracker will use two detector technologies, silicon pixel and silicon microstrip detectors, covering a total area of ~ 220 m^2. The layout outlined here is the result of

[2] Pseudorapidity is a measure of the angle from the interaction point and is given by $\eta = -\ln\left(\tan\left(\theta/2\right)\right)$ and $\frac{r}{z} = \tan\theta$. θ = 90° is perpendicular to and θ = 0° is parallel to the z-axis (beam axis).

intensive simulations taking into account requirements for track reconstruction and constraints such as material budget and cost, Fig. 1.2.

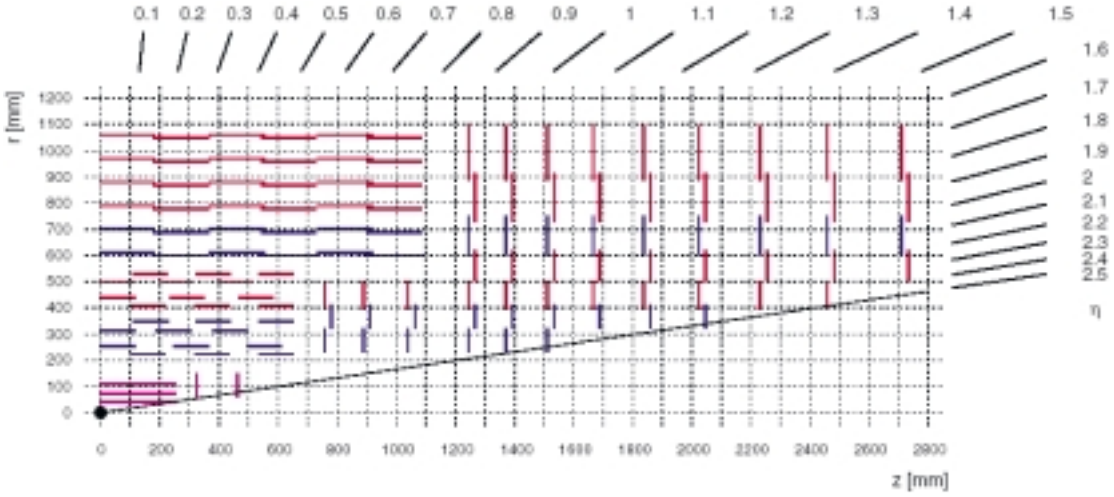


Figure 1.2: Schematic diagram of one quadrant of the CMS Tracker.

The origin denotes the interaction point and the numbers on the top and right give the angle in units of η. Closest to the interaction point, the three horizontal layers and two vertical lines denote pixel detector layers. All other layers are silicon microstrip layers [3].

The region closest to the interaction point is instrumented with silicon pixel detectors offering a position resolution of 10 → 15 μm. The pixel detector system is composed of modules of pixelated sensor plates with integrated readout chips connected to them using the bump bonding technique. Due to the high radiation levels, pixel detectors within 10 cm of the interaction point cannot survive over the lifetime of CMS and will have to be replaced. For this reason, the pixel barrel system will be installed in two stages. At low luminosity, two layers will be installed, one at 4.3 cm and the other at 7.2 cm. At high luminosity, the layer at 4.3 cm will be removed and another will be placed at 11.0 cm. The two endcap disks are located at a mean distance to the interaction point of 32.5 cm and 46.5 cm. In the high luminosity configuration, the pixel detector will have an active surface of close to one square metre, instrumented with approximately 45×10^6 channels.

The pixel detector is surrounded by a silicon microstrip detector, known as the silicon strip tracker (SST), consisting of ten barrel layers (from 22 cm up to 120 cm) and twelve endcap disks on either side of the barrel. These layers are numbered from the interaction point outwards.

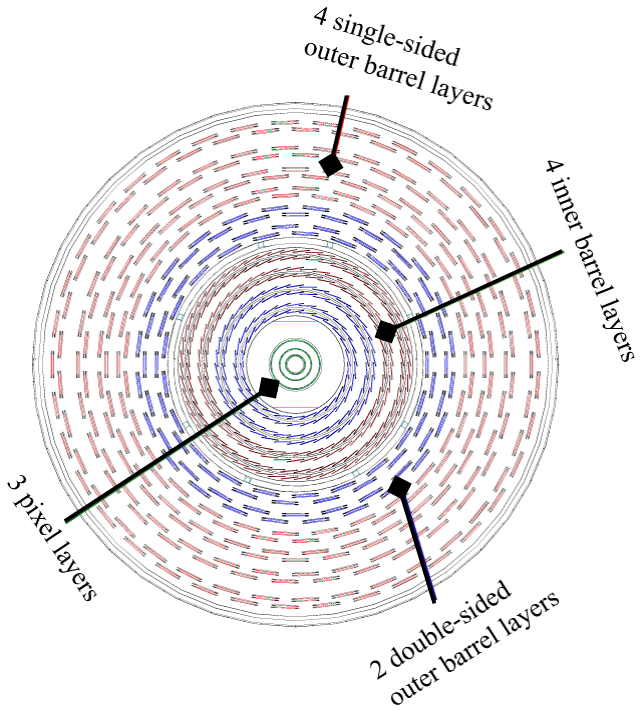


Figure 1.3: Cross-section of the CMS Tracker detector system in the barrel region.

Fig. 1.3 is a cross-section of the Tracker barrel, showing the SST to be composed of single-sided and double-sided layers. The double-sided layers are made of two single-sided sensors mounted back to back, one tilted by an angle of 100 mrad with respect to the other which effectively gives two-dimensional hit positions. The Tracker barrel region consists of four SST inner barrel layers (TIB) followed by six outer barrel layers (TOB). The first two layers of both the TIB and TOB are double-sided.

The endcap system consists of three inner endcap disks (TID) and nine outer endcap disks (TEC) on either side of the barrel.

The distinction between inner and outer regions is not made simply on the grounds of position. Due to the need to optimise the combination of three parameters, depletion voltage (explained in Chapter 2), signal-to-noise ratio and radiation tolerance, the sensors used in the two sections are actually different. The depletion voltage scales with thickness squared and inverse resistivity, but low-resistivity sensors are more radiation tolerant. In the inner section where the radiation levels are higher, the detectors are made of 320 μm-thick low-resistivity sensors. Sensors in the outer regions are 500 μm in thickness to compensate for the higher noise due to higher capacitance in their longer strips. Experimental measurements have determined that operating the detectors at high voltage in a –10 ^{o}C dry environment will limit the extent of radiation damage to the sensors.

1.3.2 Tracker Radiation Environment

The radiation field within the Tracker is characterised by two distinct sources. Firstly, secondaries from the p-p interactions, the product of their interactions in the Tracker structures and some decay products, give the dominating contribution to the fluences at the inner layers of the Tracker. This component of the fluence is almost independent of the z-coordinate and behaves roughly as $1/r^2$, where r is the distance from the beam-line. Almost all of the charged hadron fluence originates from the vertex. Secondly, a significant component of the neutron fluence is due to albedo from the surrounding electromagnetic calorimeter. The most intense source of albedo neutrons is the end-cap ECAL. While the fluence originating from the vertex is irreducible, a polyethelene moderator inserted in the bottom structure of the ECAL is shown to efficiently reduce the neutron fluence by a factor of 2.5. The radiation environment over a period of 10 years is presented separately for total dose (1 Gy = 100 rad), neutrons and charged hadrons, Fig. 1.4. To put into perspective the radiation hardness requirements of Tracker electronics, the total dose radiation environment is up to four orders of magnitude higher than the levels at which modern commercial components usually fail ($5 \rightarrow 20$ krad).

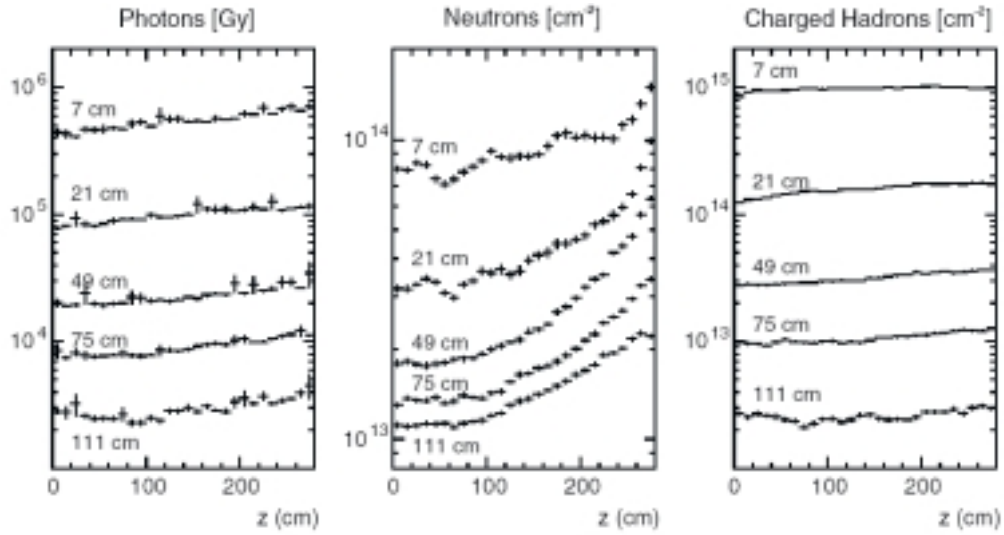


Figure 1.4: Radiation levels at selected radii in the CMS Tracker region. All values correspond to 10 years of operation.

1.3.3 Strip Tracker Electronics

The electronics system for the SST must fulfil the formidable requirements, in terms of particle fluences, magnetic field, material budget and inaccessibility, imposed by the environment in which it will operate whilst being capable of functioning at the level 1 trigger rate of 100 kHz. It is based on a uni-directional analogue readout chain and a bi-

directional digital control chain. Both chains consist of components located in close proximity to the silicon sensors, connected by optical fibres to components housed 100 m away in the experimental barracks. A Timing, Trigger and Control (TTC) system common to all LHC experiments provides clock and trigger information, ensuring the necessary level of synchronicity with the accelerator clock. The SST electronics system is described in more detail in Chapter 3 with an emphasis on radiation tolerance.

1.4 The APV Readout Chip

Imperial College London and the Rutherford Appleton Laboratory (RAL) are responsible for developing the silicon microstrip detector readout chip, the APV (Analogue Pipeline Voltage mode). The APV chips will sample, amplify and store signals from their corresponding microstrip detectors.

In addition to radiation tolerance, the APV has to fulfil the important requirements of low noise and low power driven by the need to discriminate significant signals from the background and to keep the material budget (and consequently the cooling system) at a minimum.

Since its conception in 1993, several versions of the APV chip have been built using different process technologies. Earlier versions such as the APV6 [4] and the APVD [5] were designed and manufactured in qualified radiation hard processes (1.2 μm Harris AVLSIRA process and 0.8 μm TEMIC DMILL process respectively). However, a decrease in defence-related systems acquisitions led to a dramatic drop in the number of radiation-hardened CMOS microcircuit fabrication lines [6]. This in turn led to an increasing disparity in performance, availability, and price of radiation-hardened parts compared to commercial CMOS microelectronics parts. In addition, the long turnaround time from design to production added pressure to the tight schedule for construction of the detector. Attention began to turn to commercial sub-micron technologies in 1997. The interest in these technologies comes from their excellent performance in terms of speed, density and noise, from potentially large cost savings and from increased radiation tolerance compared to their predecessors [7]. The final version of the chip, the APV25 [8], uses a 0.25 μm commercial process. Although no steps are taken in the fabrication process to harden the APV25 chip, it is radiation tolerant by its nature (the oxide layers are very thin) and by design (the chip features p^+ guardrings and enclosed transistor geometries to suppress leakage current paths) [9]. These properties and design features are discussed in more detail in Chapter 2.

1.4.1 The APV25 Analogue Chain

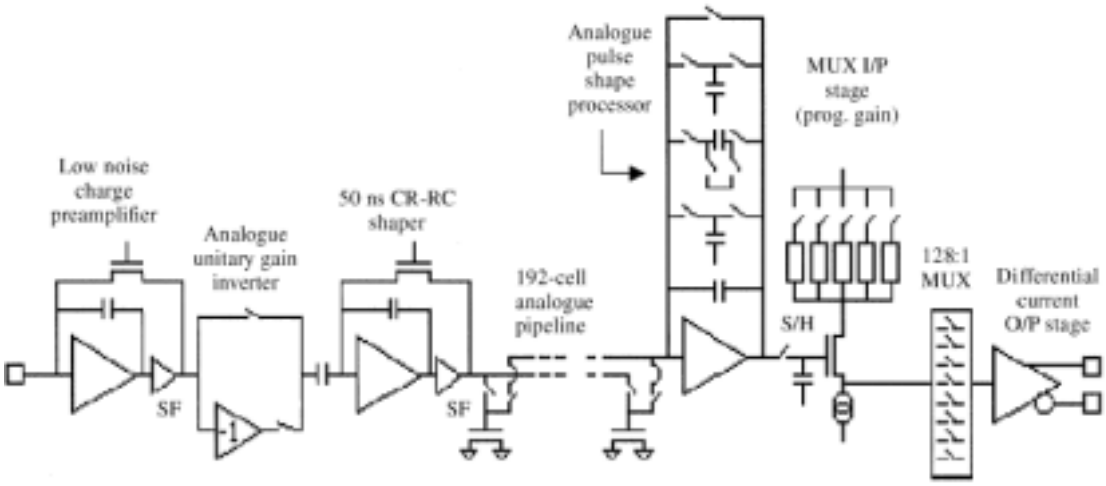


Figure 1.5: Block diagram of the APV25 analogue chain, from [10].
Each of the 128 channels has its own chain from preamp to multiplexer (MUX) stage.

The APV25 analogue block consists of 128 channels, each of which is designed to be bonded on the front side of the chip to a silicon microstrip. The signal from such a strip is first amplified by an integrating preamplifier, then passed through an inverter which can be optionally switched on or off before being shaped by a CR-RC shaper with a 50 ns peaking time, Fig. 1.5. Every 25 ns the shaper output (corresponding to 100 mV/MIP, where 1 MIP = 25000 *e* for a minimum ionising particle traversing a 300 μm thick silicon sensor) is presented to the pipeline input. Up to 4 μs worth of information can be stored in the 192 cells of the pipeline. The fate awaiting the information stored in each pipeline cell depends on the mode of operation of the chip and whether or not a trigger has been initiated. A digital pipeline control block consisting of write and trigger pointers sequences the writing, triggering, storing, and retrieval of data from the pipeline. When a trigger is received, useful data are marked after a programmable latency, and held in the pipeline until they can be read out. A 32 deep FIFO retains the addresses of pipeline columns holding marked data. When a signal is read from the pipeline it is processed by a switched capacitor filter, the analogue pulse shape processor (APSP).

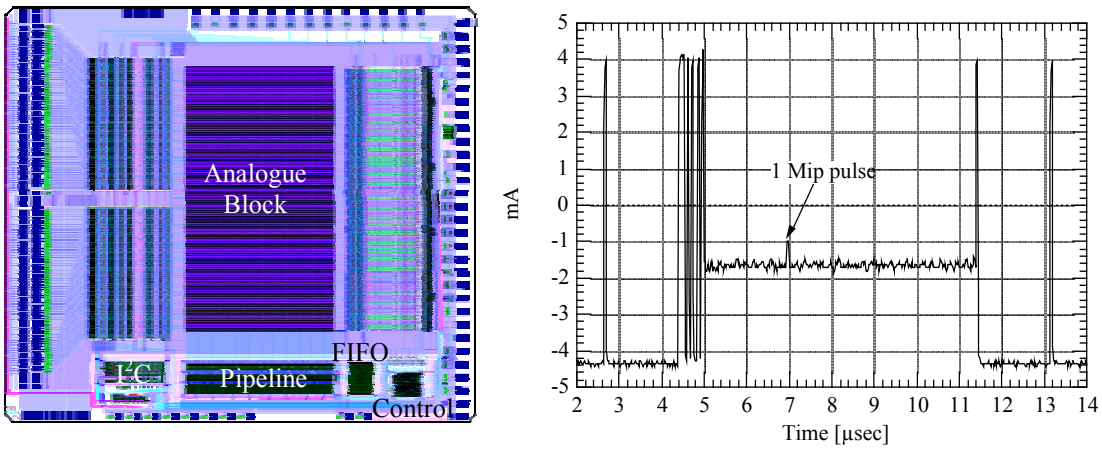
1.4.2 The APSP

The action taken by the APSP is determined by one of three modes of operation. The first mode of operation, *deconvolution*, is used in normal operation when data rates are sufficiently high such that the effects of pile-up are significant. In this mode the APSP removes the effects of pile-up to confine the signals to one 25 ns interval. The APSP implements the deconvolution algorithm on the charges from three consecutive pipeline

cells, storing them on three capacitors of different sizes (corresponding to the deconvolution weights). It then outputs a weighted sum of the contents of the three capacitors. The second mode, *peak*, is used when pile-up is not significant and a larger signal-to-noise ratio is required. Here the APSP acts simply as an amplifier and the charge from only one pipeline cell is passed onto the first APSP capacitor. The first capacitor is smaller in peak mode, ensuring that both modes of operation result in the same gain. Although both modes of operation have the same gain, the signal-to-noise ratio is better in peak mode. This is because the noise is higher (by a factor of ~ 1.7) in deconvolution mode since the rising edge of the shaper output, which is used for the third sample, is prone to slewing effects. The third mode, *Multi*, can be used when calibrating a pulse shape, and in this mode multiple consecutive pipeline columns can be triggered and read out without APSP filtering.

1.4.3 APV25 Output

The outputs from all the 128 channel shaper stages are multiplexed (the order does not correspond to the natural channel order) and driven off the chip as a differential bi-directional current preceded by a digital stream. This consists of a 3-bit digital header, the 8-bit pipeline column address and an error bit. The amplitude of the digital header is +/– 4 mA and the final analogue gain is +/– 1 mA/MIP, Fig. 1.6 (a). Data can be read out at either 20 MHz or 40 MHz rates, and for the 20 MHz rate, interleaving allows for two-chip read-out at a rate of 40 MHz.



(a) APV25-S1 Layout. The total area is 8.06 × 7.1 mm².

(b) One line of the APV25 differential output.

Figure 1.6: APV25 layout and output.

The main digital blocks are indicated: the I²C bias registers, pipeline pointers, FIFO and control logic.

1.4.4 Additional Features of the APV25

An internal calibration circuit enables the testing of the analogue circuitry. It generates and injects a pulse of programmable amplitude into between one and eight groups of 16 channels. The timing of the calibrate pulse is adjustable in steps of 3.125 ns.

An on-chip bias generator controls the biases (current, voltage or charge) of the analogue stages of the APV25. A two-wire serial 'slow control' interface based on the Philips I^2C protocol is used to program the chip operation mode, internal bias registers and calibration settings. The I^2C interface also handles error states.

Since both clock and trigger lines to the chip are active during the sensitive acquisition time of the chip, they are implemented using low voltage differential signals (LVDS) to minimise interference. In addition to the normal trigger signal sent as a single pulse, a 1 on the *TRIG* line, reset and calibration request signals can also be sent. The reset signal consists of two pulses separated by one clock cycle, 101. This instructs the chip to clear any pipeline pointers and re-launches them with the programmed latency value. A calibrate request signal is a double pulse, 11, on the *TRIG* line. The different *TRIG* signals mean that normal triggers must be separated by at least two clock cycles.

Under normal running conditions the APV25 chip shows very good linearity, better than 5 % over a 5 MIP range, as well as substantial improvements in noise when compared with its predecessors (noise at 0 pF is 246 and 396*e* rms with a slope of 36 and 59.4*e* rms/pF in peak and deconvolution mode, respectively). Its power consumption is 2.3 mW/channel.

1.5 Summary

The intense radiation field produced by the LHC and the requirement to operate the Tracker microstrip detectors at –10 ^{o}C define the operational environment of the APV25. Approximately 75 000 APV25 chips will be required to read out the ~10^7 microstrip channels. Because the APV25 is manufactured in a commercial CMOS process, it has to be thoroughly evaluated before it can be deployed on such a large scale in CMS.

Chapter 2
MOSFET Operation

The APV25 readout chip is manufactured in a commercial 0.25 μm CMOS technology. To understand how the APV25 will perform in the CMS Tracker environment some knowledge of the operation of the Metal Oxide Semiconductor Field Effect Transistor (MOSFET), the basic building block of the chip, is required. This chapter introduces the properties of the MOSFET and explores how radiation and temperature effects can change its behaviour.

2.1 MOS Device Physics

The MOSFET is essentially a MOS capacitor with two p-n junctions placed adjacent to the channel. CMOS processes use silicon (Si) technology since it is the most mature among all semiconductor technologies. In addition, silicon is easily available, making it the cheapest semiconductor material. It can be doped with impurity atoms, changing its properties. For example, if an arsenic atom with five valence electrons takes the place of one Si atom in the lattice, four of its valence electrons form covalent bonds with surrounding Si atoms and the fifth electron is essentially free for conduction. The silicon is said to be n-type and the arsenic atom is called a donor. When a boron atom with three valence electrons takes the place of a silicon atom, all three valence electrons form covalent bonds and the absence of a fourth electron creates a hole. This is a p-type semiconductor, and the boron atom is an acceptor atom.

The energy at which the probability of finding an electron in a given electronic state is one half is called the Fermi level, E_F. In an n-type (p-type) semiconductor, E_F is closer to the conduction (valence) band. In a very pure slab of silicon the Fermi level is exactly half way between the valence and conduction band. The silicon is in its intrinsic state and its Fermi level is called the intrinsic Fermi level, E_i. The corresponding intrinsic carrier density is n_i ($n_i = 9.65 \times 10^9$ cm^{-3} at room temperature [11]).

2.1.1 Charge Carrier Transport

The motion of charge carriers in MOS devices is the result of two basic transport phenomena, carrier drift and carrier diffusion.

Carrier drift arises in the presence of an electric field. Taking the case of an n-type semiconductor as an example, the charge carriers are electrons. With no applied field,

the thermal motion of an electron can be visualised as a succession of random scattering from collisions with lattice and impurity atoms and other scattering centres. Over a sufficiently long period of time, the net displacement is zero. The average time between collisions is called the mean free time, τ_c. With an applied electric field, ξ, the electron experiences a force of $-q\xi$ and is accelerated in the opposite direction to the field. The additional velocity component introduced is called the drift velocity, v_n. Conservation of momentum leads to the following expression for v_n:

$$v_n = -\left(\frac{q\tau_c}{m_n}\right)\xi \qquad \text{..... eq. (2.1).}$$

where m_n is the effective electron mass which takes into account the influence of interactions with the positive ion cores. The factor $\frac{q\tau_c}{m_n}$ is called the mobility, μ_n (units cm^2/Vs). Various scattering mechanisms contribute to the total mobility of which the most important are lattice scattering from thermal vibrations, μ_L, and impurity scattering, μ_I, when a charge carrier travels past an ionised impurity. The temperature and doping dependence of mobility will be discussed later. The total mobility is given by:

$$\frac{1}{\mu} = \frac{1}{\mu_L} + \frac{1}{\mu_I} \qquad \text{.....eq. (2.2).}$$

Carrier diffusion arises from the movement of charge carriers from a region of high concentration to a region of low concentration, resulting in a diffusion current. The net current is a combination of drift and diffusion components.

2.1.2 The p-n Junction

The p-n junction is a diode since it allows current to flow only in one direction. It is formed by bringing into contact doped p- and n-type semiconductors, Fig. 2.1.

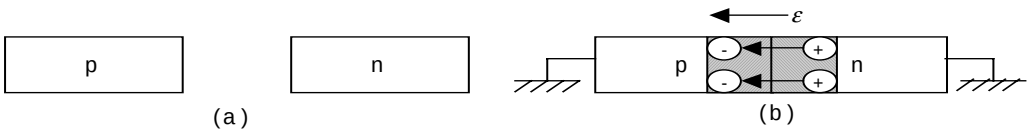


Figure 2.1: The p-n junction.
(a) Uniformly doped p-type and n-type semiconductors before junction is formed.
(b) The electric field in the depletion region.

The large carrier concentration gradients at the junction cause carrier diffusion. Holes from the p-side diffuse into the n-side and electrons from the n-side diffuse into the p-

side. These recombine to remove all free carriers from a small region at the interface called the depletion region. Here, only ionised donors and acceptors remain with a resulting electric field directed from the positive charge to the negative charge.

The junction properties can be modified by applying an external bias. The junction is said to be forward-biased when a positive voltage is applied to the p-side with respect to the n-side. This reduces the depletion layer width and the reduced energy barrier for majority carriers leads to increased diffusion currents. The junction is reverse-biased when a positive voltage is applied to the n-side with respect to the p-side. Reverse bias increases the depletion region width. Fewer carriers have enough energy to diffuse over the higher energy barrier and the diffusion current is strongly suppressed. Only a very small net negative drift current remains. The ideal p-n junction diode equation is:

$$I = I_0\left(e^{\frac{eV_A}{kT}} - 1\right) \qquad \text{.....eq. (2.3).}$$

It is derived using the depletion approximation for an abrupt junction and assuming no external generation sources, no generation or recombination in the depletion region and low-level injection. In practice, eq. (2.3) cannot adequately describe the behaviour of semiconductors with small n_i such as silicon, because of generation and recombination of carriers in the depletion region. Under the reverse-bias condition, the generation current can become significant. For a small forward bias, the recombination current can dominate over the diffusion component.

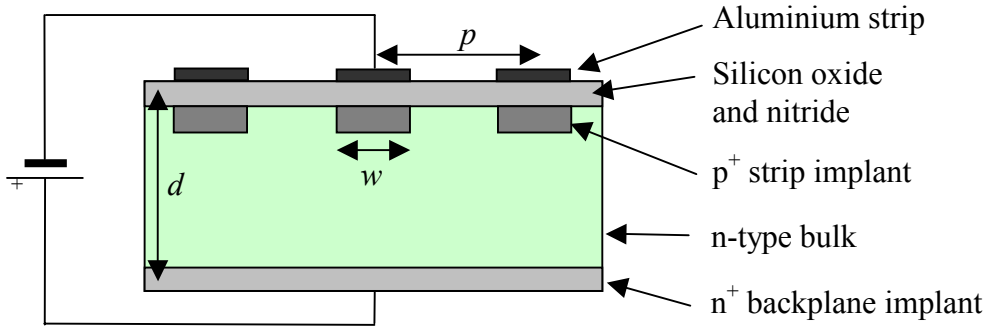


Figure 2.2: Cross-section through an AC-coupled strip detector where w is the strip width, p is the strip pitch and d is the detector thickness [12].

The silicon p-n junction is at the heart of diode detectors that have been used extensively in the physics of radiation detection [13]. The Tracker microstrip sensors are essentially rows of p-n junctions, manufactured by implanting highly doped p^+ strips on an n-type substrate, Fig. 2.2. Particles traversing the sensors generate electron/hole pairs and the resulting current is AC-coupled to the readout electronics.

2.1.3 The MOS Capacitor

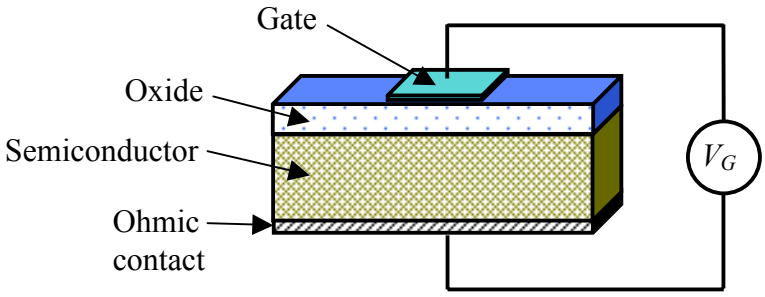


Figure 2.3: Schematic of a MOS capacitor.

In a silicon-based MOS capacitor the gate is usually made of polysilicon, and the oxide is SiO_2, Fig. 2.3. When the semiconductor substrate is p-type silicon, applying a negative voltage to the metal gate ($V_G < 0$) with respect to the ohmic contact leads to an accumulation of majority charge carriers (holes) near the oxide-semiconductor interface. For a small positive gate bias ($V_G > 0$), holes are expelled from the oxide-semiconductor interface leaving negatively charged acceptor ions. As V_G increases, the electron concentration at the oxide-semiconductor interface increases. Eventually, the inversion region is reached where the electron concentration at the interface exceeds the hole concentration.

The gate voltage at which the minority carrier concentration in the inversion layer is equal to the majority carrier concentration in the bulk semiconductor is called the threshold voltage, V_{th}, given by:

$$V_{th} = 2\phi_F + \frac{\varepsilon_r^s x_{ox}}{\varepsilon_r^{ox}} \sqrt{\frac{4eN_A}{\varepsilon_r^s \varepsilon_0} \phi_F} \qquad \text{.....eq. (2.4) for p-type Si.}$$

$$V_{th} = 2\phi_F - \frac{\varepsilon_r^s x_{ox}}{\varepsilon_r^{ox}} \sqrt{\frac{4eN_D}{\varepsilon_r^s \varepsilon_0} (-\phi_F)} \qquad \text{.....eq. (2.5) for n-type Si.}$$

where ε_r^s, ε_r^{ox} are the relative permittivities of Si and SiO_2 respectively, ε_0 is the permittivity of free space, N_A and N_D are acceptor and donor concentrations, e is the elementary charge and ϕ_F is the electrostatic potential at the Fermi level w.r.t the intrinsic level. ϕ_F is given by:

$$\phi_F = \frac{kT}{e} \ln\left(\frac{N_A}{n_i}\right) \qquad \text{.....eq. (2.6) for p-type Si.}$$

$$\phi_F = -\frac{kT}{e} \ln\left(\frac{N_D}{n_i}\right) \qquad \text{.....eq. (2.7) for n-type Si.}$$

where k is the Boltzmann constant and T is the temperature in Kelvin.

2.1.4 The MOSFET

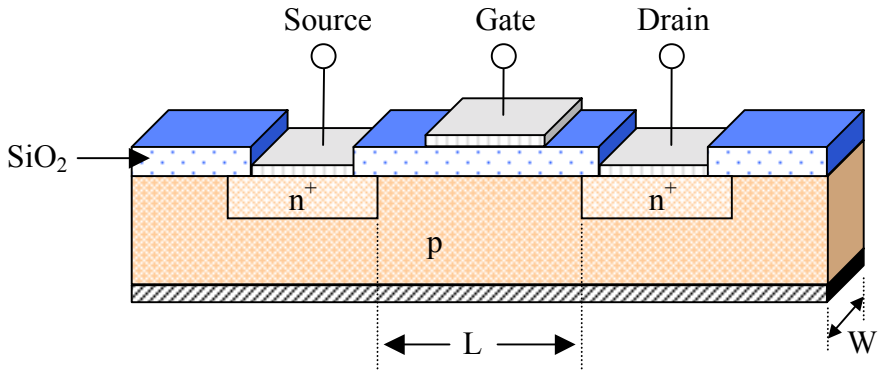


Figure 2.4: Schematic diagram of an n-channel MOSFET.

In the n-channel MOSFET known as NMOS, Fig. 2.4, the drain and source diffusions (n^+ implants) adjacent to the conducting channel are heavily doped with ions of the opposite polarity to that of the ions in the channel or bulk. Contacts are made to the source, drain and gate. Parameters of interest are the gate-to-source voltage, V_G, the drain-to-source voltage, V_D, and its corresponding current, I_D. An additional contact can also be made to the bulk and a voltage applied here will combine with the gate voltage to change the properties of the channel.

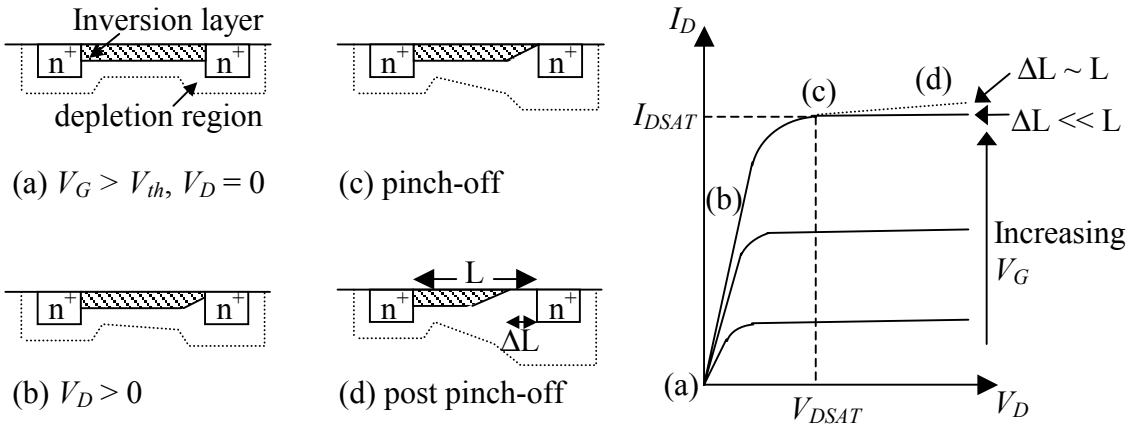


Figure 2.5: $V_G > V_{th}$ in (a), (b), (c) and (d).

The schematic diagrams depict the change in shape of both the inversion layer and the depletion layer in an n-channel MOSFET as V_D increases. The I_D-V_D curve shows how I_D varies with V_D.

When no voltage is applied to the gate, the region between the source and the drain immediately below the oxide contains excess holes and very few electrons, effectively an open circuit since no current can flow between the drain and the source. With the application of a sufficiently positive V_G, an inversion layer forms, enabling a current to

flow between the drain and the source. The greater V_G is, the stronger the inversion in the conducting channel and the higher the conductance between source and drain.

For a fixed value of V_G above threshold, the magnitude of the drain-to-source current flowing through the conducting channel is controlled by V_D. For a small positive V_D, electrons flow from the source to the drain and the channel acts as a resistance so I_D is proportional to V_D and the transistor is said to be operating in the linear region, Fig. 2.5 (b). As the drain voltage is increased, it eventually reaches a point at which the inversion layer width is reduced to zero near the drain implant. This is the pinch-off point beyond which the current remains essentially the same, Fig. 2.5 c). As the drain voltage is further increased, the inversion layer retreats away from the drain implant and the channel length decreases from a length L to a length $L - \Delta L$, Fig. 2.5 d). In practice, for smaller channel lengths, I_D continues to increase slowly beyond the pinch-off point.

To describe the drain current, I_D, an expression is required for each region of operation. In the linear region of operation below pinch-off, I_D is given by:

$$I_D = \frac{W\mu_n C_{ox}}{L}\left[(V_G - V_{th})V_D - \frac{V_D^2}{2}\right] \qquad \text{.....eq. (2.8).}$$

At pinch-off, $I_D = I_{DSAT}$, $V_D = V_{DSAT} = V_G - V_{th}$ and substituting this information into eq. (2.8) leads to:

$$I_{DSAT} = \frac{Z\mu_n C_{ox}}{2L}(V_G - V_{th})^2 \qquad \text{.....eq. (2.9).}$$

Beyond pinch-off, in the region of operation also known as saturation, the drain current does not increase and eq. (2.8) can be used, substituting I_D for I_{DSAT} and V_D for V_{DSAT}.

2.1.4.1 MOSFET Transconductance

The transconductance, g_m, is given by the following equations:

$$g_m = \frac{\partial I_D}{\partial V_G} = \frac{W\mu_n C_{ox}}{L} V_D \qquad \text{.....eq. (2.10) in the linear region.}$$

$$g_m = \frac{W\mu_n C_{ox}}{L}(V_G - V_{th}) \qquad \text{.....eq. (2.11) in the saturation region.}$$

The channel conductance is essentially zero in saturation for an idealised MOSFET and in the linear region it is given by:

$$g_d = \frac{\partial I_D}{\partial V_D} = \frac{W\mu_n C_{ox}}{L}(V_G - V_{th}) \qquad \text{.....eq. (2.12).}$$

2.1.4.2 MOSFET Subthreshold Current

The subthreshold current is the drain current for $V_G < V_{th}$ where the conducting channel is only weakly inverted. It is dominated by diffusion instead of drift and as a consequence, it decreases exponentially with decreasing V_G below V_{th}:

$$I_D \approx e^{q(V_G - V_{th})/kT} \qquad \text{……eq. (2.13).}$$

The subthreshold region of operation is important in digital circuits where transistors act as on/off switches because it describes where the switch changes state. It is not so important in analogue circuits where transistors are operated in strong inversion.

2.1.5 Technological Trends

Over the past forty years the benefits of higher density, lower power consumption, improved performance and reduced costs as transistors reduce in size have encouraged continued growth in the CMOS technology sector. In 1965 Gordon Moore predicted that the number of transistors on integrated circuits would double each year. Ten years later, his predictions were observed to be correct and his initial statement acquired the status of a law, called Moore's law (with a modification in the time scale from one year to nearly two years). Table 2.1 illustrates the difference between two generations of Intel Pentium processes.

Table 2.1: Comparison of two Intel Pentium process generations.

Process	Year	Gate length [μm]	No. of transistors [$\times 10^6$]	Die size [mm^2]
P648	1989	1	1.2	79
P858	2000	0.18/0.13	42	217

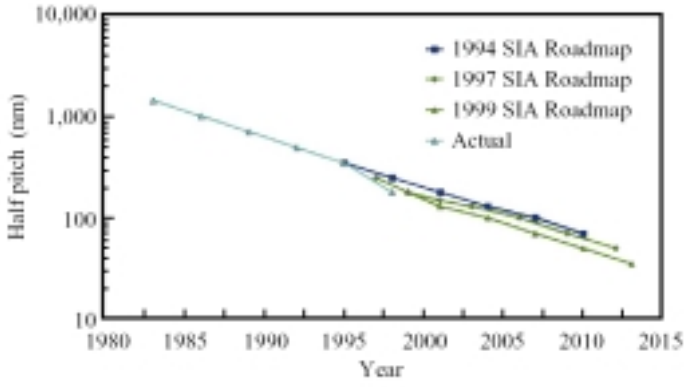
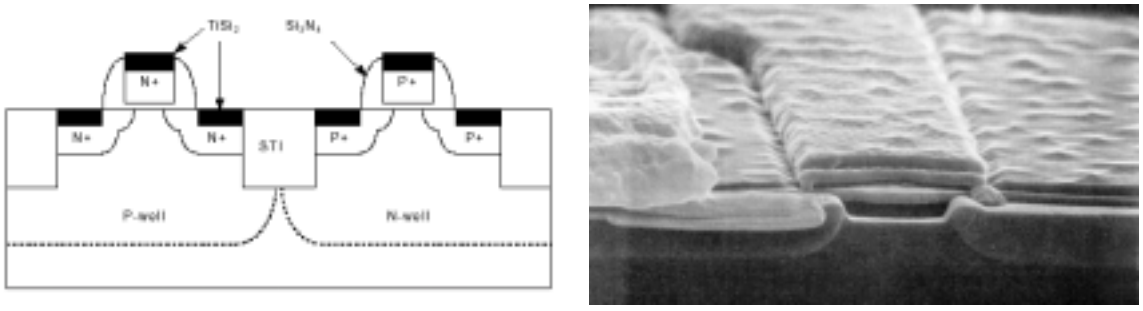


Figure 2.6: Trends in lithographic resolution.

Half pitch represents the minimum size of lithographic features on a chip. (SIA-Semiconductor Industry Association) [14].

The reduction in transistor dimensions can be attributed to improvements in the lithographic resolution and in the design of transistors. Fig. 2.6 illustrates the trends in

lithographic resolution. One major consequence of these is that the conducting channel becomes shorter. This leads to the so-called short-channel effects, affecting the operation of MOSFET transistors and leading to a departure from the idealised behaviour outlined previously. For example instead of remaining constant, the drain current increases with drain voltage beyond V_{DSAT}. If the channel length approaches the depletion layer widths of the source and drain junctions, a condition known as punch-through occurs, where the gate loses control of the current. Minimising the short-channel effects can be achieved by reducing transistor dimensions and voltages by a scaling factor α, which ensures that all internal electric fields remain the same as those of long-channel MOSFETs. As the gate oxide is made thinner, tunnelling effects become more pronounced and will eventually limit the size of transistors.



(a) Schematic cross-section of a 0.25 μm process [15].

(b) Scanning electron microscope photograph of an NMOS transistor.

Figure 2.7: Modern CMOS technologies.

Fig. 2.7 shows a schematic cross-section of a 0.25 μm CMOS process along with a photograph of a MOS transistor.

2.1.6 Noise

Noise, in the broadest sense, can be defined as any unwanted disturbance that obscures or interferes with a desired signal [16]. In cases of interest here, the term noise refers to spontaneous fluctuations in the current passing through, or the voltage developed across, semiconductor bulk materials or devices. These spontaneous fluctuations which are related to the discrete nature of charge carriers set a lower limit to the quantities to be measured or the signal to be amplified.

The CMS microstrip detectors will produce current signals, which have to be read and amplified by the APV25. Amplification is the first stage in signal processing to ensure that later stages do not significantly contribute to the noise [17]. The overall signal-to-

noise ratio is therefore determined by the noise due to the amplifier, ideally arising in the input transistor of the preamplifier [18].

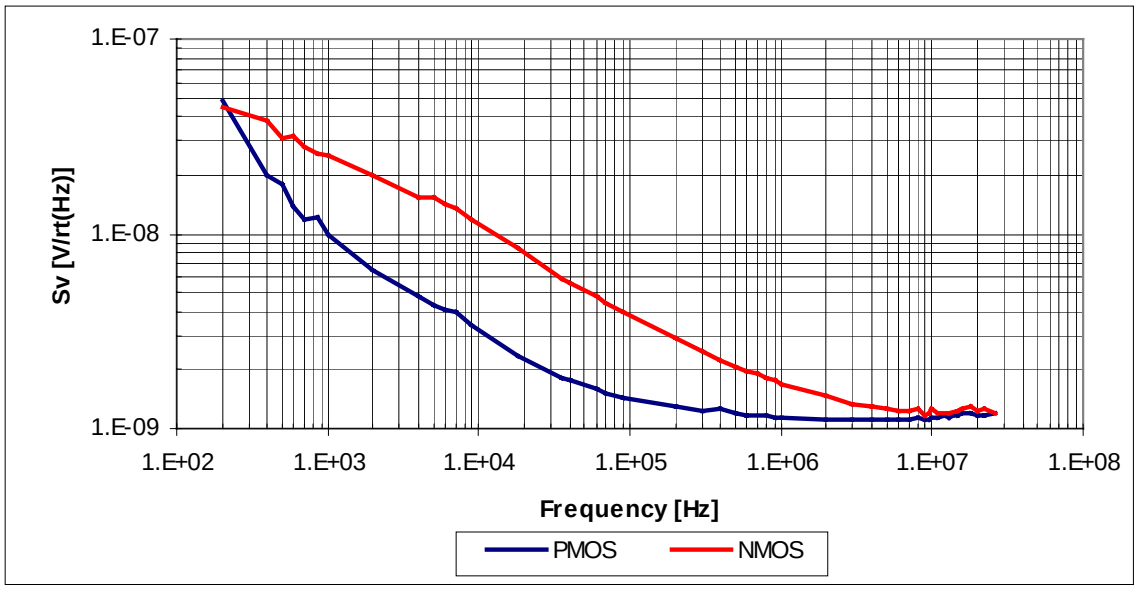


Figure 2.8: Noise spectrum of PMOS and NMOS transistors from a 0.5 μm process.

The typical voltage noise spectral density of MOSFETs is illustrated in Fig. 2.8. Two distinct frequency regions can be identified, with different noise behaviour in each. At low frequencies, the dominant component of the noise is frequency dependent. At high frequencies, the noise is essentially frequency independent. The two regions can be thought of as separated by a 'corner frequency', f_c. Values from several Hz to several hundred kHz are common for this parameter. As is apparent in Fig. 2.8, the corner frequency is higher for NMOS than it is for PMOS.

2.1.6.1 1/f Noise

The noise dominating at low frequencies is called 1/f noise because the power spectral density for the current caused by this type of noise is practically proportional to 1/f. It is also known as flicker noise and has historically been explained as free-carrier exchange with traps at interfaces, which cause a fluctuation of carrier density. The model explains the near-linear increase of 1/f noise with decreasing frequency. This model was first proposed by McWorther and is better adapted for noise at interfaces and therefore MOSFET devices [19].The increase in noise is a result of a distribution of characteristic exchange times related to the traps' spatial distance into the oxide and/or energy difference from the semiconductor band edges [20]. The further a trap is from the SiO_2/Si interface, the lower its frequency response. Hooge proposed another model based on mobility fluctuation, which is more consistent with noise in bulk semiconductors [21].

The gate referred voltage noise is given by:

$$S^2_{V,1/f} = \frac{A_f}{f^{\alpha}} \qquad \text{……eq. (2.14).}$$

where f is the frequency, α is an experimental coefficient known as the flicker noise exponent (typically ~ 1) and A_f represents the voltage noise in units of V^2 at its intercept with the y-axis. A_f is given by:

$$A_f = \frac{K_f}{(C_{ox})^2 WL} \qquad \text{…….eq. (2.15).}$$

where C_{ox} is the gate capacitance per unit area, W and L are the nominal channel width and length respectively, and K_f is a technology-dependent parameter known as the flicker noise coefficient. Eq. (2.15) shows that the 1/f noise component is dependent on process technology and transistor dimensions. For the transistors shown in Fig. 2.8, A_f is around 10^{-14} V^2. For the 0.25 μm technology used to manufacture the APV25, K_f is of the order of 10^{-25} V.C [22].

2.1.6.2 Thermal Noise

Thermal noise (also called white noise, Johnson noise or Nyquist noise) is the type of noise best characterised for the MOSFET. It is dominant at high frequency and independent of frequency. The origin of this noise can be traced to the random thermal motion of carriers in the channel. This is similar to the mechanism in resistors where the thermal noise spectral density is given in voltage by *4kTR*, *R* being the resistance. The derivation for the channel thermal noise of a MOSFET is more complex than that of a resistor since the operating region of the device has to be taken into account. In saturation and strong inversion, the following expression is used for the thermal noise:

$$S^2_{V,White} = \frac{8}{3} kT \frac{\Gamma}{g_m} \qquad \text{……eq. (2.16).}$$

where k is the Boltzmann constant, T is the temperature in Kelvin, Γ is the excess noise factor (typically ~ 1) and g_m is the transconductance given earlier, eq. (2.11).

2.2 Consequences of Radiation on MOSFET Operation

Severe degradation of the operational characteristics of MOS devices and circuits can result from exposure to ionising radiation. Ionising radiation is simply defined as that with an energy above the threshold to break atomic bonds and create electron/hole pairs in the materials of interest, which are Si and SiO_2 in silicon-based MOS devices.

Photons or charged particles such as electrons, protons, or atomic ions can all cause ionisation.

Another class of radiation damage exists, displacement damage, where atoms in a material are displaced from their original locations by the incident radiation. Displacement damage is primarily caused by hadrons and can result in a reduction in the gain of bipolar transistors through a deterioration of the minority carrier lifetime in the silicon substrate. MOS devices are not affected by changes in the minority carrier lifetime and are therefore relatively insensitive to displacement damage.

Ionising radiation effects in MOS devices can be divided into two categories:

- total dose effects which are due to an accumulation of ionising radiation over a period of time in the oxide layers in MOS devices and circuits.
- transient radiation effects (or Single Event Effects, SEE) due to the generation of photocurrents in the silicon substrate by high-dose-rate radiation such as the passage of highly energetic particles.

2.2.1 Total Dose Radiation Effects

When a MOSFET is exposed to high-energy ionising radiation, electron/hole pairs are created uniformly throughout the oxide. These carriers can be trapped in the oxide and at the Si/SiO_2 interface [23]. The number of electron/hole pairs created in a material is directly proportional to the amount of energy absorbed by that material. The total dose is commonly expressed in units of rads, equal to 10^{-2} joules absorbed per kilogram of the specified material (1 rad = 10^{-2} Gy = 100 erg.gm^{-1}). All the effects characterising the parameter evolution of the MOSFET after irradiation are grouped under the term annealing.

Following electron/hole pair generation in the oxide by ionising radiation, electrons rapidly drift out of the oxide since the electron mobility is high (low field mobility at T = 300 K is $\mu \sim 20$ cm^2.V^{-1}.s^{-1}), leaving holes, which have much lower mobility ($\mu \sim 10^{-4}$–10^{-11} cm^2.V^{-1}.s^{-1}), trapped in the oxide. The electron/hole pair creation energy in SiO_2 is around 18 eV [24]. Radiation-generated electrons play a minor role in initial recombination processes but are otherwise generally ignored in discussions of charge trapped in the oxide. Not only are they highly mobile but long term trapping rates are up to six orders of magnitude less than those for holes.

Much work has been done to characterise charge generation and recombination, hole transport and charge trapping in SiO_2 in thick oxides (d_{ox} > 20 nm), a good summary of which can be found in [25]. Many models have been used to describe experimental data

such as the columnar recombination model (when charge pairs are deposited in dense columns and recombination is a strong process), the Onsager geminate recombination model (when charge pairs are created far apart on average and recombination is a weak process) and the continuous-time random walk (CTRW) model for hole transport. This work successfully identified the characteristics of oxide trapped charge such as the field, temperature and oxide thickness dependence and the location and type of traps. The hole traps are local oxygen vacancy defects such as strained Si-Si bonds that can capture holes and become various forms of a defect know as the *E'* centre. The accumulated knowledge has lead to the adoption of measures to harden thick oxides for use in radiation environments.

Improvements in oxide quality (fewer contaminants, low-growth-temperature) and the scaling of CMOS technologies, in particular the reduction of d_{ox}, have led to a reduction in oxide trapped charge and an increase in the inherent radiation hardness of MOS devices [26]. For $d_{ox} > 10$ nm the effects of radiation generated charge generally drop as the square of the oxide thickness. For $d_{ox} < 10$ nm, most of the holes are removed from the oxide within seconds to minutes and the models developed to describe hole generation, transport and trapping in thicker oxides are no longer valid [27]. The main processes of hole removal are described in the following paragraph.

Immediately after oxide trapped charge is created it begins to be neutralised. This process is dependent on time, temperature and electric field and can be accounted for by invoking two mechanisms [25], Fig. 2.9:

- the tunnelling of electrons from the silicon into oxide traps,
- the thermal emission of electrons from the oxide valence band into oxide traps.

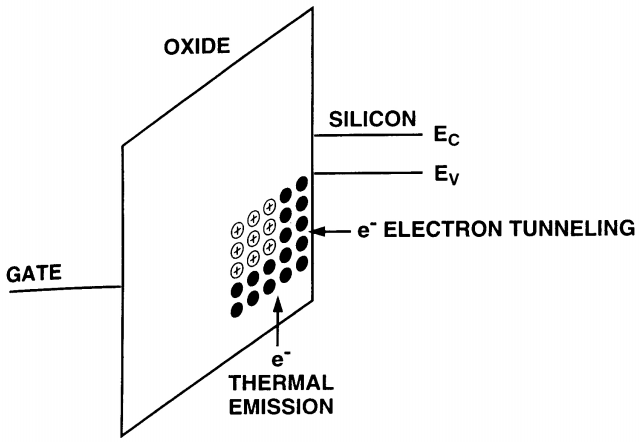


Figure 2.9: Schematic diagram illustrating the neutralisation of oxide-trap charge by electron tunnelling from the silicon and by thermal emission of electrons from the oxide valence band.

The first mechanism can be depicted as a tunnelling front moving into the oxide. If this front is defined as the position corresponding to the maximum rate of tunnelling, $x_m(t)$, then the distance of the front into the oxide at a given time t is given by:

$$x_m(t) = \frac{1}{2\beta}\ln\left(\frac{t}{t_0}\right) \qquad \text{……eq. (2.17).}$$

where β is the tunnelling barrier height parameter, and t_0 is a time scale parameter [25]. This simple model is not complete since after a given distance in the oxide, there are fewer trapped holes in certain oxides and the rate of annealing decreases with time.

At temperatures above 150 ^{o}C, hole removal occurs via the thermal process. Trapped hole annealing depends on both the energy level and spatial distribution of traps which are heavily process-dependent.

The 0.25 μm process used in the manufacturing of the APV25 has an oxide thickness of 5.5 nm, allowing neutralisation of oxide traps during the process of ionisation by tunnelling from both sides of the oxide. Work done by Benedetto *et al.* has shown that, for 5.3 nm oxides, the tunnelling front from the silicon meets that from the gate close to the middle of the oxide about 1 s after hole generation and trapping [28].

The lack of oxygen at the SiO_2/Si interface introduces strained and uncompleted bonds. These can trap charge from the Si conduction and valence bands and are the so-called interface traps. The pre-irradiation interface-trap density is usually too small to cause any significant effect (< 10^{10} traps/cm^2). However, ionising irradiation generates additional interface traps which can affect the operation of MOS devices. Interface traps are located within one or two atomic bond distances (0.5 nm) from the silicon lattice. Unlike oxide trapped charge which is always positive, interface trapped charge can be positive, neutral or negative. Because of this, interface traps are identified as either donors or acceptors. For NMOS transistors, interface traps contribute a net negative charge and are therefore acceptors. For PMOS transistors, interface traps contribute a net positive charge and are therefore donors.

A trivalent Si atom bonded to three other Si atoms, the P_b centre, has been identified as the defect responsible for interface traps in work by Lenahan and Dressendorfer [29].

The most common technique for measuring interface traps in transistors is the subthreshold technique. It consists of analysing changes in the subthreshold slope or swing, S, of the I_D-V_G curve. S is defined as the change in V_G required to reduce the transistor current by one decade.

The change in interface trap density, ΔD_{it}, following an irradiation is given by:

$$\Delta D_{it} = [C_{ox} / kT \ln(10)](S_{Drad} - S_{Do}) \qquad \text{.....eq. (2.18).}$$

where S_{Do} and S_{Drad} are subthreshold swings measured before and after irradiation, respectively [25].

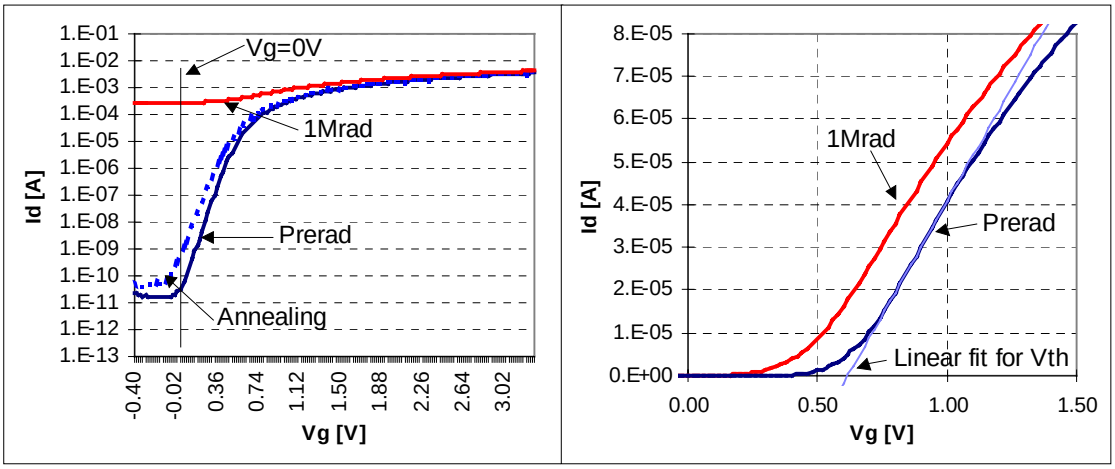
Interface trap buildup occurs on time scales much slower than oxide trapped charge buildup and continues to evolve after irradiation. It is dependent on many variables such as dose, dose rate, electric field, temperature and processing. Many workers have reported a D^X dependence on dose with X ranging from 0.65 to 0.95 for $d_{ox} > 45$ nm. For very thin oxides, interface trap buildup is observed to be strongly suppressed. Saks *et al.* have reported a ΔD_{it} which is very much smaller in very thin oxides ($d_{ox} < 12$ nm) compared with that predicted from the D^X dependence observed in thicker oxides [30]. This is attributed to the tunnelling of radiation-induced holes out of the oxide (equivalent to electrons tunnelling into oxide) before conversion of the holes to interface states. The buildup of interface traps is strongly temperature dependent. Below 100 K, electrons and holes are essentially 'frozen' and interface trap buildup is completely inhibited. Unlike oxide trapped charge, interface trapped charge does not anneal at room temperature [25]. Significant annealing is observed only for T > 100 ^{o}C.

The consequences of oxide trapped charge and interface trapped charge on the electrical characteristics of the MOSFET are the following:

- threshold voltage shift,
- decrease in mobility,
- increase in noise,
- increase in leakage current.

Effects on the thin gate oxide are responsible for the first three consequences. Charge trapped in the lateral and field oxides used to isolate drain and source implants and to isolate adjacent MOSFETs causes the increase in leakage current.

Fig. 2.10 shows the effects of leakage current and threshold voltage shift on the electrical characteristics of a MOSFET.



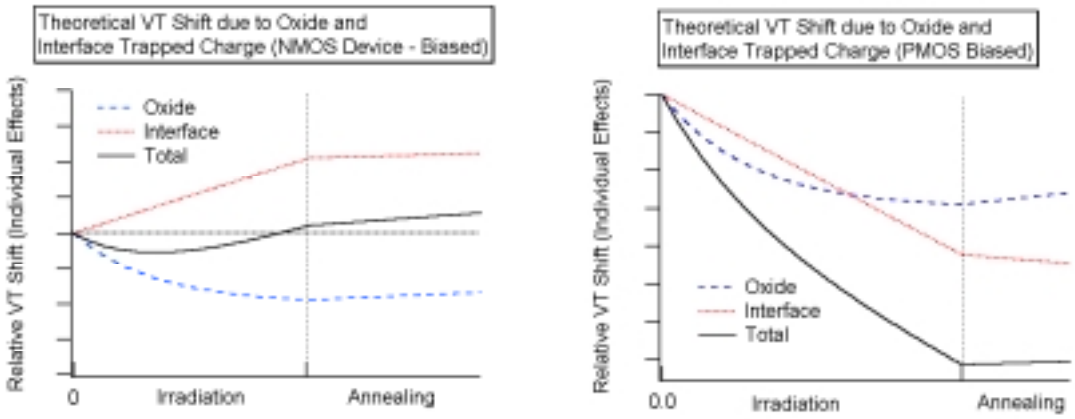
(a) *(b)*

Figure 2.10: Drain current as a function of gate voltage.

(a) in logarithmic scale as a function of gate voltage to show the leakage current, and (b) in linear scale to show the threshold voltage shift.

2.2.1.1 Threshold Voltage Shift

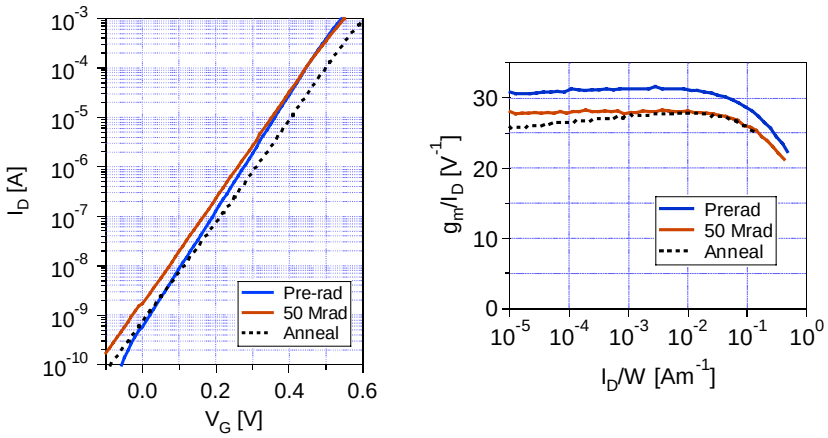
The trapped charge in the oxide and at the Si/SiO_2 interface causes a shift in the threshold voltage. Oxide trapped charge is always positive and causes a negative shift in the threshold voltage for NMOS and a positive shift (in absolute value) in the threshold voltage for PMOS. Interface trapped charge causes a positive threshold voltage shift in both NMOS and PMOS. Since oxide trapped charge is positive for both N- and PMOS transistors, oxide trapped charge and interface trapped charge compensate each other for n-channel transistors and have a cumulative effect for p-channel transistors, Fig. 2.11.



(a) *(b)*

Figure 2.11: V_{Th} shift in biased (a) NMOS, and (b) PMOS transistors [31].

2.2.1.2 Decrease in Mobility



(a) *(b)*

Figure 2.12: NMOS transistor (a) Subthreshold swing and (b) Transconductance.

Fig. 2.12 illustrates the change in subthreshold swing and transconductance due to irradiation. Interface trap formation is responsible for the decrease in the mobility of carriers by introducing additional Coulomb scattering centres in the conduction channel. Mobility degradation is more pronounced for NMOS than it is for PMOS. Transconductance, which is directly related to mobility, also decreases with irradiation.

2.2.1.3 Increase in Noise

Transistor noise is particularly important for analogue applications. Although 1/f noise is related to traps at the interface, in NMOS devices a good correlation has been shown between the increase in 1/f noise after irradiation and charge trapping in the oxide in defects of the *E'* type located near the interface called border traps [32]. Under normal operating bias conditions (+ve bias for NMOS and –ve bias for PMOS), the 1/f noise of both n- and p-channel transistors decreases through post-irradiation annealing [33].

At high frequencies, a radiation-induced decrease in mobility and transconductance can lead to an increase in noise. It has also been reported that the excess noise factor, Γ (in short-channel devices it accounts for hot carrier effects due to high electric fields, when carriers in the inversion layer are not in thermal equilibrium with the Si substrate), can account for most of the increase in thermal noise [22]. The mechanisms behind the radiation-induced increase in Γ have not been identified or reported in the literature.

2.2.1.4 Increase in Leakage Current

A build up of charge in the oxides used to isolate drain and source implants can lead to a leakage current between those implants and can cause the device to be switched on when there is no external applied bias on the gate.

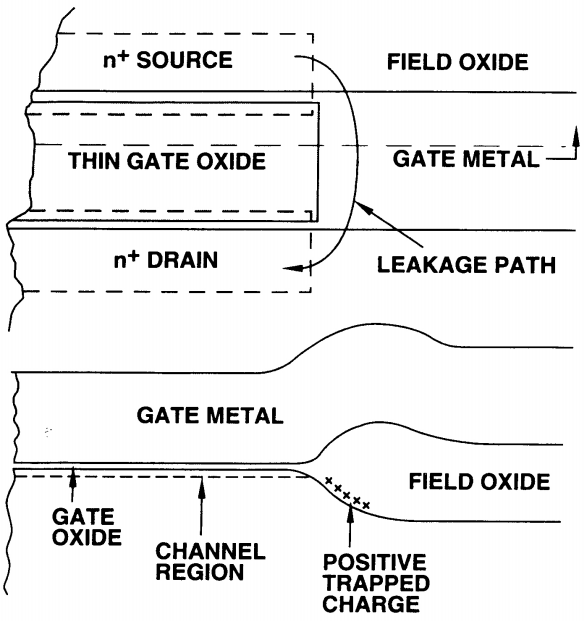


Figure 2.13: Cross-section of a parasitic field oxide transistor showing the primary leakage current paths [34].

Fig. 2.13 illustrates the primary leakage path due to a buildup of positive charge in the lateral (field) oxide for a device using the LOCOS (local oxidation of silicon) isolation scheme. The process used in the manufacturing of the APV25 employs the STI (Shallow Trench Isolation) scheme.

Field oxides are much thicker than gate oxides. Unlike gate oxides, which are routinely grown by thermal oxidation, field oxides are produced using a wide variety of deposition techniques (e.g. Chemical Vapour Deposition, CVD). Thus, the trapping properties of a field oxide may be poorly controlled and can be considerably different than for a gate oxide.

The threshold voltages of parasitic field oxide transistors are initially very large. As radiation-induced oxide charge builds up in a field oxide, it causes a decrease of the threshold voltage of the field oxide parasitic transistor on a p-type substrate (equivalent to an n-channel field oxide transistor). If the buildup of charge is large enough, excessive leakage current can flow from the source to the drain of the gate-oxide transistors and between transistors. This will greatly add to the static supply leakage current of a circuit and, sometimes, functionality is lost.

Because of the nature of trapping in the field oxide (positive charge trapping), increase in leakage current due to irradiation only applies to NMOS transistors.

Special layout techniques can be used to cut the source-to-drain leakage paths which are present at the edges of standard n-channel transistors. One such technique consists of drawing a gate around the drain when designing n-channel transistors, thus eliminating

the edges of the transistor [35, 36, 9]. This is illustrated in Fig. 2.14. Transistors designed with these layout features are known as edgeless or enclosed transistors.

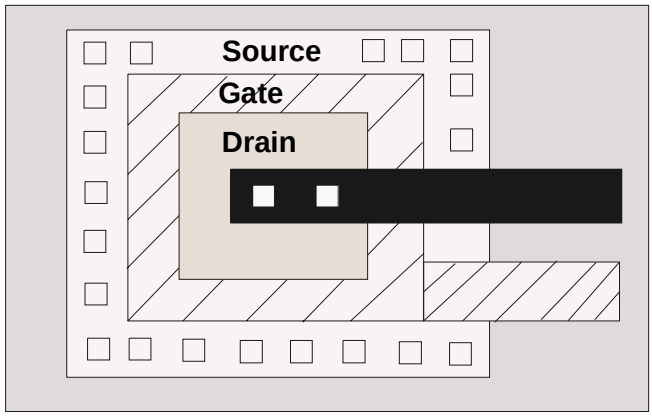


Figure 2.14: Edgeless transistor.

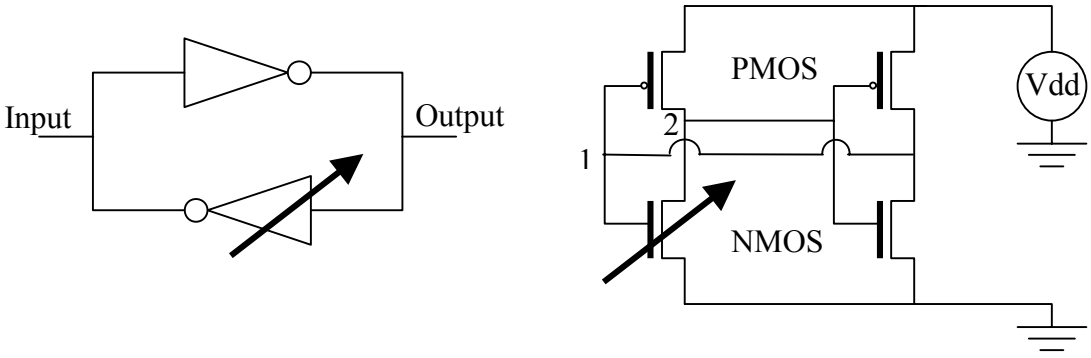
Leakage paths that, under the field oxide, carry current between neighbouring n-channel transistors and between differently biased n^+ diffusions can be cut by the use of channel stops. This is achieved by surrounding the n-channel transistors with p^+ guard rings.
The APV25 design incorporates both enclosed transistors and p^+ guard rings.
Significant differences in radiation hardness have been reported in transistors of different geometry (channel length and width) [37]. Studies on a process with a gate thickness of 25 nm show that transistors with shorter gate lengths tend to show more negative threshold voltage shifts during irradiation but less positive shifts during post-irradiation annealing than transistors with longer channel lengths. Simple scaling theory cannot account for these effects which occur because of differences in trapped-charge densities among devices of different sizes. It is difficult to predict whether the radiation hardness dependence on transistor geometry is significant for processes with thin gate oxides where annealing via tunnelling dominates. A considerable difference has also been observed in the radiation hardness of commercial technologies from different manufacturers since these have little interest in identifying and controlling technology parameters that affect it, such as gate oxide quality [38].

2.2.2 Single Event Effects (SEE)

Single event effects (or transient radiation effects) depend on the rate at which the ionising dose is delivered to a circuit rather than on the total dose delivered. A relatively short pulse in a MOS circuit can be induced by a high-density ionisation track created by the passage of a charged particle, leading to various failure modes. A distinction is usually made between failure modes that are permanent (hard errors) and those that are non-destructive (soft errors). There are three main categories of SEE: Single Event Upset (SEU), Single Event Gate Rupture (SEGR) and Single Event Latchup (SEL).

2.2.2.1 Single Event Upset (SEU)

SEU is a soft error affecting both dynamic and static registers that store logic states. It is characterised by the deposition of sufficient charge on a circuit node to cause the inversion of a logic state. SEUs pose a threat to the normal operation of the digital parts of the APV25 chip because they can cause logic errors in control circuits and bit errors in data transmission by corrupting the digital header address. A detailed knowledge of SEU behaviour under LHC conditions is necessary in order to plan how to operate the chips (e.g. hard resets) in CMS.



(a) Schematic representation. *(b) Circuit description.*

Figure 2.15: A memory cell composed of two cross coupled inverters [39]. *The arrow represents a heavy ion strike.*

Fig. 2.15 depicts a memory cell composed of two cross-coupled inverters and its circuit description. It is designed to have two stable states, one representing a stored '0' and the other a stored '1'. In each state, two transistors are switched on and two are turned off.

A heavy ion strike on one of the inverters can produce a transient change in the voltage appearing at the input of the other. If the input voltage falls below the threshold for switching, the memory cell changes state [40]. Depending on the state of the cell, injection of charge above a critical value, Q_{crit}, at points 1 or 2 will cause the state of the cell to invert. The sensitive volume of the memory cell, defined as that volume in which charge generated by ionisation can be collected fast enough to cause an upset, can be approximated by the drain implant volume of the 'off' NMOS transistor and that of the source of the 'off' PMOS transistor. An incident particle must have a linear energy transfer (LET) high enough to generate charge above Q_{crit} and must strike the sensitive volume for an upset to occur. The LET for a given particle incident on a material is a measure of the rate of energy transfer in that material and is given by:

$$LET = \frac{dE}{dx} \times \frac{1}{\rho} \qquad \text{.....eq.(2.19).}$$

where $\frac{dE}{dx}$ is the energy loss per unit length and ρ is the material density.

The cross-section, σ, for SEU is defined at normal incidence as:

$$\sigma = \frac{N_{events}}{\Phi} [\text{cm}^2] \qquad \text{.....eq. (2.20).}$$

where Φ is the total incident particle fluence, and N_{events} is the number of SEU events counted during the test [41].

SEU results are usually given in plots of cross-section vs. particle LET, which is illustrated in Fig. 2.16. LET_{th} is the minimum particle LET required for SEU and σ_{sat} is the saturating cross-section. The experimental points are often fitted with a Weibull curve using the following expression [42]:

$$\sigma = \sigma_{sat}\left\{1 - \exp\left[-\left(\frac{LET - LET_{th}}{W}\right)^{S}\right]\right\} \qquad \text{.....eq. (2.21).}$$

This allows for the extraction of σ_{sat} and of LET_{th}. W and S are fitting parameters without physical meaning.

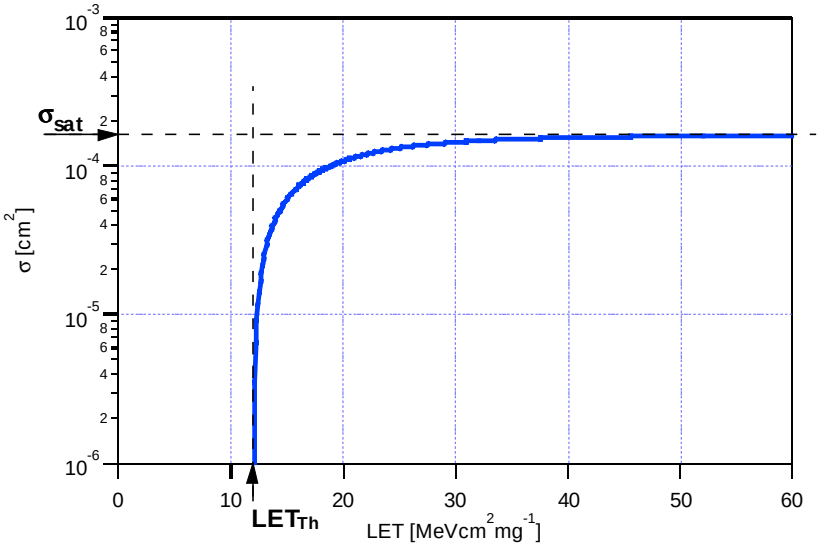


Figure 2.16: A typical cross-section curve.

2.2.2.2 Single Event Gate Rupture (SEGR)

A Single Event Gate Rupture (SEGR) is caused when a highly ionising particle traverses the gate oxide of a MOS device and induces the creation of a dense ionised track. This can lead to an electrical short through the oxide, causing permanent damage. SEGRs are normally associated with power MOSFETs operating under high electric fields. However, their importance has to be assessed for the CMS environment.

Various models have been developed to try and explain the SEGR mechanism. One of the models which fits experimental data well is based on the concept of a conducting cylinder surrounding the track of the ionising particle.

The conducting pipe model is a simple semi-empirical model which hypothesises a linear dependence of inverse electric field on LET:

$$E_{CR} = \frac{E_0}{1 + L/B} \qquad \text{.....eq. (2.22).}$$

where E_{CR} is the critical field to rupture, E_o is the breakdown field, L is the particle LET and B is a fitting parameter which is technology dependent.

The increase in oxide electric field as technologies scale raises the concern that single event gate rupture (SEGR) could become a severe problem for advanced integrated circuits, such as those used in space applications [43].

Sexton *et al.* [44] have explored the dependence of SEGR on oxide thickness for oxide thicknesses between 6 nm and 18 nm. They report that the critical field, defined as the field at which gate rupture is observed at a given LET, increases with decreasing oxide thickness at any given LET. The thinnest oxides had critical fields above 7 MV/cm (LET = 80 MeV.cm^2/mg), indicating the potential for improved SEGR tolerance for advanced technologies. Massengill *et al.* report similar trends in their sub-5 nm oxides [45]. This increase in critical oxide field is attributed to reduced defect creation by hot carriers in the oxide.

Following their work on thin oxides, Sexton *et al.* have examined the impact of ion damage in 5 nm and 7 nm oxides to determine whether SEGR is a single ion effect [46]. They conclude that SEGR (identified by a large leakage current at low voltage levels) and precursor ion damage (noticeable by a gradual increase in leakage current at high voltage levels) are largely unrelated effects. This supports a single ion model for SEGR. They have observed that the capacitors with 5 nm oxides are unexpectedly difficult to rupture. In a few cases, an SEGR characteristic similar to the thicker 7 nm oxides is observed. However, in most cases no SEGR characteristic is observed.

A paper by Johnston *et al.* [47] addresses the issue of the dominance of soft, rather than hard, breakdown in oxides below 6 nm. Capacitors with oxide thicknesses of 4.5 nm and 7.5 nm have been studied. The results obtained show increasing critical field for decreasing oxide thicknesses, in agreement with the trend observed in [44]. The authors report that no true oxide shorts are observed in either oxides, but breakdown in the thinner oxides produces much lower current conditions. Localised regions within the oxide, which are more sensitive to the breakdown process, are taken to be the reason for the requirement of multiple hits before the onset of breakdown. The authors state that the ions have to strike a small critical region of the device when the applied field is high enough to cause breakdown in this region. The results are further evidence for a single

ion interaction mechanism, with no dependence on residual damage from previous ion strikes. Although the leakage currents observed are very small, they are large enough to cause circuit failure if they occur internally in small-area devices within VLSI circuits.

The work reported above has been carried out at high fields with relatively low ion fluences (maximum of 10^8 cm^{-2}) [44, 46, 47]. In a study of the cumulative damage produced by high radiation doses at low oxide fields during irradiation, Ceschia *et al.* [48] have observed soft breakdown phenomena at zero fields under irradiation with high LET ions. Radiation-induced leakage current (RILC), a manifestation of a trap assisted electron tunnelling conduction mechanism [49, 50], is observed for irradiations with low LET ions. Local oxide damage due to the overlap of different ion tracks, because of the high ion fluences (greater than 10^8 cm^{-2}) used, is quoted as the likely cause of the occurrence of radiation-induced soft breakdown (RSB). RILC and RSB have different field dependences, with RILC being a maximum at zero fields whilst RSB is a minimum at zero fields. The authors have observed a large increase in leakage current when RSB is activated, with an LET threshold for RSB activation in their 4 nm oxides of around 20 $MeV.cm^2.mg^{-1}$.

In some very rare cases, nuclear interactions with tungsten (used in circuits for the connection between silicon and metal layers) can lead to an LET of 80 $MeV.cm^2.mg^{-1}$ [51]. However, most of the knock-on atoms generated by the passage of charged particles in the CMS environment will have LETs rarely exceeding that of the Si ion. Fig. 2.17 shows that the maximum LET for a Si ion in silicon is $\sim 3.5 \times 10^4/(2.33 \times 10^3)$ = 15 $MeV.cm^2.mg^{-1}$.

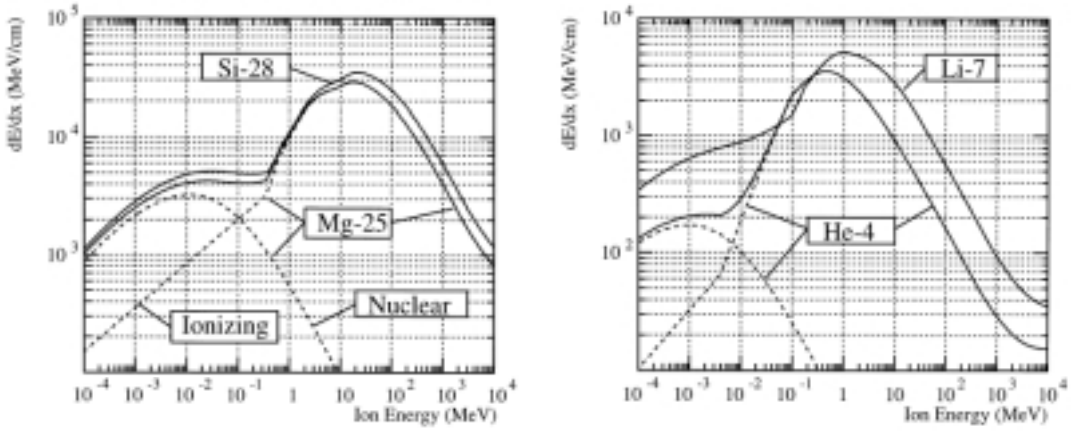


Figure 2.17: Energy loss of some ion species in silicon as a function of the kinetic energy of the ion, from [52].

Fig. 2.18 shows some results by previous workers along with lines representing the maximum electric field across the APV25 oxide and the maximum LET expected in the CMS radiation environment, indicating that the APV25 should be SEGR-free.

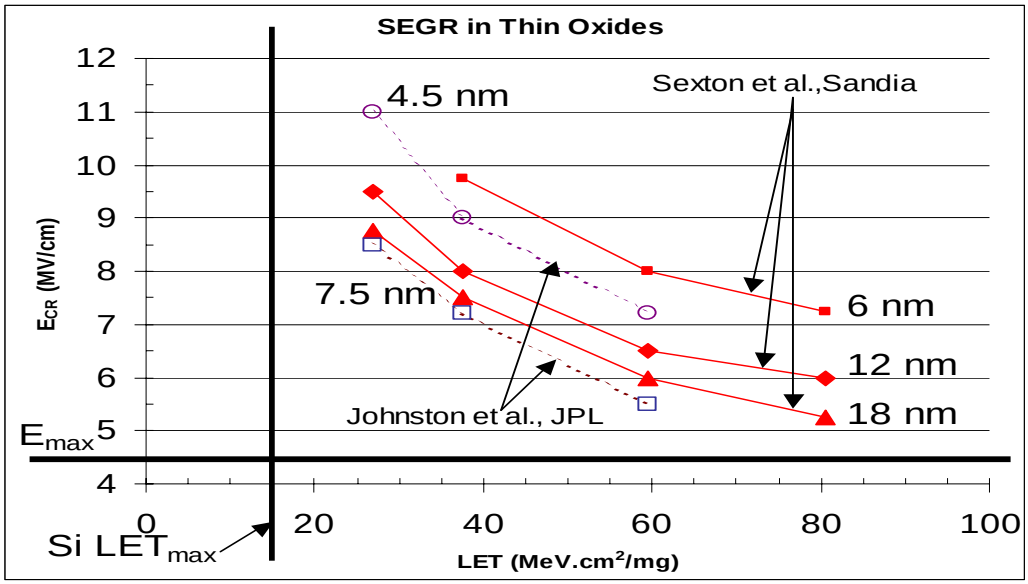


Figure 2.18: Critical electric field as a function of particle LET.

The horizontal bold solid line indicates the electric field across the oxides in an APV25. The vertical line indicates the maximum LET expected in the CMS Tracker.

2.2.2.3 Single Event Latchup (SEL)

Inherently, CMOS technologies consist of adjacent n- and p-type regions. A parasitic SCR (semiconductor controlled rectifier) can be formed by p-n-p-n structures which can be present in CMOS circuits. Under normal conditions, this parasitic device is switched off. It can be turned on by a triggering current such as that produced by ionising radiation. This is known as latchup and causes the circuit to turn fully on, creating a short across the device until it burns up or the power is cycled. Modern commercial CMOS processes are designed to be less susceptible to electrically-induced latchup from transients at input/ouput pins and power supply sequencing but are not necessarily immune to radiation-induced latchup.

The use of Shallow Trench Isolation (STI), thin epitaxial substrates and retrograde wells reduces latchup sensitivity in commercial technologies [53]. Theory predicts that the minimum triggering conditions should depend on the reciprocal of the epitaxial thickness and the thin (< 3 μm) epitaxial substrates of most commercial devices do not latch up for LET values of ~ 100 $MeV.cm^2.mg^{-1}$ [43].

The design rules that ensure the APV25 is total-dose radiation tolerant (enclosed NMOS transistor layout and p^+ guard rings which cut leakage current paths) provide additional

protection against SEL. Static and dynamic registers implemented with these design rules in a 0.25 μm technology did not latch up during irradiation tests up to the maximum LET of 89 MeV.cm^2/mg [54]. There is no evidence to suggest that SEL could be a problem for 0.25 μm technologies in the CMS radiation environment.

2.3 Temperature Effects

The APV25 chip has been extensively tested by research groups involved with the production and testing of components in the readout chain, mostly at room temperature. To limit radiation damage to the silicon microstrip detectors, the CMS Tracker will be operated at –10 ^{o}C. Although temperature effects are more pronounced for the silicon microstrip detectors and components such as the laser drivers, it is important to understand their consequences on the operation of the readout chip.

2.3.1 Temperature Dependence of Threshold Voltage

An expression for V_{th}, eq. (2.4), was given in section 2.1.3. It can be seen that the sensitive term is ϕ_F, which varies with temperature as eq. (2.6). The following expression is used for n_i:

$$n_i = \sqrt{N_C N_V}\, e^{\left(-E_g / 2kT\right)} \qquad \text{……..eq. (2.23).}$$

where N_C, N_V and E_g all change with temperature [11, 20, 55].

Fig. 2.19 shows the variation of threshold voltage with temperature for temperature-dependent values of n_i taken from [2.9].

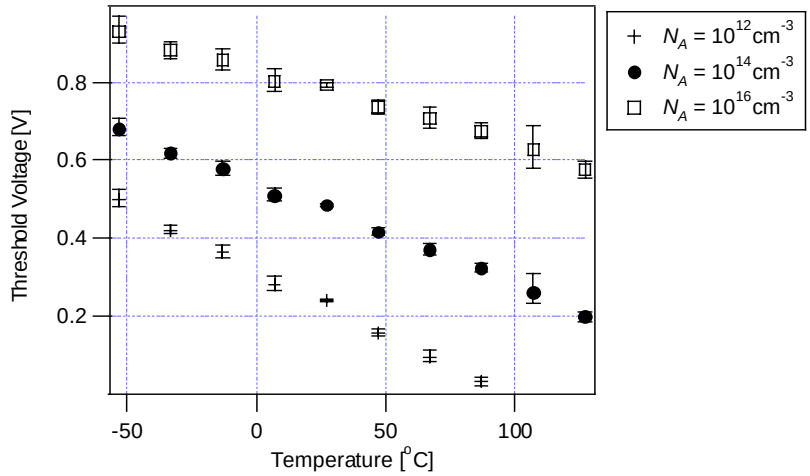


Figure 2.19: Variation of V_{th} with temperature for an NMOS transistor for different values of N_A.

As can be seen in Fig. 2.19, V_{th} decreases with increasing temperature for an NMOS transistor. V_{th} decreases in absolute value with increasing temperature for PMOS.

Usually, information on the processing details such as N_A is not available and the following expression is used to quantify the change of V_{th} with temperature [56]:

$$V_{th}(T) = V_{th}(T_0) - \alpha(T - T_0) \qquad \text{……..eq. (2.24).}$$

In eq. (2.24), $\alpha \approx 1\text{mV/}^{\text{o}}\text{C}$ but is process-dependent and has to be determined, for example by measuring individual transistors on test structures manufactured alongside chips on a wafer.

2.3.2 Temperature Dependence of Mobility

In Section 2.1.1, mobility was seen to be related to lattice scattering and impurity scattering. Above absolute zero, lattice atoms are subjected to thermal vibrations which are responsible for lattice scattering. Thermal vibrations increase with increasing temperature and lattice scattering dominates at high temperatures leading to a decrease in mobility with increasing temperature. The mobility term due to lattice scattering, μ_L, decreases in proportion to $T^{-3/2}$[57].

Ionised impurities are responsible for impurity scattering, where a charge carrier is deflected due to the Coulomb interaction. This deflection is less pronounced the higher the temperature since carriers move faster and spend less time near impurities. Impurity scattering is therefore less significant at higher temperatures. The mobility term due to impurity scattering, μ_I, varies as $T^{3/2}/N_T$, where N_T is the total impurity concentration [58]. The temperature dependence of mobility is represented by the following expression:

$$\mu_n(T) = \mu_n(T_0)\left(\frac{T}{T_0}\right)^X \qquad \text{…....eq. (2.25).}$$

where the factor X takes into account the compensating contributions of lattice and impurity scattering. Typically $X \approx -1.5$ but it is process-dependent and must be derived from data.

2.3.3 Temperature Dependence of Transconductance and Noise

Transconductance and noise are related to mobility by the following expressions:

$$g_m(T) \propto \mu_n(T) \qquad \text{…....eq. (2.26).}$$

$$S_V \propto \sqrt{\frac{T}{g_m}} \qquad \text{…….eq. (2.27).}$$

Eq. (2.27) suggests that the noise should decrease with decreasing temperature.

2.4 Summary

Two major types of radiation damage affect CMOS processes: total dose ionising radiation effects and single event effects (SEU, SEL, SEGR). The current trend in device scaling introduces inherent total dose radiation hardness to commercial CMOS technologies. In particular, tunnelling into the thin gate oxide of the latest processes neutralises the oxide trapped charge induced by ionising radiation. Leakage current paths between drain and source and between adjacent transistors can be reduced through the adoption of special design rules such as enclosed NMOS transistor layouts and the extensive use of p^+ guard rings. These design rules along with common features of modern CMOS processes such as shallow trench isolation, thin epitaxial substrates and retrograde wells ensure that SEL sensitivity is not a concern for CMS electronics. SEGR is a problem which usually affects the operation of power MOSFETs where the electric fields across the oxide are high. Experimental data suggest that SEGR susceptibility actually decreases with decreasing oxide thickness and that this damage mechanism should not pose a threat to the operation of the 0.25 μm CMOS process. SEUs will occur in many of the CMS electronics components and must be accounted for in the final systems. One important parameter for SEUs is the rate at which they occur since this determines the reloading or resetting of components that are affected.

The need to monitor the change in the electrical characteristics of MOS devices with temperature was identified. A crucial parameter in the design of the CMS silicon microstrip tracker is the signal-to-noise ratio. This is expected to improve in the CMS environment (compared with room temperature measurements) since the APV25 chip will be operated at –10 ^{o}C.

Chapter 3
CMS Front-End Electronics

CMS electronics systems form a federation of sub-projects: pixel tracker, silicon strip tracker, electromagnetic calorimeter, hadron calorimeter, muon barrel drift tubes, muon endcap cathode strip chambers and resistive plate chambers [59]. They amplify, store and digitise detector signals and in addition to radiation tolerance, they must at various levels meet the requirements to minimise noise, power consumption and cost, which leads to the adoption of a variety of systems. For example, tracking detector electronics have to tolerate high levels of radiation but, because of the high particle rates, they are not involved in the triggering process. This is carried out by the calorimeter and muon systems where timing and synchronisation are major issues.

Radiation tolerant, custom-made ASICs are planned for the high levels of radiation in the Tracker and some of the calorimetry whereas the low radiation environment of the muon systems permits the use of commercial components.

All systems will be subjected to radiation, from the innermost layers of the pixel tracker with total doses of 40 Mrad and charged hadron fluences of 8×10^{14} cm^{-2} to the cavern walls with total doses of a few krad and neutron fluences of $\sim 10^{11}$ cm^{-2} over the 10 year lifetime of the experiment (5×10^{7} s of operation at high luminosity) [60]. Radiation testing is therefore a feature of the evaluation of every component for use in CMS.

3.1 The Pixel Tracker

The CMS pixel detector provides high-resolution 3-D space points required for the track pattern recognition and for b-tagging. It consists of three barrel layers and two disks at each end. The barrels are 53 cm long and cover an area of about 0.8 m^2 with roughly 800 modules. The 96 modules of the end disks cover an area of around 0.28 m^2. The readout of the entire pixel detector is carried out by ~ 16 000 readout chips (ROCs), with 16 ROCs bump-bonded to each Si sensor [61].

3.1.1 Pixel Readout Chip

Each sensor pixel is connected to its own readout circuit (Pixel Unit Cell, PUC) on the ROC, which has an array of 52×53 PUCs organised in 26 double columns.

The PUCs are subdivided geometrically into an analogue block and a digital readout block, Fig. 3.1. The analogue block has an amplifier, shaper and comparator. The

analogue input can come either from the sensor pixel during normal operation or from an internal calibration pulse for testing purposes. It is amplified, shaped and fed to a comparator stage that has a global threshold. Each PUC is equiped with a 4-bit register. Three bits are used to fine-tune the local comparator threshold, which is required because of channel-to-channel variations, and the other bit is used to switch off the discriminator in the case of noisy pixels.

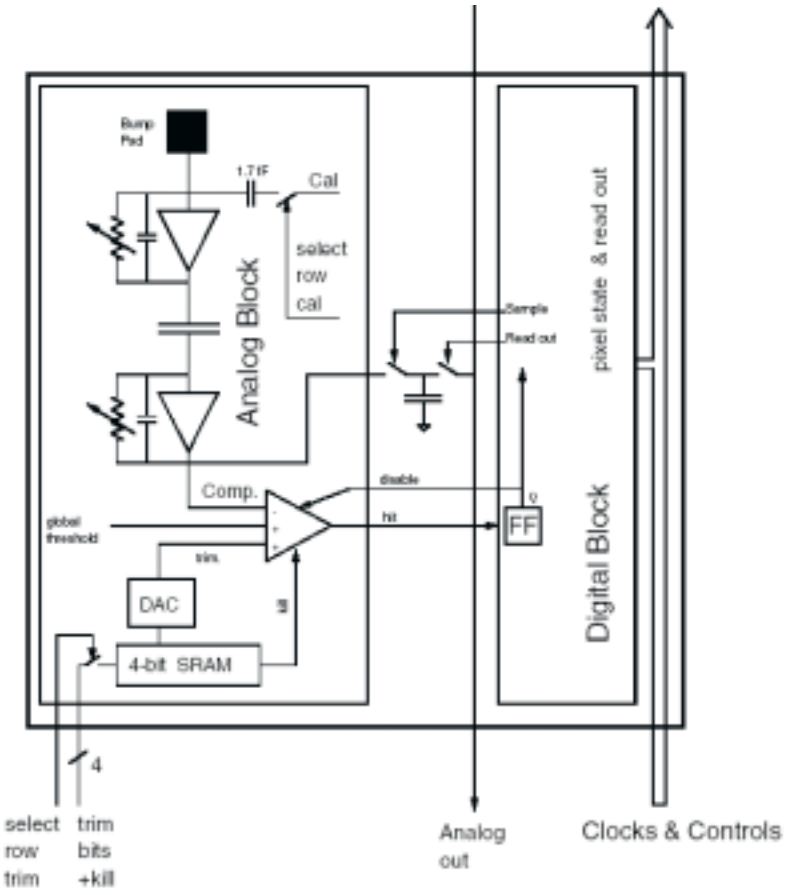


Figure 3.1: Schematic diagram of a pixel unit cell (PUC).

In addition to the PUCs, each ROC has a column periphery, a time-stamp and readout bus block and a control and interface block. The column periphery organises the pixel readout and takes care of time-stamp and trigger verification. The time-stamp & readout bus block contains two bunch-crossing counters, and the necessary buses for the distribution of their codes to the time-stamp buffers in all columns. It also contains the readout logic for collecting all hits in a readout cycle. All control voltages and currents are generated by DACs in the control & interface block.

3.1.2 Readout Scheme

When pixels are hit, they notify the column periphery. The data are then read out in two stages. During the first stage, which runs at 40 MHz, the time information is stored in

the time-stamp buffer and the address and the analogue signal of each hit pixel is transferred to the column data buffer located in the column periphery. Data have to be stored for 3.2 μs while waiting for the Level-1 (L1) trigger decision. The data confirmed by the L1 trigger are saved for the second stage of the readout while the unconfirmed data are eventually overwritten. During the second stage, the triggered data are flushed from each double column and sent on optical links to the Front End Driver (FED) modules 100 m away from the detector.

3.1.3 Status of Pixel Electronics

SEU investigations have been carried out on prototype pixel readout chips fabricated in two different radiation-hard SOI technologies (DMILL 0.8 μm and Honeywell RICMOS 0.8 μm) at the 200 MeV pion beam at the Paul Scherrer Institute (PSI) where the beam intensity was 10^9 pion.s^{-1} [62, 63, 64, 65]. These have highlighted the need either for changes to the design of the chip, such as larger transistors to increase the critical charge for SEU or logic triplication, or the adoption of reset mechanisms to periodically refresh pixel thresholds.

PSI 43, the first complete version of the chip fabricated in the DMILL process, has been found to be fully operational under laboratory tests and during exposure to a 300 MeV/c pion beam [66]. The SEU cross-section has been measured to be 1.5×10^{-14} cm^2, for the individual pixel registers. A translation of the chip into a 0.25 μm technology is planned which offers the possibility of a further pitch reduction from 150×150 μm to 100×150 μm. As the Lorentz angle and hit multiplicity tend to decrease after irradiation-induced type inversion in the sensor material, the smaller pitch provides some safety margin to conserve the resolution in the specified range. The bump bonding technology to connect sensor and readout chips has been successfully mastered at the PSI.

3.2 Silicon Microstrip Tracker

The silicon microstrip tracker readout system consists of approximately 10 million detector channels and, at expected track occupancies, will generate a large proportion of the final data volume at CMS.

Analogue readout has been adopted for the CMS Tracker. This choice is driven by the reduction of the front-end chip complexity, power dissipation and potentially better position resolution through charge sharing between strips [67]. A schematic diagram of the proposed readout electronics system for the silicon strip detectors is shown in

Fig. 3.2. Table 3.1 lists the Tracker readout and control components. The APV25 front-end chip was described in Chapter 1 and will not be discussed here.

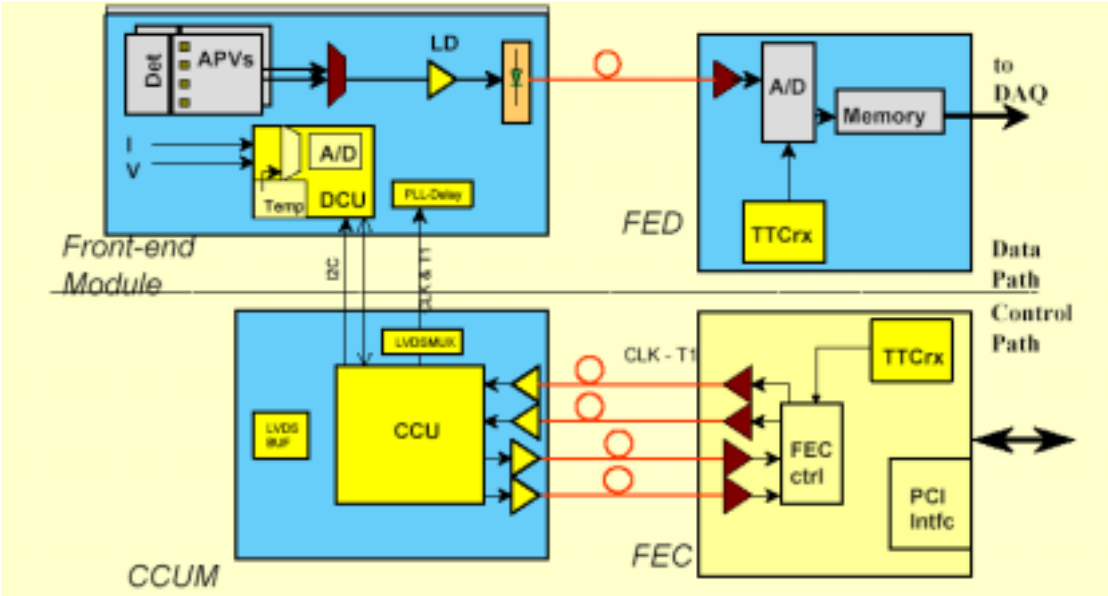


Figure 3.2: Schematic diagram of the CMS SST readout and control system.

Table 3.1: Summary of the components used in the system with their functions. The numbers listed are approximations based on the Technical Design Report [2].

Component	Function	Number (Approx.)
APV25	128-channel silicon front-end chip	90 k
APVMUX	2 APV:1 optical link multiplexer	45 k
CCU25	Clock, trigger and command distribution	2 k
PLL25	Clock recovery and programmable delay	30 k
DCU25	Interface to monitor slowly varying parameters	25 k
LLD25 Laser driver	Bias and modulate laser current (4 channel)	15 k
Laser diode	Electrical-optical converter	50 k
Photodiode	Optical-electrical converter	50 k
Analogue receiver	Amplifier for analogue signals	45 k
Digital receiver	Amplifier for digital control, clock and trigger	2→5 k
LVDS Tx/Rx	Converts digital electrical levels to LVDS standard	3 k
FEC	Distribution of clock, trigger and control data and reception of monitoring data, via optical links	20→100
FED	Reception and processing of analogue data and interface to CMS DAQ	550

The tracking system experiences one of the most severe radiation environments in the whole of CMS with 10-year doses and fluences up to about 15 Mrad and 3×10^{14} chargedhadrons.cm^{-2} at the innermost microstrips and ~1 Mrad and 10^{13} neutrons.cm^{-2} for the outermost detectors.

3.2.1 Front-End Hybrids

The front-end hybrids house a varying number of APV25 chips, connections and decoupling capacitors for the power and detector bias lines, miniature twisted-pair interfaces for the input and output signals, the APVMUX, PLL and DCU chips. Most of the power will be dissipated in the APV chips and the hybrids must ensure efficient heat transfer to the cooling system.

3.2.2 Optical Links

Optical data transmission has been chosen for the Tracker because of its small contribution to the material budget, high data transfer rates and immunity to electrical interference.

The ~ 50 000 uni-directional analogue links are based on edge-emitting laser transmitters and p-i-n photodiode receivers operating at a wavelength of 1310 nm [68]. In every single-mode fibre, 256 electrical channels are time-multiplexed at a rate of 40 MSamples/s. The individual fibres originating from the transmitters are fanned in, first to a 12-way ribbon, and then to an 8-ribbon cable carrying 96 fibres away from the detector to the counting room. The total length of the link is approximately 100m of which 10m is within the high radiation environment.

The ~ 1000 bi-directional digital links used for control and timing distribution are based on almost identical components as the analogue readout system, but with a different modularity. The transceiver modules placed inside the detector include radiation resistant photodiodes and discriminating amplifiers, whereas those located in the counting room are based on standard commercial components. The optical receiver has been fabricated in a commercial 0.25 μm CMOS process and its measured performance is well within specifications: a dynamic range of more than 30 dB and 80 MHz bandwidth [69]. The leakage current control feedback loop works beyond the required 100 μA to compensate the radiation-induced photodiode leakage current.

Semiconductor lasers are only sensitive to radiation-induced displacement damage. The damage mechanism originates in the creation of non-radiative recombination centres in the active volume of the laser which reduce the optical gain. Creation of traps causes very little degradation since they have to be at the right energy level to interfere with laser generation and the pre-irradiation defect density is high. Minimising the active volume can further reduce degradation. Modern lasers are deliberately constructed with a small active volume to increase the laser gain by optimising the overlap of carriers with the optical field in the cavity, to minimise electrical power requirements and to

maximise efficiency. They are therefore less sensitive to radiation damage. A consequence of displacement damage is a shift in laser threshold current corresponding to a shift in the DC bias point. It has to be compensated by the driving electronics to avoid falling into the sub-threshold regime of the laser. P-i-n photodiodes are also sensitive to displacement damage but the measured effect is very small.

Ionisation is the dominant damage source in optical fibres subject to irradiation. It has been demonstrated that the radiation-induced loss in the most exposed section of fibres will be negligible throughout the lifetime of the CMS experiment [70].

3.2.3 Front-End Driver (FED)

The optical fibres carrying the analogue data from the APV chips connect to the Front End Driver (FED) digitising boards housed in the underground counting room. Opto-receiver packages consisting of 12 channels of p-i-n diodes perform the optical-to-electrical conversion. The FED receives 96 channels, each of which is digitised by a 40 MHz, 10-bit commercial ADC and digitally processed before transmission to the next level of the CMS data acquisition system [71], Fig. 3.3. The post-ADC processing of an APV frame is performed by Field Programmable Gate Arrays (FPGAs) and consists of synchronisation, pedestal correction, re-ordering, common mode correction and cluster-finding.

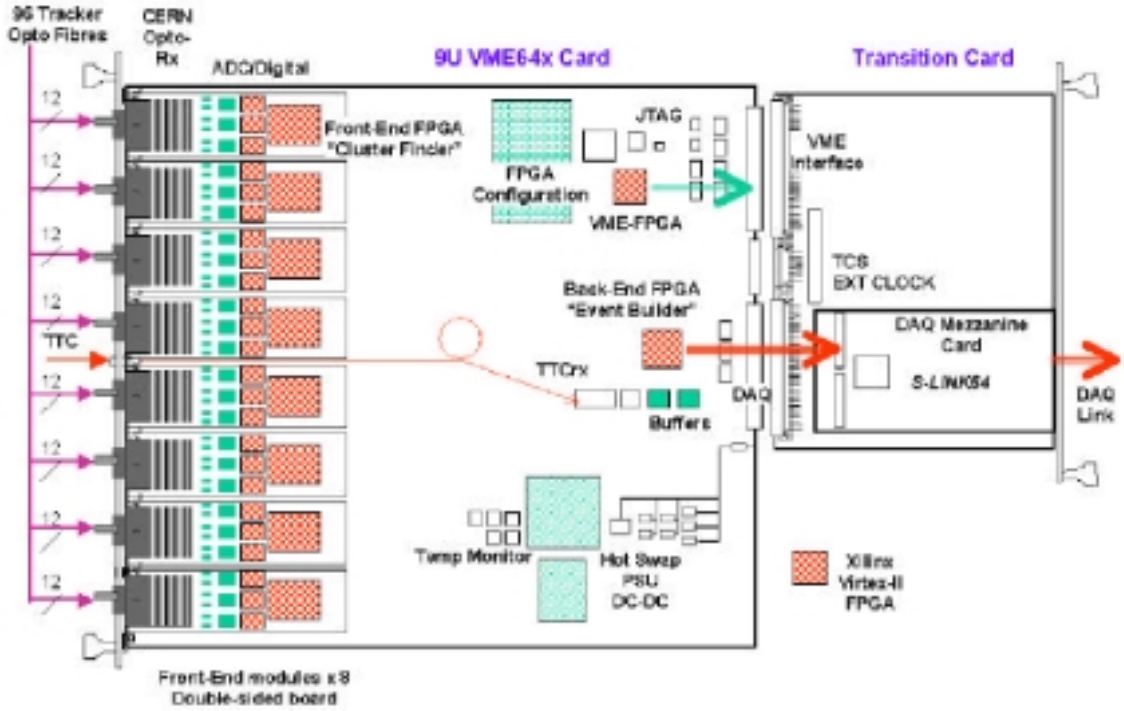


Figure 3.3: The FED 9U VME layout and its transition card.

3.2.4 Control System

A total of about 3 Mbytes of parameter data is contained in the front-ends [72]. This has to be distributed and monitored by the control system and any errors have to be corrected. The parameter download frequency has not yet been defined.

The Tracker control system consists basically of three main functional blocks:

- a Front End Controller (FEC) card located in the control room manages the communication network and interfaces to the CMS slow control system;
- a communication network based on a simple token-ring architecture provides a link between control room and embedded electronics;
- a Communication and Control Unit (CCU) provides a link between the communication network and the front-end ASICs. A Phase Locked Loop (PLL) ASIC is responsible for recovery and distribution of trigger and clock signals.

The ring architecture through which it is possible to connect a number of CCUs serially was designed to minimise costs. The final Tracker will have groupings of 10 to 20 modules on each CCU, 1 to 4 CCUs per ring and 2 rings per FEC.

The components exposed to the high radiation environment are designed in the 0.25 μm CMOS process and in addition to the design rules which protect against total dose effects and latchup, they have the following SEU redundancy features [73]:

- CCU25, 3× logic + voting in node controller, parity on all registers for the data path, several status SEU registers and counters, auto-reset and one hot-FSM,
- PLL25, 3× redundancy on 99 % of chip,
- DCU25, 3× redundancy on I^2C interface,
- LLD25 (Linear Laser Driver), 3× redundancy on I^2C interface.

3.2.5 Status of Tracker Electronics

Many of the optical link components have been irradiated with neutrons to fluences over 10^{14} cm^{-2} and with gammas to total doses above 20 Mrad [70, 74, 75, 76, 77]. Thermally accelerated ageing tests suggest that the lasers and p-i-n photodiodes have a sufficiently long lifetime to operate without failure for well in excess of 10 years inside CMS [77]. A test card housing CCUs, LDs, DCUs, PLL25s and LVDSMUXs has been successfully operated in a 200 MeV proton beam at the PSI in December 2001. SEU tests of the CCU25 have been carried out at the PSI 300 MeV proton beam (3×10^8 $p.s^{-1}$) where the error rate was 4.58 SEU/chip/hour [78]. This translates to a worst-case rate of 84 SEU/hour for all 2000 CCU25s at LHC.

3.3 Crystal Electromagnetic Calorimeter (ECAL)

The CMS ECAL [79] will consist of 82 728 crystals of lead tungstate ($PbWO_4$) arranged in a barrel (61 200 crystals) and two endcaps (10 764 crystals each).

Readout electronics must be capable of coping with energies of up to ~ 2 TeV from the decay of a massive $Z' \rightarrow e^+e^-$. For smaller signals, the most stringent performance requirements are imposed by the $H \rightarrow \gamma\gamma$ decay, which is also the benchmark process for performance evaluation. Observing this decay channel requires excellent resolution for energies up to ~100 GeV.

The radiation environment in the endcap ECAL is defined by total dose levels as high as 2 Mrad and a neutron fluence of up to 5×10^{14} cm^{-2}.

3.3.1 Readout Chain

The original system for the ECAL 'light-to-light' readout chain is shown in Fig. 3.4. It consists of two distinct parts, one 'on detector' Very Front End (VFE) and the digital readout and processing part placed in the counting room [80].

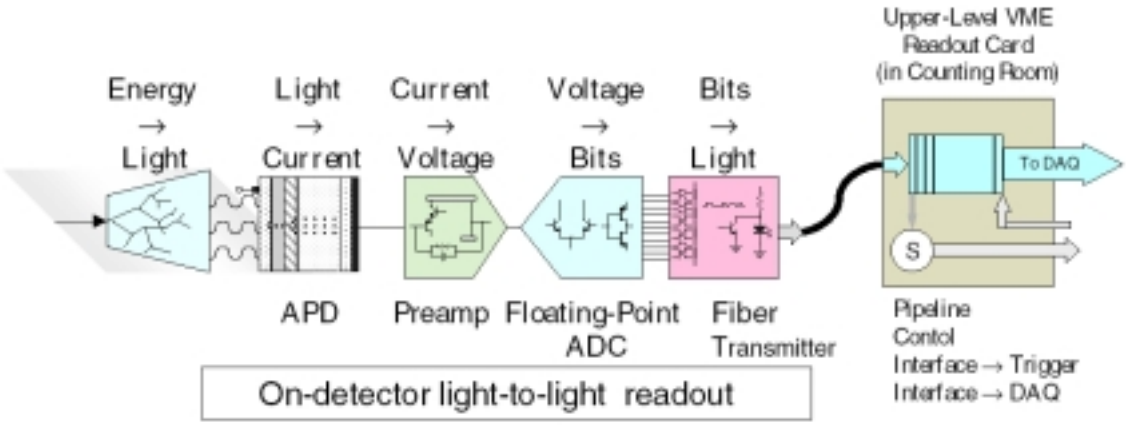


Figure 3.4: Original scheme for the ECAL readout chain.

The readout chain begins when scintillation light from the $PbWO_4$ crystal is converted into a photocurrent by the photodetector. The photocurrent is then converted into a voltage by a preamplifier. The amplified signal is digitised by a floating-point ADC. A high-speed optical link transports the digitised data off the detector to the counting room [81]. With this layout, digital sums representing the energy deposit in a trigger tower must be presented to the trigger system every 25 ns.

The original system described above was very flexible but most of the data moved 'off detector' with one optical link per crystal was not eventually used for physics. An alternative is a system that generates trigger primitives at the detector and stores all the

data until a Level-1 trigger accept is received. Its advantages are a reduction in the number of data links (from ~ 91000 to ~ 12000) and in the complexity of the 'off detector' electronics, reducing the overall cost of the ECAL. The new scheme, based on a readout unit of 25 crystals, has been proposed with the following features [82]:

- A Very Front-End (VFE) electronics board, with the Floating Point PreAmplifier (FPPA) and ADC chips,
- A Front-End (FE) electronics board, with the Fenix (stores data during the L1 trigger latency, generates trigger primitives), GOL (transmits data to 'off detector electronics'), Tracker Clock and Control and voltage regulator chips.
- A reduced number of data and control links, using the Tracker link technology,
- A reduced number of 'off detector' components.

3.3.1.1 Floating Point PreAmplifier (FPPA)

The FPPA chip performs the internal pulse shaping and contains a preamplifier, sample/hold and gain multiplexing circuits [83]. A multi-gain switching topology is used to compress the 16-bit range of the crystals into the 12-bit digital format [84]. The preamplifier voltage is amplified by four clamping amplifiers with gains of 1, 5, 9, or 33. Voltage comparators and digital logic in the circuit then determine which of the four voltage samples is the largest below a certain threshold. The FPPA chip designed for the initial readout scheme is implemented in a radiation-hardened technology.

3.3.1.2 ADC

The voltage from the comparator stage is multiplexed and digitised by a 12-bit ADC. The output data consist of a floating point representation of the voltage in the form

G_2	G_1	G_0	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

where G_2 is a data type flag, $[G_1..G_0]$ is a 2-bit code representing the gain range used (1, 5, 9, 33) and $[D_{11}..D_0]$ is the 12-bit ADC mantissa. In this way, the 12-bit ADC covers the full 16-bit dynamic range. The Analogue Devices AD9042 12-bit, 40 MHz ADC was chosen for the initial readout scheme.

3.3.2 Status of ECAL Electronics

The only change that has been observed following exposure of the FPPA to 10^{13} protons.cm^{-2}(equivalent to roughly 1 Mrad and 2×10^{13} 1MeVneutrons.cm^{-2}) is a 3 % drop in the gain [85]. The implementation of the new readout architecture in a 0.25 μm CMOS technology is currently under design (including FPPA, ADC, Fenix and GOL chips) and prototypes will be available for testing in 2003.

3.4 Preshower

Background reduction in the $H \rightarrow \gamma\gamma$ search requires good π^0/γ separation. For a Higgs mass of 120 GeV, the π^0s have a transverse energy of the order of 60 GeV leading to a separation between the 2 photons arising from the π^0 decay of about 0.8 cm in the barrel region but only a few mm in the endcaps [86]. Whilst π^0 rejection can be performed by the ECAL in the barrel region, the fine granularity of a preshower detector is required in front of the endcap ECAL to separate single showers from overlaps of two close showers.

The requirements of 5 % charge measurement and 1-to-400 MIP dynamic range distinguish this silicon detector from the Tracker. The preshower is formed with two orthogonal planes of silicon detectors each divided into 32 strips with a pitch of 1.9 mm. Each plane is preceded by a thin lead absorber. A total of 4 304 detectors will be installed, corresponding to 137 728 channels.

At η=2.6, the integrated radiation after 10 years of LHC running will be the equivalent of 2×10^{14} neutrons.cm^{-2} and 6 Mrad. The leakage current increases with radiation and the detectors have to be maintained at –5 ^{o}C to keep it below 20 μA per strip.

3.4.1 Preshower Front-End Electronics

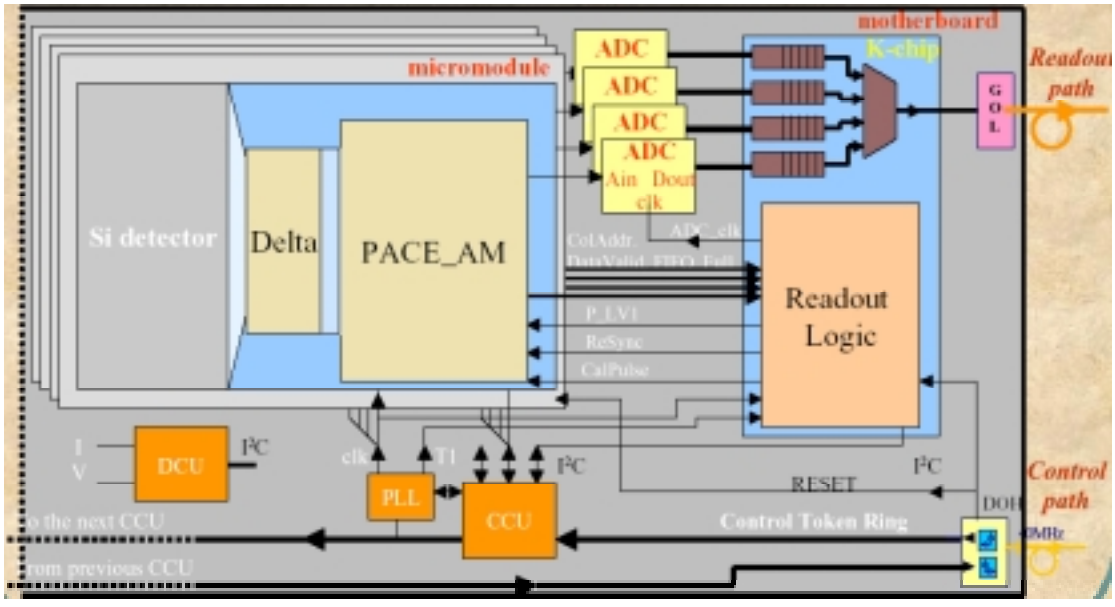


Figure 3.5: Preshower electronics, from [87].

Fig. 3.5 illustrates the electronics used in the Preshower. The Preshower front-end, PACE 2, consists of two chips, Delta and PACE_AM [88].

Delta consists of three blocks, the Delta preamplifier, a leakage current compensation unit (LCC) and a switched gain shaper [89]. The LCC monitors and subtracts the radiation-induced detector leakage current from the DC coupled input.

The PACE_AM analogue memory stores the charge of each input channel at a frequency of 40 MHz in 160 memory slices.

The analogue data from each PACE 2 assembly is fed to an ADC at 20 MHz. The ADC is the same as that used in the ECAL, the AD9042. The output of 4 ADCs goes into a digital data concentrator chip, the K chip, before an optical exit from the experiment. The optical link, CCU, PLL and DCU chips will be taken from the Tracker.

3.4.2 Status of Preshower Electronics

The PACE 2 chips, Delta and PACE_AM, have been manufactured in the BiCMOS DMILL technology. Delta is radiation tolerant to 4×10^{13} neutrons.cm^{-2} and to 10 Mrad(Si). Further irradiation tests are necessary to a fluence of 2×10^{14} neutrons.cm^{-2}. A complete redesign of PACE 2 called PACE 3 is currently underway in a 0.25 μm technology. A prototype SRAM from the K chip has been manufactured in a 0.25 μm technology and tested to 10 Mrad. No degradation in performance has been observed.

3.5 Hadron Calorimeter (HCAL)

The hadron calorimeter measures the energy and direction of particle jets and missing transverse energy flow and helps identify electrons, muons and photons. It is a sampling calorimeter consisting of an active material inserted between copper absorber plates [90]. Three main subsystems of the hadron calorimeter can be distinguished: the barrel, the endcap and the forward calorimeters. The active elements of the barrel and endcap hadron calorimeter are 4 mm thick plastic scintillator tiles read out using wavelength-shifting (WLS) plastic fibres. The active medium in the forward calorimeter is provided by quartz fibres sensing Cerenkov light from electromagnetic showers.

HCAL detector electronics will be subjected to maximum total doses of 190 rad and a neutron flux of 3.1×10^{11} n.cm^{-2}.

3.5.1 HCAL Readout

The HCAL readout chain begins with the photodetectors coupled to the active media. The photodetectors in the barrel and endcap system are hybrid photodiodes (HPDs) [91, 92], those in the forward region are photomultiplier tubes (PMTs).

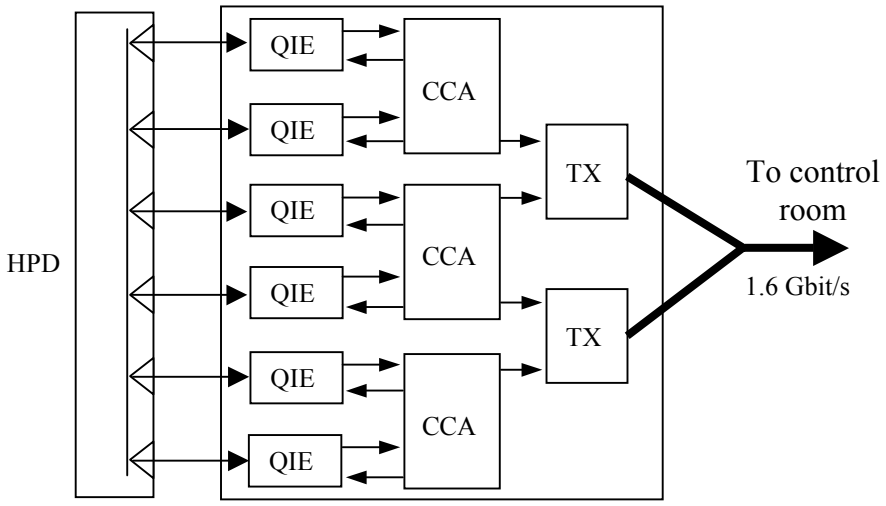


Figure 3.6: HCAL front-end electronics. TX represents the Gigabit Optical Link and the VCSEL.

The HCAL readout scheme is shown in Fig. 3.6. A multi-range current splitter and gated integrator, the QIE (Q for charge, I for integrating, and E for range encoding) ASIC, performs the analogue signal conditioning and digitisation. In the QIE the input current is simultaneously integrated on all ranges and comparators are used to select the lowest range that is not at full scale. The digitised output is in an 8-bit format with a 3-bit range and 5-bit amplitude.

The CCA (Channel Control ASIC) performs functions such as supplying clocks to QIEs, data formatting and synchronisation. The GOL (Gigabit Optical Link) performs a parallel-to-serial conversion and drives the data to a commercial Vertical Cavity Surface Emitting Laser (VCSEL). The data is then optically transmitted out of the radiation area at 1.6 Gbit/s to the HCAL trigger and data acquisition boards.

The QIE is fabricated in the Austria Micro Systems (AMS) 0.8 μm BiCMOS process (proven to be rad-tolerant to 10 Mrad) whilst the CCA is fabricated in the Agilent 0.5 μm CMOS process.

3.5.2 Status of HCAL Electronics

Estimates of the HCAL radiation environment have uncertainties of the order of a factor of three and for this reason, most HCAL front-end electronics components have been tested for radiation tolerance to 4×10^{11} n.cm^{-2} and 1 krad [93]. These tests demonstrate SEL immunity for at least 4 years of operation. The measured SEU rate was 0.1 – 0.01 SEU/chip/year.

3.6 Muon Endcap Cathode Strip Chambers (CSC)

The front-end electronics for the CMS Endcap Muon System [94] has to:

- acquire precise muon position and timing information for offline analysis;
- generate muon trigger primitives for the L1 trigger system.

In a CSC layer, the anode wires are in the azimuthal direction and provide precise timing measurements. The cathode strips are in the radial direction and measure the azimuthal coordinate of a hit. Overall, the endcap CSC system consists of 540 six-plane trapezoidal chambers, each with ~1000 readout channels. Electronics in the innermost CSCs are subjected to a neutron fluence of 8.7×10^{11} cm^{-2} and a total dose of 1.8 krad.

3.6.1 Overview of CSC Electronics

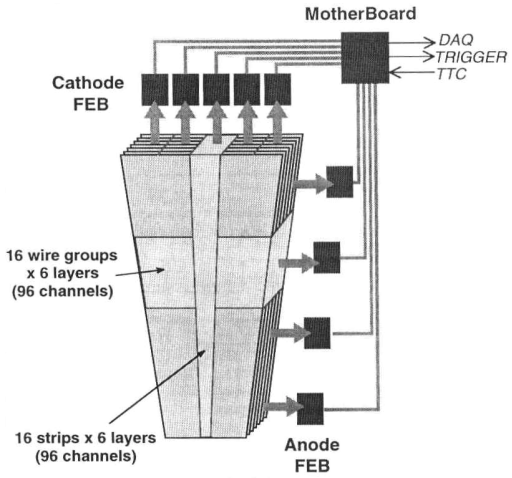


Figure 3.7: Organisation of the CSC front-end electronics.

Cathode and anode front-end boards (FEB) are mounted directly on the CSC modules, Fig. 3.7. Because both types of FEBs are similar (the main difference is the peaking time of the shaped pulse, 30 ns for the anode readout compared with 100 ns for the cathode readout), only the cathode front-end board (CFEB) is described here.

Each CFEB is designed to read out a tower consisting of 16 neighboring strips per layer by 6 layers deep, corresponding to a total of 96 channels. The input signals from each of the strips are sent into 16-channel amplifier-shaper ASICs. Each input signal is amplified and shaped into voltage pulses. The shaper produces two outputs. One is connected to the trigger path whose main components are a Comparator Network and a Local Charge Track (LCT) processor. The other output is connected to a Switched Capacitor Array (SCA) which holds voltage levels sampled every 50 ns during the L1 trigger latency. When trigger conditions are met, the SCA output is digitised by a 12-bit

ADC (to cope with a dynamic range of 4000) operating at 20 MHz, multiplexed and sent to the DAQ system.

FEB data are sent to a readout motherboard (MB) mounted on the chamber. The MB sends the readout and trigger data to the central DAQ system and the L1 trigger system. It receives trigger, timing and control (TTC) signals and distributes them to the FEBs.

The preamplifier-shaper ASIC (Buckeye) and the SCA ASIC are 0.8 μm CMOS chips. Digitisation is performed by the Analog Device AD9225. Readout control, multiplexing and clock generation (for SCA and ADC) are all performed by FPGAs.

3.6.2 Status of CSC Electronics

Final prototypes of the on-board cards have been fully tested for functionality and integration onto the chamber, including cooling. The CFEB has been irradiated with 63 MeV protons and 1 MeV neutrons [95]. The CMOS components have survived total doses of 10 krad with no deterioration of analogue performance. The FPGAs have survived beyond total doses of 30 krad. No latchup has been detected for fluences of up to 2×10^{12} protons.cm^{-2}. The SEU rate for the Xilinx Virtex XCV50 on the CFEB for all boards is 1 every 600 s [96]. It is 1 in 240 s for all XILINX Virtex XCV1000E on the ALCT. To recover from SEUs, the FPGAs have to be reloaded periodically. The reloading time is around 40 ms.

3.7 Muon Barrel Drift Tube Chambers (DT)

The CMS muon barrel system consists of four stations, MB1-MB4, integrated in the return yoke of the magnet and instrumented with 250 chambers, which account for a total of ~ 200000 channels [97]. The basic sensitive element of the chambers is a drift cell with a pitch of 40 mm by 13 mm and approximately 400 ns maximum drift time. The chambers are made of three independent subunits, or superlayers (SL). Within an SL, the four layers of drift tubes are staggered by half a cell, making it possible to use the correlation of the drift times in the different planes to compute the coordinate and angle of the crossing muon tracks without any external time tag.

Radiation levels in the DT area are relatively low, with a maximum total dose of 12 rad and a neutron fluence of 2.3×10^{10} cm^{-2}.

3.7.1 Front-End ASIC and Readout Electronics

Front-end electronics amplify the signals coming from the detector, compare them in the fastest way with a threshold and send the result to the trigger and readout chains.

The front-end ASIC (MAD) preamplifier is of the charge sensitive input type with a designed decay time constant of 50 ns and is mounted inside the DT chamber gas volume to minimise electronics noise. This is required to allow operation of the drift tubes at low gain, which is advisable for reasons of reliability and chamber lifetime.

The remaining local electronics (TDCs and trigger track element processors) are located on readout boards (ROBs) mounted in custom minicrates on the chamber structure outside the gas volume.

Most of the trigger electronics is located 90 m away, in the counting room, because of the radiation levels, access and maintenance [98]. A local Bunch and Track Identifier (BTI) identifies tracks giving signals in at least three out of four drift tube layers and assigns the correct bunch crossing to which a detected muon belongs. It is required because the maximum drift time of the particles in the DTs of 400 ns is much longer than the 25 ns spacing between two consecutive bunch crossings. BTIs have a time resolution of ~ 3 ns, which is fast enough to be used in the L1 trigger [99].

3.7.2 Status of DT Electronics

The BTI and part of the trigger chain are fully prototyped and were reviewed in the September 2000 ESR. The front-end (MAD) ASIC and high voltage distribution/signal pick-off cards have been approved and are in bulk production. HPTDCs have been developed at CERN in a 0.25 μm technology. Good results were obtained when the front-end and readout electronics were exposed to a muon test beam in July 1999 [100]. The SEU rate was estimated to be less than one per day for all components on the readout boards following irradiation with protons to a fluence of $5 \times 10^{10} \mathrm{cm}^{-2}$ [101].

3.8 Muon Resistive Plate Chambers (RPC)

CMS has added planes of resistive plate chambers (RPCs) in both the barrel and the endcaps to provide an additional, complementary trigger. RPCs are gaseous parallel-plate chambers that combine a reasonable level of spatial resolution with excellent time resolution (~ 3 ns), comparable to that of scintillators. In the muon system, these chambers will cover roughly the same area as the DTs and CSCs but will provide a faster timing signal and have a different sensitivity to background. Trigger signals coming from the DTs, CSCs and RPCs will proceed in parallel until reaching the level of the global trigger logic.

The key parameters for the RPCs are time resolution, efficiency, and rate capability for the muon trigger. The response of the RPCs should be fast and uniform to manage the 25 ns bunch crossing interval.

Each RPC strip behaves like a transmission line since the propagation velocity is ~ 5.5 ns/m, longer than the ~ 1 ns rise time of the induced signal. It has to be properly terminated at both ends and this is achieved by the input resistance of the chip at one end and by a resistor at the other end. The total charge induced on a strip ranges from ~ 20 fC to more than 20 pC but such a wide linear dynamic range is not required. The threshold can be set at 20 fC with a $\sigma_{noise} < 4$ fC without loss of detector efficiency.

The radiation environment in the muon barrel region is principally composed of neutrons generated from hadronic interactions in the calorimeters or from the interaction of the primary proton beam with the beam pipe and collimators, and gammas originating from neutron capture in the surrounding material. The neutron fluence will be of the order of 10^{10} cm^{-2} in the barrel and 10^{11} cm^{2} in the endcaps [102]. The total dose in the endcaps will be around 1 krad over the experiment lifetime and an order of magnitude less in the barrel.

3.8.1 The RPC Front-End Electronics

The 24-channel front-end board (FEB) is connected directly to the RPCs. It houses four front-end chips (FECs), two synchronisation units (SU), two DACs for threshold setting and the Front-End Board Controller (FEBC). Four FEBs belonging to the same RPC chamber are connected together.

The FEC is made of eight identical channels, each one consisting of preamplifier, zero-crossing discriminator, monostable circuit and differential line driver. In an RPC working in avalanche mode, an after-pulse often accompanies the avalanche pulse. Therefore, a monostable circuit follows the discriminator and gives a pulse shaped typically at 100 ns, in order to mask the possible second trigger and to prevent the zero-crossing discriminator from triggering on the noise. The FEC is manufactured in a 0.8 μm technology by AMS.

The SU stores the FEC output data if they fall within a pre-defined time window within a bunch crossing period and synchronises them with a selected bunch crossing period.

3.8.2 Status of RPC Electronics

The RPC FECs have showed good yield from a 1000 chip pre-production. Automatic testing has been commissioned and radiation tolerance tests of the on-detector front-end electronics are now complete. No significant degradation in chip performance has been

observed during total dose tests on the FEC [103]. The threshold LET has been estimated to be 4.9 $MeVcm^2mg^{-1}$ and the average time between SEUs in each FEC at CMS has been calculated to be about 1 hr following tests for neutron-induced SEUs [104]. Prototype RPCs with the AMS FEC have been tested and their time resolution is found to be better than 1.5ns [105, 106].

3.9 Summary

The electronics for the CMS sub-detector systems are at various stages of development. Their diversity is a consequence of the different requirements in each sub-detector. For example, the Tracker is required to have high spatial resolution, the calorimeter is required to have good energy resolution over a large dynamic range and the large area over which muon systems are deployed requires good alignment and stability.

The radiation damage mechanism that will pose a real threat to the reliable operation of many of the electronics systems is SEU. Table 3.2 lists the maximum radiation levels in each sub-detector along with technologies used and estimated SEU rates where data are available.

Table 3.2: Summary of radiation levels and SEU rates in CMS electronics.

Sub-system	Total Dose [rad]	Neutrons [cm^{-2}]	Ch. Hadrons [cm^{-2}]	Technology	SEU rates
Pixel	40 M	10^{14}	8×10^{14}	Rad-hard DMILL 0.8 μm	–
Tracker	15 M	9×10^{13}	3×10^{14}	Com. 0.25 μm CMOS	All CCU25s 84/hr All APV25s 116/hr
Preshower	7 M	1.6×10^{14}	3×10^{13}	Rad-hard DMILL	–
ECAL	2 M	5×10^{14}	5×10^{13}	Com. 0.25 μm CMOS	–
HCAL	190	3.1×10^{11}	2.7×10^{8}	Rad-hard AMS & com. Agilent 0.5 μm CMOS	0.1-0.01/Chip/Yr
Muon DT	12	2.3×10^{10}	2.7×10^{7}	AMS 0.8 μm BiCMOS	All ROB Components <1/dy
Muon CSC	1.8 k	8.7×10^{11}	5.5×10^{8}	Com. FPGAs and 0.8 μm CMOS	All Virtex FPGAs 0.1-0.25/hr
Muon RPCs	1 k	10^{11}	10^{8}	Rad-hard AMS	1/Chip/hr

SEUs will affect chips exposed to high levels of radiation, modifying chip thresholds, bias register settings and output data. Whilst some of the more recently designed custom

ASICs have SEU redundancy features, the older ASICs and many of the commercial components will be more vulnerable to SEUs. Frequent downloads of operating parameters have to be planned for in the final system.

The success of the Tracker in implementing its front-end in the 0.25 μm technology has led to its adoption by other sub-detectors (Pixel, ECAL, Preshower, Muon DT) as well as the other three LHC experiments. Whilst the microelectronics industry has moved on from the 0.25 μm technology to even smaller feature sizes (0.13 μm is now common), the newer technologies, though they have obvious advantages in terms of power consumption and circuit density, have not been qualified for use in high-energy physics experiments. The experience accumulated in the 0.25 μm technology in addition to the large gains in cost per wafer and the inherent radiation hardness make it ideal for use at the LHC, a view which is well expressed in the following quote by Weilhammer: 'The biggest help to survive the highest radiation levels probably came from outside high-energy physics in the form of the deep sub-micron CMOS technology. With relatively little specific developments by the HEP community, this technology can provide now the most radiation hard circuits for detector readout' [107].

Substantial cost savings will also be made from the use of the Tracker control architecture and optical links in other sub-detectors (ECAL, Preshower).

Chapter 4

Total Dose Testing

The 0.25 μm CMOS process used in the production of the APV25 is a commercial process that has not been qualified for radiation hardness. The responsibility for ensuring that ASICs designed in the process fulfil all requirements for operation in ionising radiation environments lies with the user. This has led to an extensive testing programme for the APV25 and individual test transistors. Most of the total dose testing has been carried out with an X-ray irradiator at Imperial College London, where test structures and APV25 chips are exposed to doses of up to 100 Mrad(SiO_2).

4.1 X-ray Irradiator for Total Dose Testing

The testing of electronics systems, devices, and components in dedicated facilities plays a central role in the investigation of radiation effects. The actual irradiation of the component or system should provide a simulation of the radiation environment it will encounter during its lifetime, although some parameters, such as exposure time, can rarely be reproduced.

Gamma- and X-ray sources are the two principal radiation sources used in total dose testing. X-ray sources offer many advantages over gamma ray sources, the most important being much higher dose rates and safer, easier handling. Though the low energy (~ 10 keV) X-rays typically used in radiation hardness tests are less penetrating than gamma rays (~ 1.25 MeV for ^{60}Co) and interact differently with matter, X-ray irradiators are fast replacing the traditional gamma ray facilities. Many comparative studies have been made of the two sources, highlighting their equivalence [108, 109, 110, 111, 112, 113, 114, 115]. An X-ray irradiator was used in the total dose tests reported here.

4.1.1 Characteristics of the X-ray Irradiator

The target material used in the X-ray tube is tungsten. The radiation spectrum consists of characteristic L-lines around 10 keV along with a bremsstrahlung continuum. The tube can be set to voltage values between 2 and 60 kV in 1 kV steps and current values between 2 and 80 mA in 1 mA steps [116]. The distance between the tube and the device under test (DUT) can also be adjusted, resulting in a change of dose rate. In microelectronics applications, the aim is to produce a spectrum whose effective energy

is peaked in the 5-15 keV photon energy region [117]. The tube voltage was maintained at 50 kV which is typical for the given application leaving two variables, the tube current and the distance between tube and DUT, to modify the dose rate. The low energy components, < 5 keV, of the X-ray beam are removed using 150 μm of Al shielding. Fig. 4.1 shows a photograph of the Seifert RP 149 X-ray cabinet.

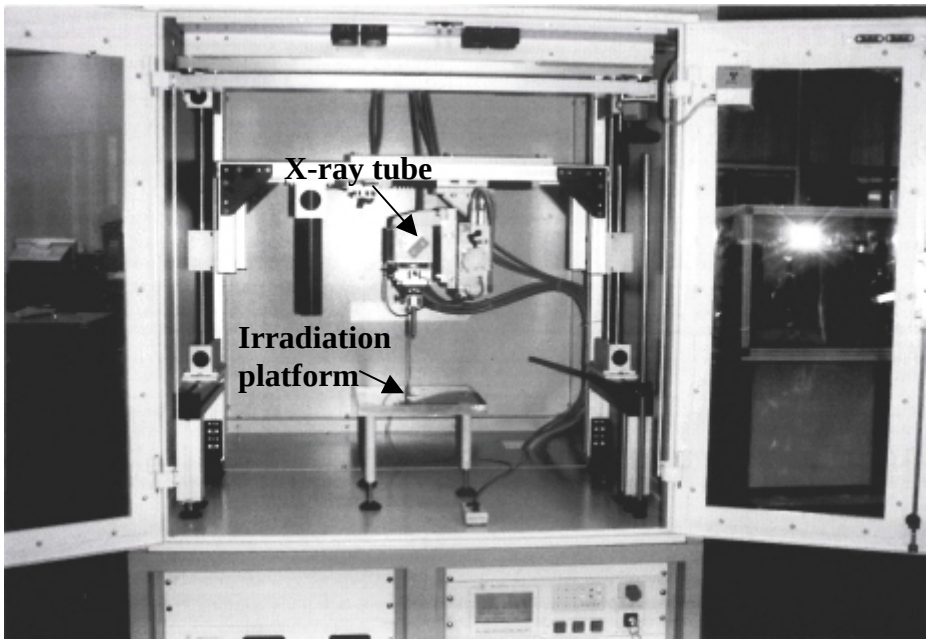


Figure 4.1: X-ray machine cabinet with the X-ray tube and the irradiation platform.

Silicon diode detectors were used for dosimetry tests on the X-ray beam. The dosimetry diode current was verified to be inversely proportional to the square of the distance between the tube and the diode and linearly proportional to the X-ray tube current at any tube height.

The DUT has to be located in such a way that it receives as uniform a dose as possible across its area. It was therefore necessary to measure the dose profile of the X-ray beam over a large irradiating area. A thick sheet of copper was used to shield most of the diode area from X-rays but allowed a fraction of the X-rays through 1 mm-diameter hole at its centre. The X-ray tube was moved from left to right and from back to front in the X-ray cabinet, covering a square grid. Readings of the diode current were taken at 1 mm intervals. The X-ray tube movement and the current readings were controlled remotely using a program written for this purpose with an instrumentation software package called LabVIEW[3]. Contour maps were drawn for the dose profiles at different X-ray tube heights. These are useful because they give a clear indication of where the DUT should be positioned.

[3] National Instruments Corporate Headquarters, 6504 Bridge Point Parkway, Austin, Texas 78730-5039 USA. Web: Ni.com/labview.

4.1.2 Determination of the Total Dose

Dose calculations can be simplified if the energy is deposited uniformly throughout the depletion region of the diode. For the X-rays to be attenuated as little as possible, thin dosimetry diodes are normally used. The attenuation length[4] of 10 keV X-rays in silicon is 134.2 μm [118]. The diode thickness must be considerably less than 134.2 μm and diodes used for this type of application are typically 25 μm thick [119]. Some thick silicon diodes were readily available for initial tests and were used in conjunction with simulation results to estimate the dose rate. These thick diodes have an active area of 5 × 5 mm^2 and a thickness of 263 μm ± 10 μm. Thinner diodes with an active area of 1 × 1 cm^2 and a thickness of 12 μm were obtained later for more precise measurements.

Given a diode current I, the following steps illustrate how the radiation dose was calculated:

- Sensitive volume mass, $m = \rho V = 2330 \times 6.585 \times 10^{-9} = (1.53 \pm 0.06) \times 10^{-5}$ kg;
- Energy deposited. The number of electron-hole pairs produced throughout the diode per second is I/q where q is the electronic charge. The energy required to generate an electron-hole pair is 3.62 eV. The energy deposited in the diode per second is $3.62 \times I$ [Js^{-1}];
- Dose rate, D, in rad(Si).s^{-1} (1 J/kg = 100 rad);
- $D = \frac{I \times 3.62 \times 100}{m} = (2.37 \pm 0.09) \times 10^7 \times I[rad(Si)s^{-1}]$ …eq. (4.1).

The calculation above can only be done when the energy is deposited uniformly throughout the device. Since an estimate of the dose rate was required before the acquisition of the thin diodes, the dose obtained from the thick diode was multiplied by a correction factor, which accounted for the attenuation of the X-ray beam. The correction factor was obtained from simulations of the X-ray environment.

The simulation program computes values for equilibrium dose[5] and total dose[6] for a given photon spectrum or mono-energetic beam and for various shielding configurations. The results are returned as plots of equilibrium dose or total dose as a function of material thickness or mass. The simulation program requires an input spectrum which was taken from a similar system [117].

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[4] The attenuation length of a given material is the length at which the intensity of an X-ray beam falls to 1/e of the incident beam intensity.

[5] The so-called equilibrium dose is the dose calculated by use of the energy absorption coefficients (electron transport across the interfaces of dissimilar substances is not considered).

[6] The total dose is calculated after the equilibrium dose and includes dose enhancement/dose reduction at the interfaces of layers with dissimilar substances and electron leakage through the front and rear surfaces of DUTs.

The total dose for each diode was inferred from the depth-dose profiles of Figs. 4.2 and 4.3 returned by the simulation software.

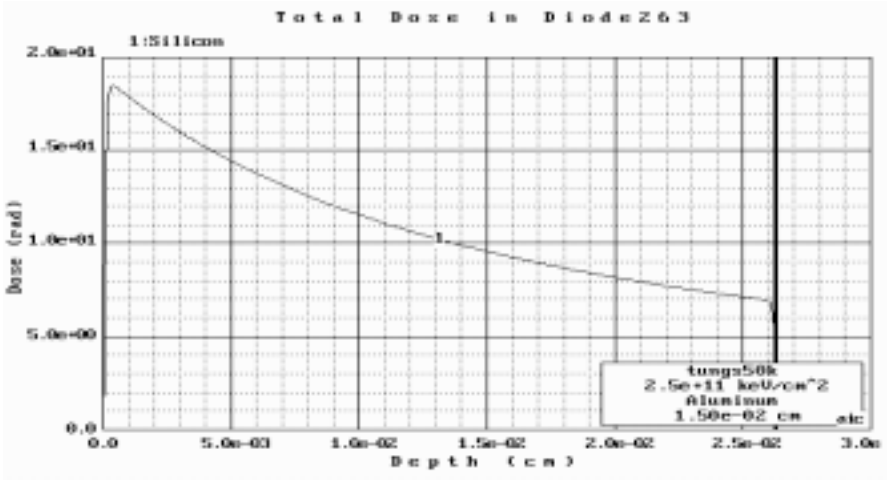


Figure 4.2: Depth-dose profile for the total dose in the thick 263 μm diode.

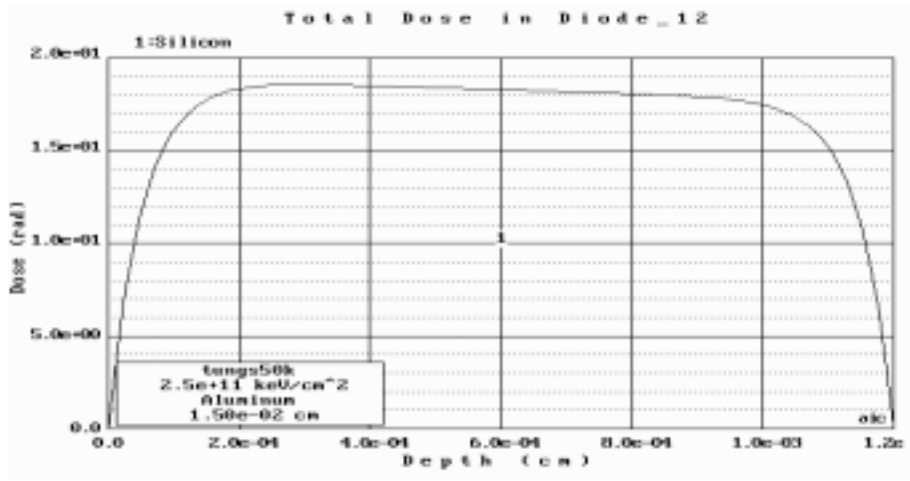


Figure 4.3: Depth-dose profile for the total dose in a 12 μm diode.

The total doses for the same incident X-ray beam intensity in the two different diodes are given in Table 4.1.

Table 4.1: Total dose in silicon slabs of various thicknesses.

Diode Thickness [μm]	Total Dose [rad(Si)]	Ratio, normalised to 263 μm dose
263	10.97	1
12	16.06	1.464

Multiplying the dose rate in eq. (4.1) by the ratio given in Table 4.1 yields the following expression:

$$D = (3.47 \pm 0.13) \times 10^7 \times I[rad(Si)s^{-1}] \qquad \text{.....eq. (4.2).}$$

where I is the current in the 263 μm diode.

Eq. (4.2) was used in the early stages of the radiation tests.

Two thin diodes were tested and the dose rates calculated are given in Table 4.2, along with thickness and current through diode. The thickness of the diodes was given by the technical specification sheet as 12 μm ± 1 μm which was confirmed using C-V measurements. The dark current is subtracted from the current reading, with an error of ± 10 nA accounting for fluctuations in the dark current during irradiation.

Table 4.2: Dose rates in thin diodes.

Diode reference No.	Diode Thickness [μm]	I [μA]	Dose rate [rad(Si)/s]
137-5	12.4 ± 0.1	0.61 ± 0.01	76.4 ± 1.9
137-6	12.0 ± 0.1	0.59 ± 0.01	76.4 ± 1.9

The current through the thick diode under the same conditions as those used in the thin diode measurements was 2.07 μA ± 0.01 μA. This corresponds to a total dose rate of 71.8 ± 3 rad(Si)/s using eq. (4.2), a value which is ~ 6 % less than the dose rate obtained with the thin diodes in Table 4.2.

A new correction factor was calculated from the ratio of the uncorrected doses in thin and thick diodes:

Uncorrected thick diode, $D = (2.37 \pm 0.09) \times (2.07 \pm 0.01) \times 10 = 49 \pm 2$ rad(Si)/s

Thin diode dose, $D = 76.4 \pm 1.9$ rad(Si)/s

$\Rightarrow$ **correction factor = 76.4 / 49 = 1.56 ± 0.1** (c.f. 1.464 in Table 4.1)

The final expressions used to convert a current in the thick diode, *I*, to a dose rate are:

$$DoseRate(Si) = (3.7 \pm 0.37) \times 10^7 \times I[rad(Si)s^{-1}] \quad \text{.....eq. (4.3).}$$

$$DoseRate(SiO_2) = (2.07 \pm 0.21) \times 10^7 \times I[rad(SiO_2)s^{-1}] \quad \text{.....eq. (4.4).}$$

The expressions above do not take into account dose enhancement effects. These occur at the interface of two materials with different photoelectric cross-sections. More electrons are produced in the material with the higher cross-section and they can cross into the material with the lower cross-section, thus enhancing its dose. The electrons are short ranged ~ 1.5 μm in Si. These effects are therefore negligible in the thick diode but can lead to an underestimate of the dose in the thin diode by up to 10 %.

A calibrated Keithley 35050A dosimeter was used to measure the dose. It was connected to an ionisation chamber placed 39 cm away from the X-ray tube mount. The tube voltage and current were 50 kV and 50 mA respectively. The dose rate measured by the chamber was 9.75 rad(air)/s.

A dose in air can be converted to a dose in silicon using the relative mass-energy absorption coefficients. A weighted average value of 7.266 for the ratio of silicon to air

coefficients was obtained by A. Papanestis [120], deduced from considerations of the X-ray spectrum.

The following equivalence between dose in air and dose in silicon was calculated from the weighted average value: 9.75 rad(air)s^{-1} ↔ 70.844 rad(Si)s^{-1}.

The thick diode current at the same position, 2.17 μA ± 0.01 μA, when used in eq. (4.3) yields a value for the dose rate of 80.4 ± 8.4 rad(Si)s^{-1}. The dose rate obtained with the diode is higher than that given by the ionisation chamber. This can be partly attributed to the fact that the ionisation chamber area is much larger (A = 12.6 cm^2 compared with 0.25 cm^2) than the diode area and therefore there is a more significant spread in intensity across the ionisation chamber, which leads to a reduction in the dose rate.

4.2 Total Dose Tests on 0.25 μm Test Structures

Test structures are usually manufactured on a wafer alongside chips to monitor and assess the quality of a given process/wafer/run. They typically contain transistors, capacitors and resistors. If a problem develops, it is often easier to investigate it using discrete components in a test structure than to analyse a chip containing thousands of transistors. Characterising a process for total dose radiation tolerance requires testing discrete transistors since this is the only way of acquiring primary information on the evolution of static parameters such as threshold voltage and subthreshold swing.

4.2.1 Transistors Tested

The measured transistors are listed in Table 4.3.

Table 4.3: Dimensions of the transistors tested.

	Version/Foundry	Device	Width [μm]	Length [μm]
Study 1	Foundry A	PMOS	2000	0.36
		PMOS	2000	0.5
		PMOS	2000	0.64
		NMOS	2000	0.36
	S0, Foundry B	PMOS	2000	0.24
		PMOS	2000	0.36
		PMOS	2000	0.48
		PMOS	2000	0.6
Study 2	S0 and S1, Foundry B.	PMOS (P1)	2000	0.24
		PMOS (P2)	2000	0.36
		PMOS (P3)	2000	0.36
		PMOS (P4)	2000	0.6
		NMOS (N1)	100	2.5
		NMOS (N2)	100	2.5

Two variants of the APV25 chip have been produced, the earlier S0 version and the final S1 version. Minor changes to the design of the chip distinguish the two versions but because the process is identical, the test structures from both are the same. All APV25 chips are manufactured at the same foundry, referred to as Foundry B. In addition to the test structures that are produced alongside the APV25, transistors from another Foundry, Foundry A, employing the same process were made available for testing. The total dose investigations on test structures can be divided into two studies. In the first study, transistors from the two different foundries were tested. In the second study, transistors manufactured at Foundry B from both the S0 and the S1 versions were tested. Most of the transistors tested were PMOS transistors with a channel width of 2000 μm. These were chosen because the dominant contribution to the noise in the APV25 is given by the input preamplifier transistor, which is a PMOS transistor with a channel length of 0.36 μm and width of 2000 μm operated with a bias current of ~ 400 μA. The NMOS transistors in Study 2 are used as current sources in the analogue front-end and the deconvolution filter of the APV25.

None of the transistors had ElectroStatic Discharge (ESD) protection. This led to a number of handling problems, even though anti-static precautions were taken wherever possible.

4.2.2 Experimental Procedure

4.2.2.1 Irradiation of Transistors

Two reference qualification methods have been defined to qualify a product for radiation hardness. These are the American MIL-STD-833 Test Method 1019.4 and the European ESA/SSC Basic Specification (BS) 22900 (from the European Space Agency, ESA). Ideas were taken from these two testing methods to develop an irradiation and annealing method more suitable for ASICs to be used in the CMS environment.

All transistors were irradiated with a bias typical of normal operating conditions applied across the gate ($|V_G| > 500$mV). This does not represent the worst-case bias conditions, which would be a maximum gate bias (2.5 V) for NMOS transistors and all terminals grounded for PMOS transistors. Irradiations were carried out in several steps up to a total dose of 50 Mrad(SiO_2). In addition to the discrete step irradiations, continuous irradiations were carried out in Study 2 up to doses varying between 20 Mrad and 100 Mrad.

Total doses at the LHC are expected to be accumulated with an average dose rate varying from 1.4 krad/h to less than 0.027 rad/h with a maximum of 720 rad/hr in the

strip tracker [121]. The dose rate used during the work described here was approximately 500 krad/h. This discrepancy in dose rates is taken into account by accelerating the annealing stage. The transistors were placed in an oven after each irradiation step at a temperature of 100 ^{o}C for 1 week. They were also biased during annealing.

4.2.2.2 Measurement of Transistors

Static parameters and noise of the transistors were measured before irradiation, after each irradiation step and after annealing. The measurement setup for the static parameter testing is shown in Fig. 4.4. It was controlled from an Apple Macintosh using LabVIEW.

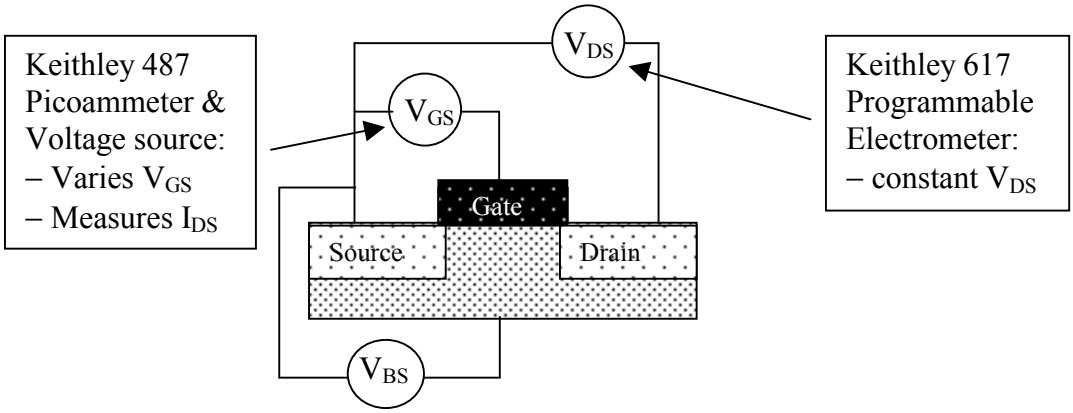


Figure 4.4: Static parameter testing setup for transistors.

In both studies, PMOS transistors were measured with and without bias applied to the bulk, V_{BS} = + 1.25 V. NMOS were always measured without bulk bias.

In Study 2, continuous monitoring of the static parameters of transistors throughout the irradiation and annealing stages was carried out for a few runs. During irradiation, the temperature in the X-ray irradiator increases by ~ 5 ^{o}C, which was taken into account in the calculation of ΔV_{Th}.

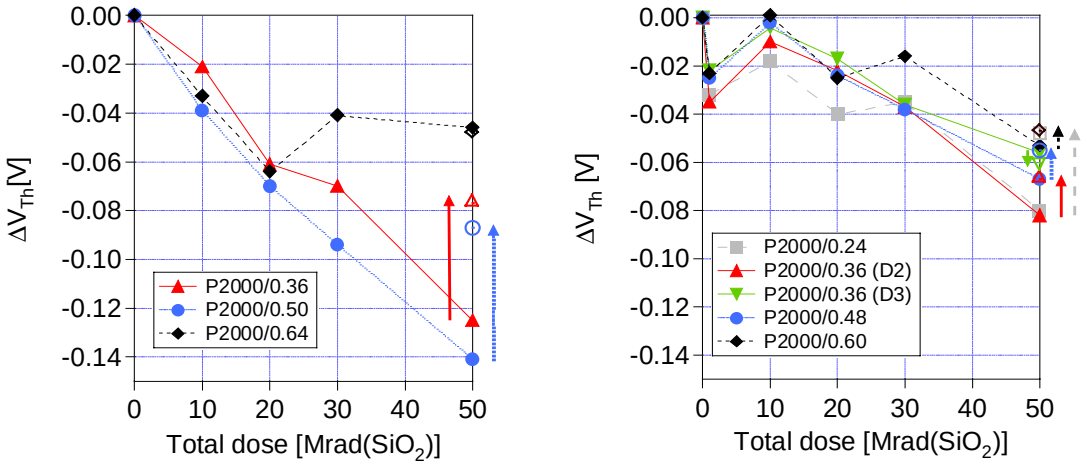
The setup used to measure the noise is described in more detail in [122]. A Hewlett Packard HP4195A spectrum analyser was used to measure the gate referred voltage noise spectra of the DUT. The system is based on converting the noise current at the drain of the DUT to a voltage by a transimpedance amplifier and by referring the voltage noise spectrum back to the gate of the DUT. The drain voltage, V_{DS}, on the DUT was set to 500 mV and a self-biasing circuit regulated the gate voltage, V_{GS}, to a value around 500 mV allowing for measurements in the moderate inversion region with 400 µA < $|I_{DS}|$ < 500 µA.

4.2.3 Static Parameter Degradation

The threshold voltage is the static parameter which is the most sensitive and therefore more attention is paid to it in this section. The threshold voltage is calculated by interpolation of the I_{DS}-V_{GS} curve between two values of drain current, with an error of ± 2 mV. The threshold voltage shift, ΔV_{Th}, is calculated by subtracting the pre-irradiation value of the threshold voltage from its value after irradiation. In order to separate the contributions from oxide and interface traps, a qualitative analysis of the subthreshold slope and transconductance was carried out.

4.2.3.1 PMOS Threshold Voltage Shift

Interface traps and oxide trapped charge both contribute towards a negative shift in the threshold voltage in PMOS transistors.

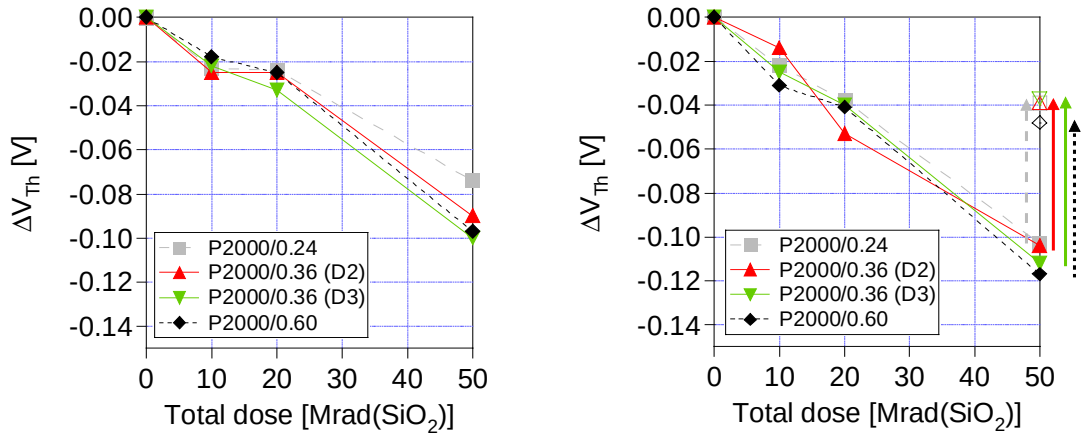


(a) Foundry A. *(b) Foundry B.*

Figure 4.5: ΔV_{Th} in PMOS transistors from Study 1.

Fig. 4.5 shows the threshold voltage shifts in PMOS transistors for foundries A and B. The maximum shift is around −125 mV for Foundry A and −80 mV for Foundry B at 50 Mrad(SiO_2) for transistors of identical dimensions (W/L = 2000/0.36 µm). The points representing the annealing are those without a background. An arrow points from the measurement at 50 Mrad to that after annealing. After annealing, 6 of the 8 transistors show some partial recovery whilst the other 2 transistors show virtually no change. There does not seem to be a correlation of radiation sensitivity with channel length for transistors from Foundry A. A trend towards larger shifts for smaller channel lengths can be observed in transistors from Foundry B. The non-linear behaviour observed in Fig. 4.5 (b) is thought to be due to a combination of factors; the transistors were left unbiased for different periods of time between irradiation steps allowing some

room temperature annealing and the absence of ESD protection may have had some effect during handling from the X-ray machine to the measurement setup.



(a) Version S0. *(b) Version S1.*

Figure 4.6: ΔV_{Th} in PMOS transistors from Foundry B, Study 2.

Fig. 4.6 shows the threshold voltage shift for the PMOS transistors irradiated during the course of Study 2. After 50 Mrad, shifts between –80 mV and –120 mV are observed. No annealing data are available for the S0 version. Significant recovery, of ~60 mV, is observed after annealing for all transistors from the S1 version. There is a small dependence of theshold voltage shift on channel length in Study 2, this time with larger voltage shifts for transistors with longer channel lengths, contrary to the trend observed in Study 1. The data sets are very small and a strong statement of the dependence of threshold voltage shift on channel length cannot be made. Though there are small differences between the data in Study 1 comparing the two foundries and the data in Study 2 comparing the two versions (S0 and S1), the threshold voltage shifts obtained in all cases are consistent. All the threshold voltage shifts observed are small and would not cause a loss of functionality or degradation of performance in ASICs such as the APV25.

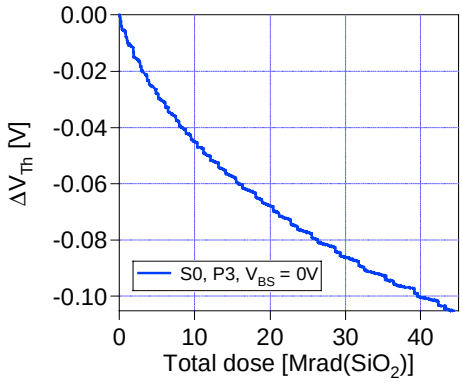


Figure 4.7: Results from the continuous monitoring of ΔV_{Th} throughout the irradiation stage in a PMOS transistor, P3, W/L=2000/0.36 µm, version S0.

The results of the continuous monitoring of PMOS transistors during irradiation are consistent with measurements after discrete irradiation steps, Fig. 4.7.

To complement the results obtained with the X-ray irradiator, a pulsed 8 MeV LINAC electron beam was used to irradiate a test structure from Foundry B [123]. The LINAC produced 0.624 krad(Si)/pulse with 50 pulses/s. The dose rate obtained was 112 Mrad(Si)/hour, much higher than that given by the X-ray source. The uncertainty on the measurement of the dose rate was 10 %.

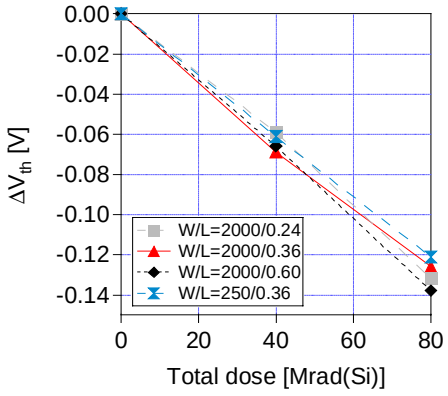


Figure 4.8: ΔV_{Th} in PMOS transistors from electron beam irradiations.

The test structure was irradiated to a final dose of 80 Mrad(Si) with one intermediate step at 40 Mrad(Si), Fig. 4.8. The results are consistent with those obtained with the X-ray irradiator.

4.2.3.2 PMOS Subthreshold Swing and Transconductance

The effect of interface states can be distinguished from that of traps in the oxide by analysing the subthreshold slope in the I_D-V_G curve. The subthreshold slope is taken in the linear region of operation of the chip, where I_D increases linearly with $|V_G|$. Charge traps at the interface can cause a reduction in mobility, which leads to a reduction in transconductance.

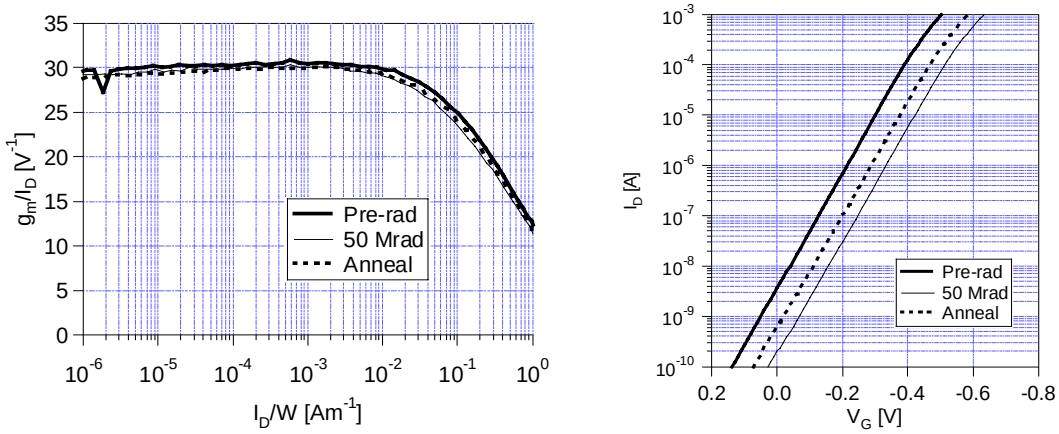
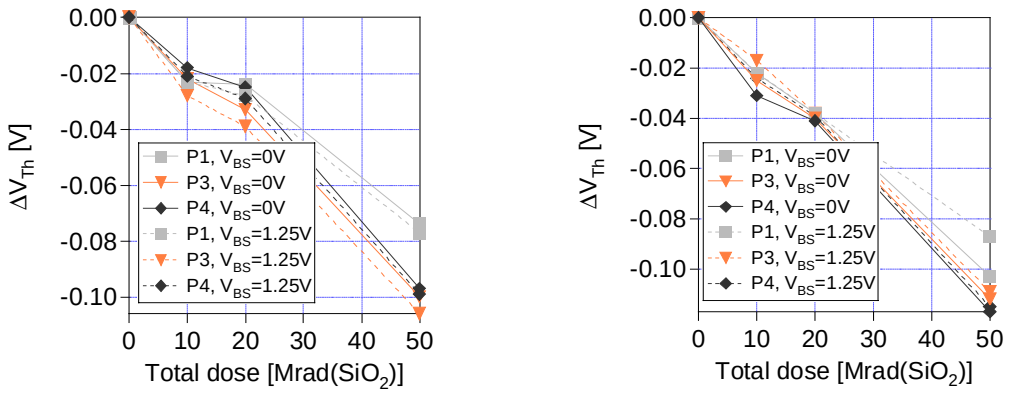


Figure 4.9: PMOS transistor transconductance and subthreshold slope.

When the reduction in mobility is high, the slope is visibly less steep. Although the threshold voltage shift can clearly be seen in Fig. 4.9, there is no significant change in the slope for PMOS transistors. This would suggest that very few interface states are generated, as expected since the negative gate bias leads to hopping of holes towards the gate electrode thus reducing the strain at the interface responsible for interface trap formation. There is no significant change in the transconductance.

4.2.3.3 PMOS Bulk Bias Dependence

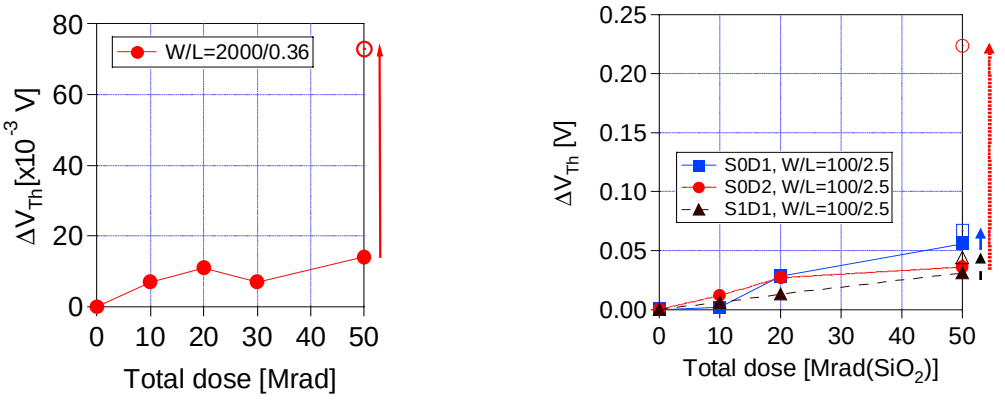


(a) Version S0. *(b) Version S1.*

Figure 4.10: Bulk bias dependence for PMOS transistors.

In Study 1, no significant difference in ΔV_{Th} is seen when the bias applied on the bulk, V_{BS}, is changed from V_{BS} = 0 V to V_{BS} = 1.25 V, Fig. 4.10 (a). In Study 2, a slight increase in ΔV_{Th} is observed for the S0 version but the opposite is observed for the S1 version. With V_{BS} = 1.25 V, fewer radiation-induced holes should move towards the Si/SiO_2 interface, hence reducing the trapped charge. However, there is no conclusive evidence pointing to a dependence of ΔV_{Th} with V_{BS}. A bias applied to the bulk is often used to minimise transistor noise but the input transistor in the APV25 is run with V_{BS} = 0V.

4.2.3.4 NMOS Threshold Voltage Shift



(a) Study 1. *(b) Study 2.*

Figure 4.11: ΔV_{Th} in NMOS transistors.

Fig. 4.11 shows a positive ΔV_{Th} in the NMOS transistor. Oxide traps cause a negative ΔV_{Th} in NMOS whereas interface traps cause a positive ΔV_{Th}. Since ΔV_{Th} is positive, the contribution from interface states is larger than that from oxide traps. In the transistor from Study 1, ΔV_{Th} is 14 mV after 50 Mrad. After annealing however, ΔV_{Th} increases to 73 mV. The transistors from Study 2 show a similar trend. One chip from version S0 shows a large shift after annealing, possibly due to handling since a few failures were observed in NMOS transistors not shown here. During annealing, it is unlikely that new interface states are being created. The jump in ΔV_{Th} is more likely caused by the thermal annealing of oxide traps.

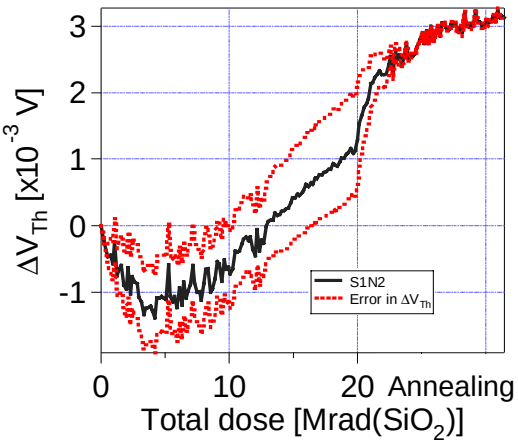


Figure 4.12: ΔV_{Th} in an NMOS transistor monitored continuously during irradiation.

The NMOS transistor that was continuously monitored during irradiation up to a dose of 20 Mrad shows a much smaller ΔV_{Th}, Fig. 4.12. One possible explanation for this is that the bias across the gate is continuously varying, allowing less interface trap formation, unlike the discrete step irradiations where the bias across the gate is constant.

4.2.3.5 NMOS Subthreshold Swing and Transconductance

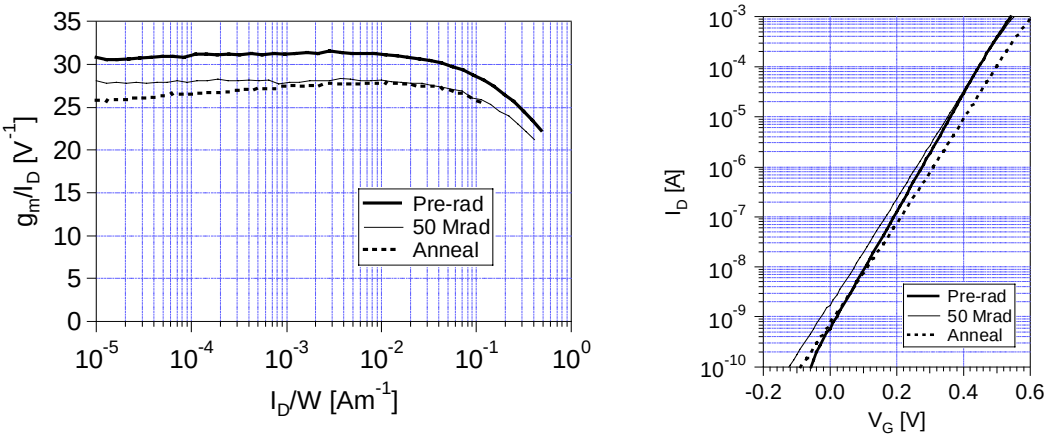


Figure 4.13: NMOS transistor transconductance and subthreshold slope.

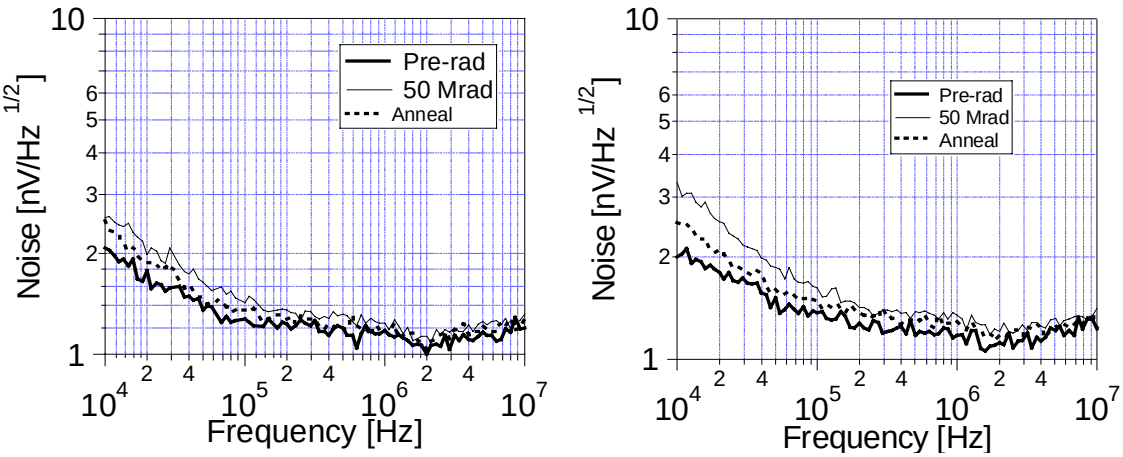
A reduction in the slope of the I_D-V_G curve is visible after irradiation and annealing, Fig. 4.13, confirming the generation of interface states, which cause a reduction in the mobility of charge carriers in the conducting channel. This reduction in mobility can also be seen in a plot of the normalised transconductance (g_m/I_D). g_m/I_D decreases by 9 % after 50 Mrad and by 15 % after annealing (weak inversion, $I_D/W = 10^{-5}$ Am^{-1}).

4.2.4 Noise

Data on noise come mostly from PMOS transistors since these are at the input of the pre-amplifier stages. NMOS transistor measurements are also presented for comparison.

4.2.4.1 Noise in PMOS Transistors

In PMOS transistors, the corner frequency lies between 5×10^4 and 2×10^5 Hz. This is true for all PMOS transistors from both foundries and both studies, Figs 4.14 & 4.15.



(a) Foundry A. *(b) Foundry B.*

Figure 4.14: PMOS transistor noise: Foundry A, Study 1, W/L=2000/0.36 μm.

The noise curves from Study 2 are in good agreement with Study 1, Fig. 4.14.

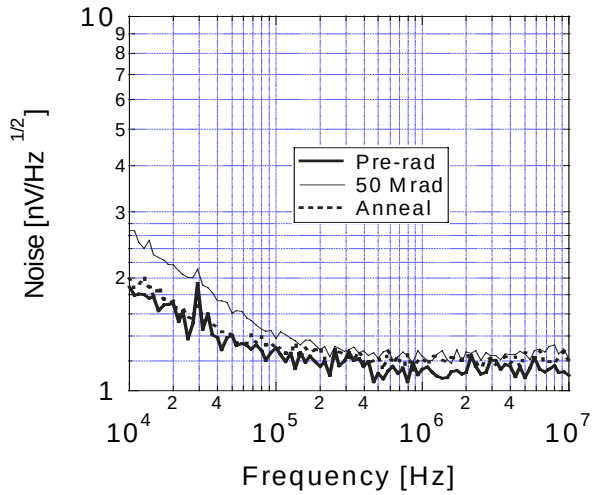


Figure 4.15: PMOS transistor noise: Foundry B, Study 2, W/L=2000/0.36 μm.

Thermal noise levels for the PMOS transistors are reported in Table 4.4. These were calculated by averaging the thermal noise values for frequencies above 1 MHz. They change very little after irradiation and annealing. The PMOS transistors from Foundry B in both studies have a slightly higher thermal noise level before irradiation and this level increases by a higher fraction after irradiation compared to the PMOS transistor from Foundry A. Since there is no change in mobility and transconductance after irradiation, the increase in thermal noise is likely to be due to changes in the excess noise factor, Γ.

Table 4.4: Thermal noise levels and percentage increase w.r.t pre-rad values for PMOS transistors irradiated with X-rays.

	Study 1				Study 2	
	PMOS Foundry A		PMOS Foundry B		PMOS Foundry B	
Dose [Mrad(SiO_2)]	Noise level [nV/√Hz]	% increase	Noise level [nV/√Hz]	% increase	Noise level [nV/√Hz]	% increase
0	1.12	0	1.14	0	1.14	0
50	1.2	7	1.25	10	1.25	10
Anneal	1.17	4.5	1.21	6	1.21	6

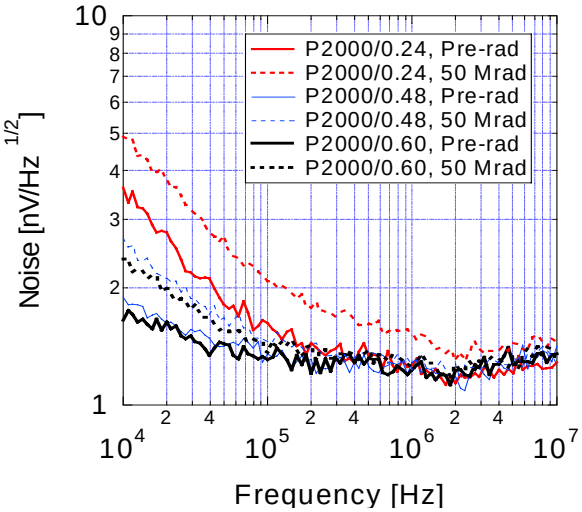


Figure 4.16: Noise in PMOS transistors from Foundry B, Study 1, showing the dependence of noise on channel length.

Transistors with smaller channel lengths show higher 1/f noise as expected, Fig. 4.16.

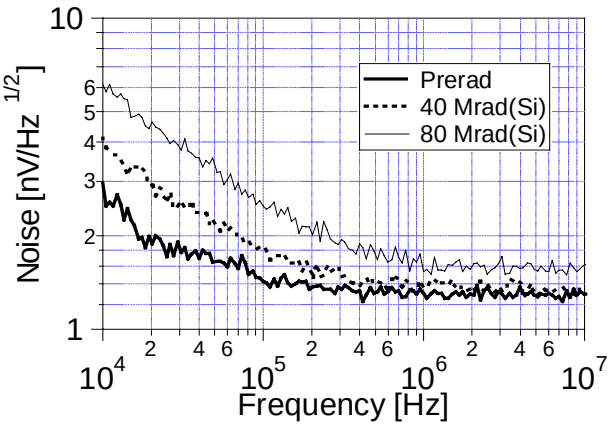


Figure 4.17: PMOS transistor noise, Foundry B, irradiated with 8 MeV electrons.

Fig. 4.17 shows the evolution of the noise characteristics of the PMOS transistor irradiated with 8 MeV electrons. The corner noise frequency increases from 50 kHz before irradiation to 400 kHz after 80 Mrad(Si). The average thermal noise level does not increase significantly after 40 Mrad(Si). However, after 80 Mrad(Si) there is a 20 % increase in the thermal noise level, Table 4.5.

Table 4.5: Thermal noise levels and percentage increase w.r.t pre-rad values for the PMOS transistor irradiated with electrons.

Dose [Mrad(Si)]	Noise level [nV/√Hz]	% increase
0	1.29	0
40	1.34	4
80	1.55	20

The higher noise levels in Table 4.5 (compared to Table 4.4) can be partially explained by the fact that the bias conditions during the noise measurements were different ($|I_{DS}|$ = 500 μA for measurements in Table 4.4, $|I_{DS}|$ = 400 μA for measurements in Table 4.5).

4.2.4.2 Noise in an NMOS Transistor

Although NMOS transistors are not used as the input transistors in the amplifying stage of the APV25, it is interesting to include some NMOS noise measurements.

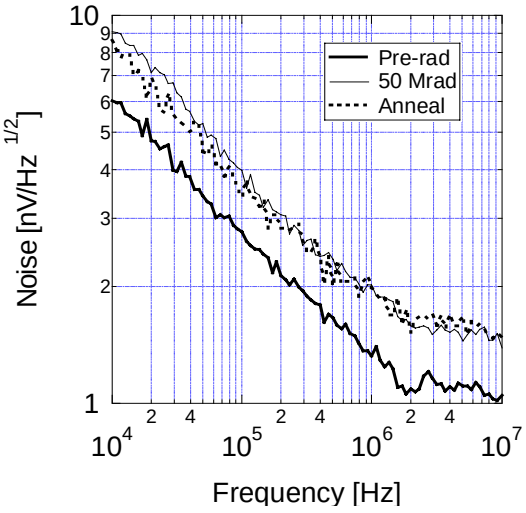


Figure 4.18: NMOS transistor noise, Foundry A, Study 1.

A comparison between PMOS and NMOS transistors confirms that the NMOS transistor has a much higher spectral noise density. In the case of the NMOS transistor, the corner frequency lies above 2 MHz, Fig. 4.18. After irradiation, the thermal noise level increases significantly compared to the PMOS transistors. This provides more evidence to suggest that interface states are being generated during irradiation.

4.3 Total Dose Tests on the APV25

Approximately 75 000 APV25 chips will be used in the CMS Tracker. These have to be fully qualified before they are mounted on detector modules. Tests of the digital functionality of the chip along with a characterisation of many of its analogue components are carried out at wafer level. The test setup is fully automated and is described elsewhere [124, 125]. It allows efficient screening of defective chips, with a test time of ~ 7 hrs for an 8-inch wafer (~ 360 chips).

Total dose tests on APV25 chips are carried out as an additional quality assurance measure. They monitor chips that have successfully passed the wafer screening tests, ensuring that these are also radiation tolerant. Because of the variation in the quality of wafers between different production runs, it is quite conceivable that some wafers contain chips that pass the wafer screening stage but are more sensitive to radiation damage. Chips have to be biased during irradiation and since the X-ray machine is not equipped with a probe station and probe card, wafers have to be diced before the chips can be mounted on custom boards and irradiated.

4.3.1 Chips Tested

Before the quality assurance test was defined, five chips were irradiated to ensure that the first few wafers received were radiation tolerant. Four chips from the S0 version were irradiated, three to 10 Mrad and one to 20 Mrad. One chip from the S1 version was irradiated to 10 Mrad. Since the measurement setup was still under development, the tests performed on these five chips were limited. None of the chips showed any significant degradation in performance.

The results that are presented here are taken from the last 23 chips that were irradiated, all from the S1 version. 10 of these are from 10 engineering wafers. 9 chips were irradiated to 10 Mrad in one step and 1 chip to 100 Mrad in several steps. No information on the position of the chips within the engineering wafers was available after dicing. The remaining 13 chips were cut from the 13 wafers from the third production lot and were all irradiated to 10 Mrad. The wafer screening tests for the third production lot revealed some wafers with areas of low yield, most of the bad chips being located around the middle and periphery of the wafer, Fig. 4.19. The position of the chips for the third production lot was marked after cutting and good chips close to the low-yield areas were chosen for irradiation, to look for correlations between radiation sensitivity and wafer quality.

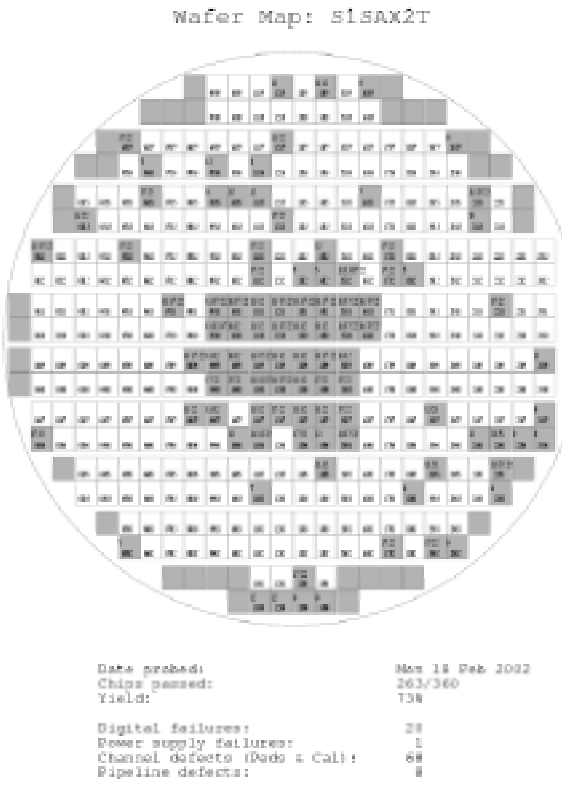


Figure 4.19: Wafer map from a wafer screening test. Failed chips are in grey.

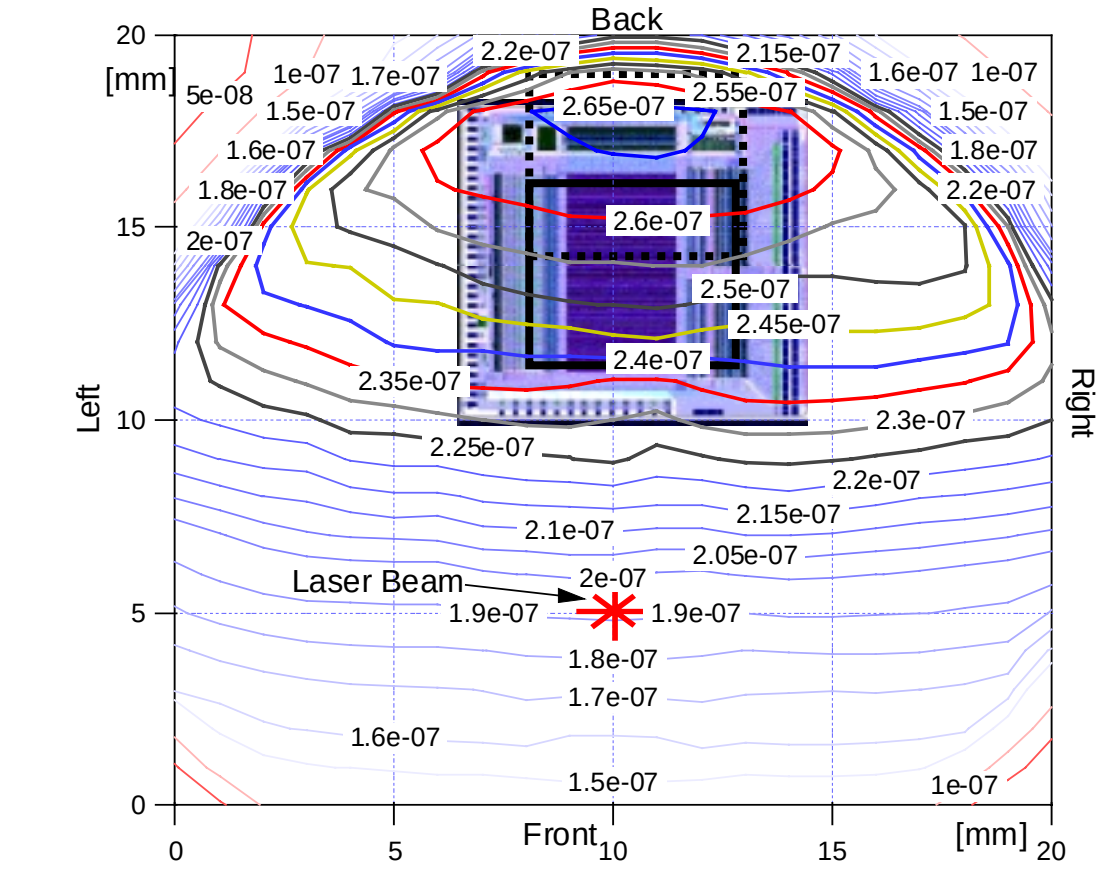
4.3.2 Experimental Procedure

4.3.2.1 Irradiation Procedure

Chips are irradiated under bias. They are clocked and triggered and the pipeline is randomly cycled in order to ensure that all pipeline cells and associated digital logic receive the same bias on average. The horizontal positioning of the chips during irradiation is shown in Fig. 4.20, superimposed on a contour map obtained using the method described in Section 4.1.1. The text labels on all sides of the graph indicate the sides of the X-ray cabinet. A laser beam situated next to the tube can be switched on to indicate where DUTs should be positioned, as recommended by the manufacturer of the X-ray irradiator. The location of this laser beam is indicated in the contour map by a '*'. It is quite clear that to achieve a variation of the dose across the chip of < 10 % the chip has to be carefully positioned. It should not be placed as indicated by the laser beam but away from the laser beam, towards the back of the X-ray cabinet. The last few mm towards the back of the X-ray field experience a sharp decrease in the field intensity.

The area of the chip located towards the back of the X-ray cabinet contains the digital blocks of the chip. The front of the chip, where the bonding pads for the 128 channels are located, points towards the right of the X-ray cabinet as it is shown in Fig 4.20. The

lowest channel numbers (channel 0 →) receive more radiation, with channel 0 receiving ~ 8 % more radiation than channel 127.



Active area of dosimetry diode, position during calculation of dose rate received by APV25 chips

Active area of dosimetry diode, position at maximum dose rate

Figure 4.20: Positioning of the APV25 during irradiation.
The contour lines show the relative intensity of the X-ray field on a horizontal plane.

The vertical distance between the edge of the X-ray tube casing and the surface of the chip is ~ 110 mm. It is a compromise between a lower height with a higher field intensity but less uniformity, and a greater height with higher uniformity but lower field intensity. The dose rate achieved in this position is 0.67 Mrad(SiO_2)/hour with an irradiation time of just under 15 hours for a dose of 10 Mrad(SiO_2). Ideally, the irradiation would be completed in one step but because the X-ray tube is operated close to its limit (tube current 55 mA, tube voltage 50 kV ⇒ 2.75 kW compared with the 3 kW limit), the X-ray machine occasionally tripped with error messages such as 'Relative under-voltage monitoring' or 'Relative over-current monitoring'. Once the X-ray machine trips, it has to be manually restarted. Because the majority of trips occurred

overnight, irradiation times varied between 15 hours and 48 hours, with some room temperature annealing taking place during those periods when the tube was not running.

4.3.2.2 Annealing

After irradiation, chips are placed in an oven at 100 ^{o}C for a week under bias. Only one chip can be placed in the oven at any one time. Because up to 5 chips can be irradiated per week but only 1 can be annealed, the time between the end of irradiation and the start of annealing is variable.

4.3.2.3 Measurement Procedure

Once the wafers have been tested with the wafer probing measurement setup, they are diced by a contractor. The cut die are sent back to Imperial College London where one chip per wafer is selected for irradiation tests and glued and bonded to a daughter board.

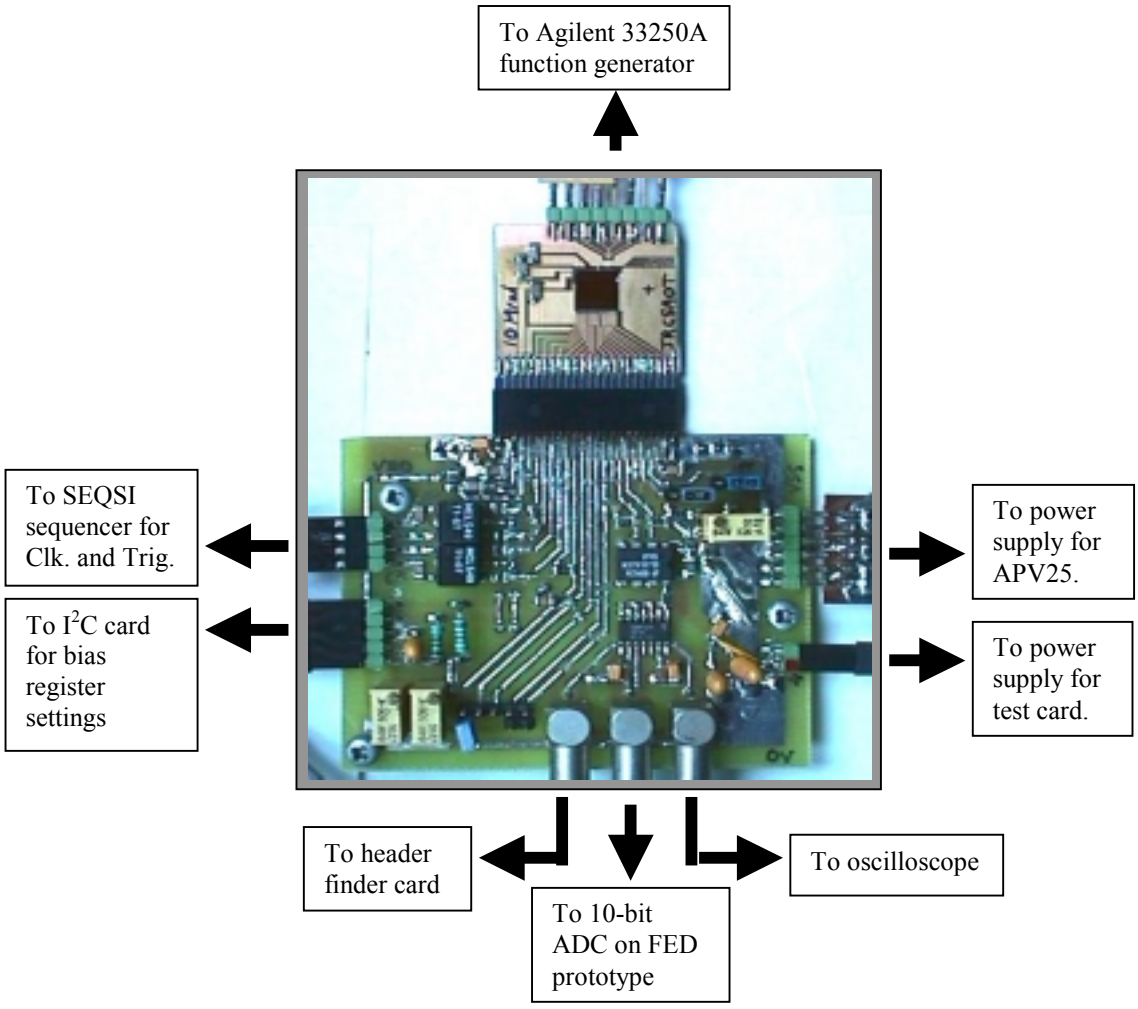


Figure 4.21: APV25 on its daughter board connected to the test card.

The daughter board containing the chip is connected to a test card which effectively acts as an interface to the various components that make-up the test setup, Fig. 4.21. A programmable multi-channel pulse generator, the Sequencer for use in Silicon readout

Investigations (SEQSI), is used to provide the 40 MHz clock and trigger (T1) signals to the chip. ECL levels from the SEQSI are converted on the test card to the LVDS levels required by the APV25. An I^2C module provides the bias register settings for the APV25. An Agilent 33250A function generator is used to inject an external pulse into one of the 128 channels on the chip. The APV25 output is wired to three lemo connectors. One of these is connected to an oscilloscope for monitoring purposes, another is connected to a custom built header finder card and the third is connected to an early Front-End Driver (FED) prototype containing a 10-bit ADC. The header finder card provides a trigger to the FED. The SEQSI, FED and I^2C cards are housed in a VME crate and controlled by an Apple Macintosh running LabVIEW. The APV25 is tested for noise, power consumption, and for its response to an external pulse and an internal calibrate pulse. The sequence is the following:

- Setting the baseline to ¼ of the full output scale;
- Tuning the pulse shape;
- Peak mode tests (external pulse, noise, calibrate pulse);
- Deconvolution mode tests (external pulse, noise, calibrate pulse).

The analogue baseline can be adjusted to lie anywhere within the digital header 8 MIP range, using the VPSP command register. The VPSP value corresponding to an analogue baseline set at ¼ of the full 8 MIP range is automatically chosen by the test setup. The analogue baseline is set three times, once before the pulse shaping procedure, once before the peak mode tests and once before the deconvolution mode tests.

Two main command registers define the pulse shape, ISHA and VFS. ISHA sets the rise time and VFS sets the shape of the tail of the pulse, though there is some interdependence between the two. The full range for the bias registers is $0 \rightarrow 255$ bits. An automatic procedure detects the best ISHA and VFS values in peak mode by cycling through ISHA values in steps of 5 and VFS values in steps of 10 and comparing each resulting pulse shape with an ideal CR-RC pulse shape.

The external pulse shape is obtained by keeping a fixed T1 and sweeping the time of charge injection, effectively changing the trigger for the Agilent 33250A. The input signal varies between –2 and 6 MIP in 0.5 MIP steps.

The internal calibrate circuit is designed to inject charge with programmable amplitude into all inputs in groups of 16 channels. The internal pulse shape is produced from a combination of a coarse mapping where the calibration request signal is set in 25 ns increments with respect to the subsequent T1 and finer mapping using an on-chip delay in steps of 3.125 ns. The internal calibrate test involves injecting charge into only one

group of 16 channels. The bias register associated with the calibrate circuit, ICAL, is set to 40 (where 25 should correspond to 1 MIP, 25 000 electrons).

The APV25 noise is measured in both peak and deconvolution modes. Three channels are bonded out and have a higher input capacitance, one channel is connected to the Agilent 33250A and the other two are connected to external capacitors. An average of 5 000 analogue frames is taken, each containing 128 channels. Common mode noise is subtracted using the following expression:

$$N_j = \sqrt{\frac{1}{N}\sum_{i=0}^{N-1}\left(A_j^i - \bar{A}_j - \frac{1}{n}\sum_{j=0}^{n-1}\left(A_j^i - \bar{A}_j\right)\right)^2} \qquad \text{..... Eq. (4.5).}$$

where N_j is the common mode noise, N is the number of frames (5 000), n is the number of channels per frame, i is the frame index, j is the channel index, A_j^i is the pedestal value for channel j in frame i, $\bar{A}_j$ is the average pedestal value for channel j.

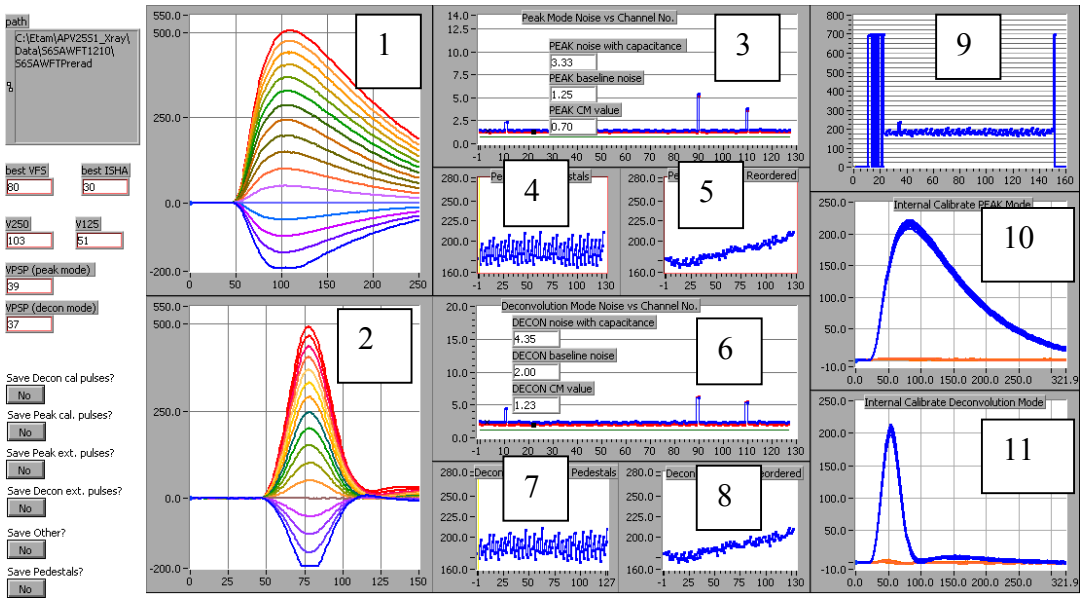


Figure 4.22: LabVIEW output.

Peak mode [Deconvolution mode]: 1 [2] Pulse shapes for externally applied signals. 3 [6] Noise. 4 [7] 128 channel pedestals, raw. 5 [8] 128 channel pedestals, re-ordered. 10 [11] Internal calibrate pulse. 9 APV25 output data stream showing digital header and analogue baseline.

In addition to the above tests, the currents drawn by the chip are recorded along with pedestals. Each chip is tested before and after irradiation and annealing. The test lasts approximately 1 hour. Fig. 4.22 shows the LabVIEW output. Data are saved in text format and analysed with Igor Pro, a data analysis package written by WaveMetrics[7].

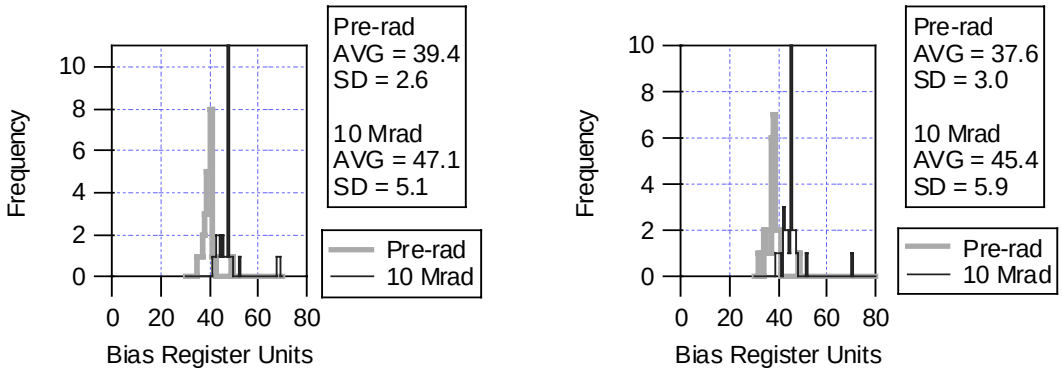
[7] WaveMetrics, Inc. PO Box 2088, Lake Oswego, OR 97035, USA. Web: wavemetrics.com.

4.3.3 10 Mrad Irradiation Results

The results in this section include all 23 chips irradiated to 10 Mrad(SiO_2).

4.3.3.1 Bias Registers

The bias registers that are modified by the automatic procedures in the test are ISHA, VFS and VPSP. These have to be changed after irradiation to maintain pre-rad characteristics such as pulse shape and baseline level. A noticeable but small increase in ISHA on average is needed after irradiation, from 28.3 to 30.7. A decrease in the value of VFS is required after irradiation, from 81.7 to 67.4. If n represents the setting for VFS, the value of the bias generator is –1.25 V + (7.5 mV × n) [126]. Δn = 14 corresponds to a shift of 105 mV. The errors on this value are large since the procedure which finds the best ISHA and VFS values increments VFS in steps of 10.



(a) VPSP, peak mode. *(b) VPSP, deconvolution mode.*

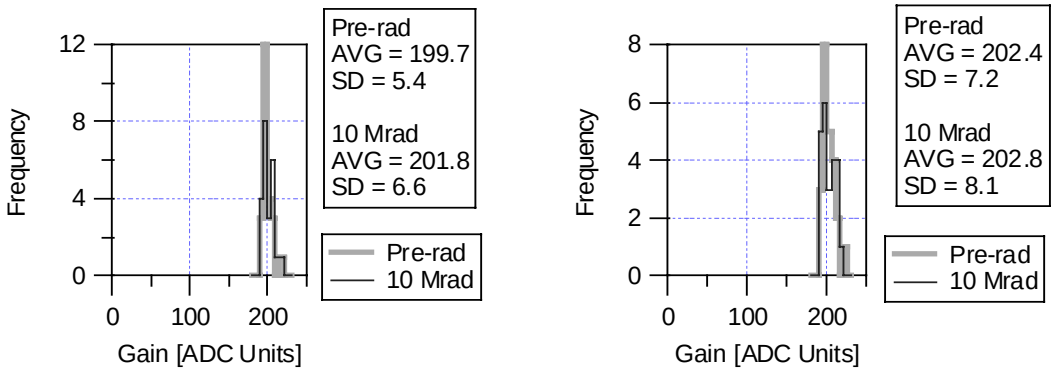
Figure 4.23: Variation of VPSP with irradiation.

A much better indicator of the shift in voltage levels for the bias generators is VPSP since it is incremented in steps of 1 by the procedure which sets the baseline at ¼ of the full output range. VPSP is set for both modes of operation of the chip and in both cases, Δn = 8, corresponding to a shift of 60 mV, Fig. 4.23. Unlike VFS, the value of VPSP must be increased after irradiation which is consistent with the expected trend, VPSP = +1.25 V – (7.5 mV × n).

The bias registers can be set anywhere between 0 and 255. In all cases, ISHA, VFS and VPSP are well within this range after 10 Mrad, which indicates that the chip can still easily be tuned after irradiation.

4.3.3.2 Externally Injected Pulse

For each pulse shape, the maximum amplitude is recorded. Fig. 4.24 shows the distribution of pulse shape maxima for the 23 chips for a 2 MIP signal. There is no significant change in the maximum amplitude of the pulse after irradiation.

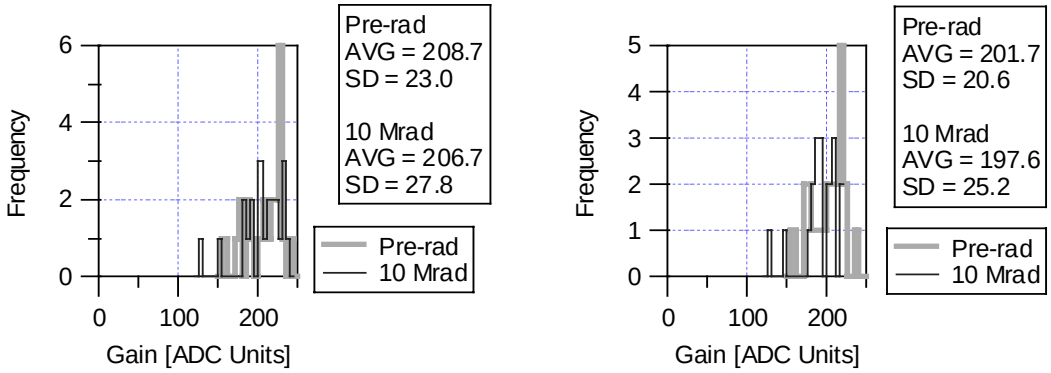


(a) Peak mode gain. *(b) Deconvolution mode gain.*

Figure 4.24: Gain for a 2 MIP external pulse.

4.3.3.3 Internal Calibrate Pulse

The distribution of the average maximum amplitude for the 16 channels, into which the internal calibrate pulse is injected, is shown in Fig. 4.25. The deconvolution mode gain has the highest change after irradiation, an average of – 2 % for the 23 chips.



(a) Peak mode gain. *(b) Deconvolution mode gain.*

Figure 4.25: Gain for a pulse injected with the internal calibrate pulse.

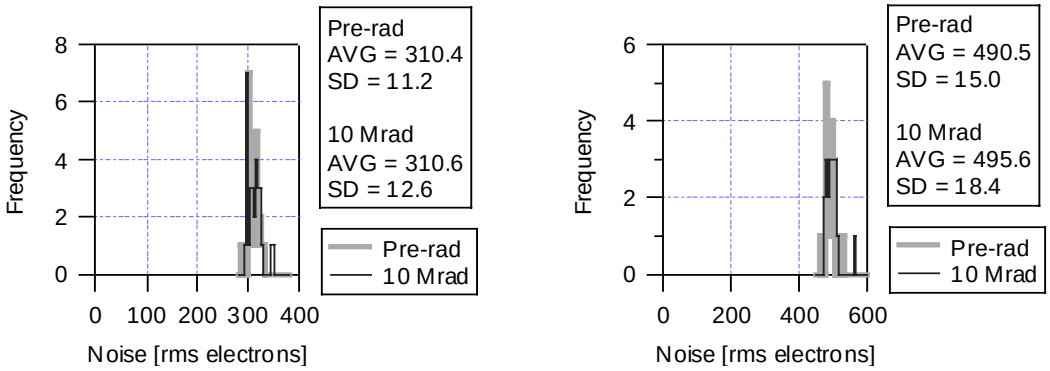
4.3.3.4 Noise

The largest average change in noise after irradiation is ~ 2 % for the 2 channels that are bonded to higher external capacitance in deconvolution mode, Table 4.6.

Table 4.6: Change in noise after 10 Mrad for all 23 chips.

	Baseline noise		High capacitance noise	
	Peak	Deconvolution	Peak	Deconvolution
Average change	0.06 %	1.04 %	–0.48 %	2.09 %
Range	–4 % → 6 %	–3 % → 6 %	–9 % → 7 %	–10 % → 15 %

In deconvolution mode, there is a relatively large spread (–10 % → 15 %) in the percentage change in high capacitance noise. The first four chips tested all show a change in noise greater than 10 %. This could be due to the fact that the testing setup was being optimised, and this noise mode (deconvolution, high capacitance) is the most sensitive to interference (on average 1111 rms electrons compared with peak mode, baseline noise of 310.4 rms electrons). For subsequent tests (the remaining 19 chips), the noise change is within ± 10 %.



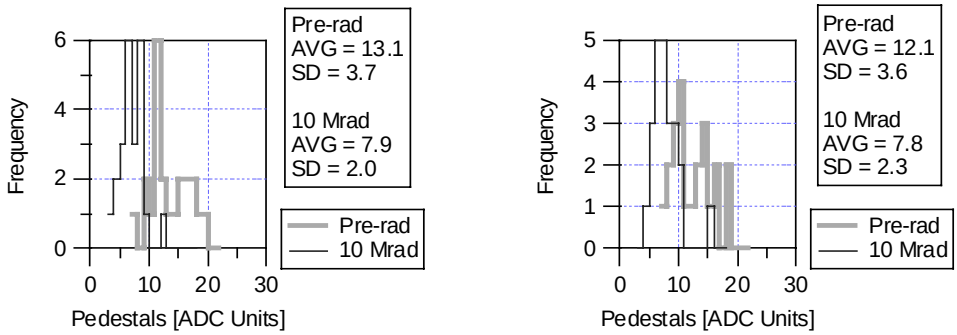
(a) Peak mode baseline noise. *(b) Deconvolution mode baseline noise.*

Figure 4.26: Baseline noise.

Fig. 4.26 shows that there is no significant change in baseline noise after irradiation. These observations are in agreement with the measurements on discrete transistors, with no change in noise anticipated after 10 Mrad(SiO_2).

4.3.3.5 Standard Deviation of Pedestals

Fig. 4.27 shows the standard deviation for the 128-channel pedestals before and after irradiation in peak and deconvolution modes. After irradiation, the standard deviation is lower, indicating a smaller spread in pedestals. An analysis of the shape of pedestals is conducted in Section 4.3.5.

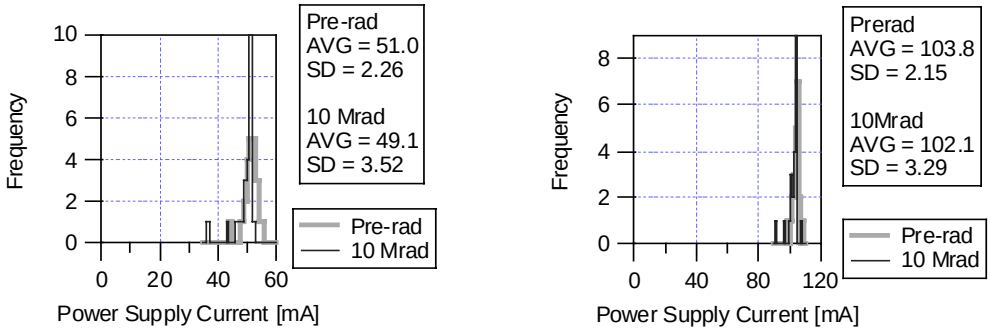


(a) Peak mode. *(b) Deconvolution mode.*

Figure 4.27: Standard deviation of the 128-channel pedestals, indicating the spread of the pedestals within the analogue output frame.

4.3.3.6 Power Consumption

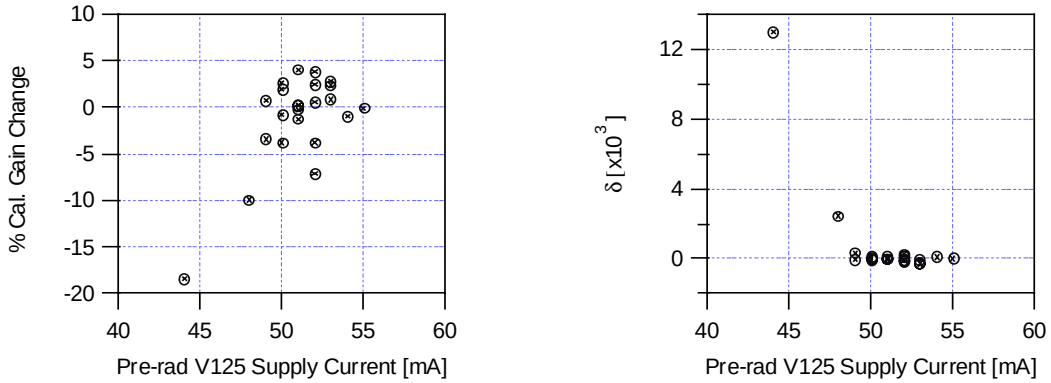
The chip is connected to a power supply with +1.25 V (V_{DD}), *GND* and –1.25 V (V_{SS}). Alternatively, all nodes can be shifted by 1.25 V, which is the convention used in CMS where *V250* corresponds to V_{DD} and *V125* corresponds to V_{SS}-V_{DD}.



(a) V125. *(b) V250.*

Figure 4.28: Power supply currents.

The power consumption decreases slightly on average after irradiation, Fig. 4.28.



(a) % change in int. cal. gain due to radiation as a function of pre-rad power consumption. *(b) δ as a function of pre-rad power consumption.*

Figure 4.29: Identifying chips that show higher than average radiation-induced changes in their characteristics.

A closer look at the bias registers, power consumption and gain shows that some chips have higher than usual radiation-induced changes. Fig. 4.29 (a) shows that with a couple of exceptions the internal calibrate gain in most chips changes by much less than ± 10 %. To parametrise general radiation effects in all chips, a variable, δ, was defined:

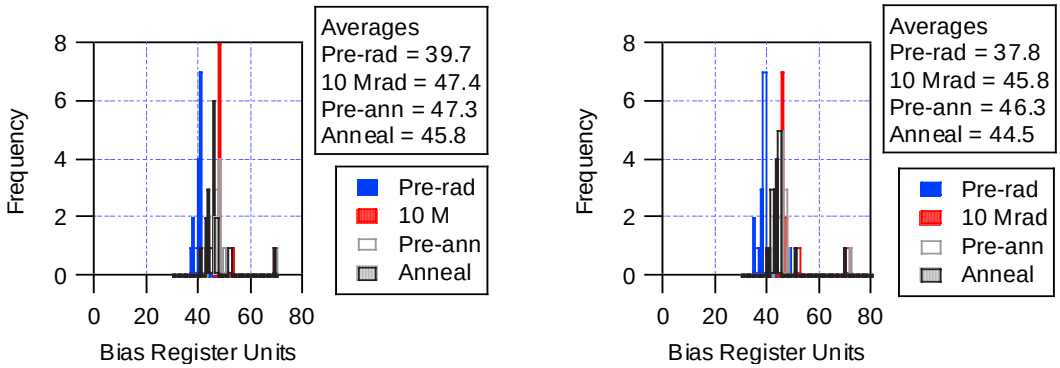
$$\delta = (\%\ \text{calibrate gain change}) \times (\%\ \text{change in VPSP}) \times (\%\ \text{change in V125})$$

Fig. 4.29 (b) shows δ plotted as a function of the pre-rad power consumption, with large values of δ for two chips. These two chips were fully operational after irradiation and in addition, since the bias registers are fully programmable, they can revert to their pre-rad characteristics following tuning of the appropriate registers. They show lower than average power consumption which might indicate that below a threshold, chips are more sensitive to radiation. This information can be used at the wafer screening stage. For example, chips that are detected with low power consumption but that otherwise pass all operational requirements at the wafer screening stage could be either kept as spares or excluded.

4.3.4 Annealing Results

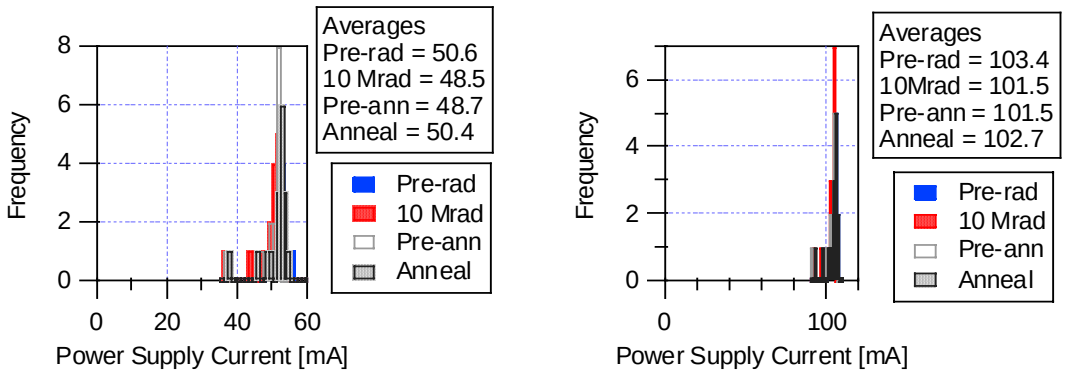
The annealing results on the chip irradiated to a final dose of 100 Mrad are presented in Section 4.3.6. Data in this section are from the 17 chips that have been annealed following irradiation to 10 Mrad.

Fig. 4.30 shows the distributions for VPSP in peak and deconvolution modes for the small sample of chips that have been annealed. The values after annealing show that there is some small recovery, corresponding to a few mV.



(a) Peak mode. *(b) Deconvolution mode.*

Figure 4.30: Changes in VPSP after irradiation and annealing.

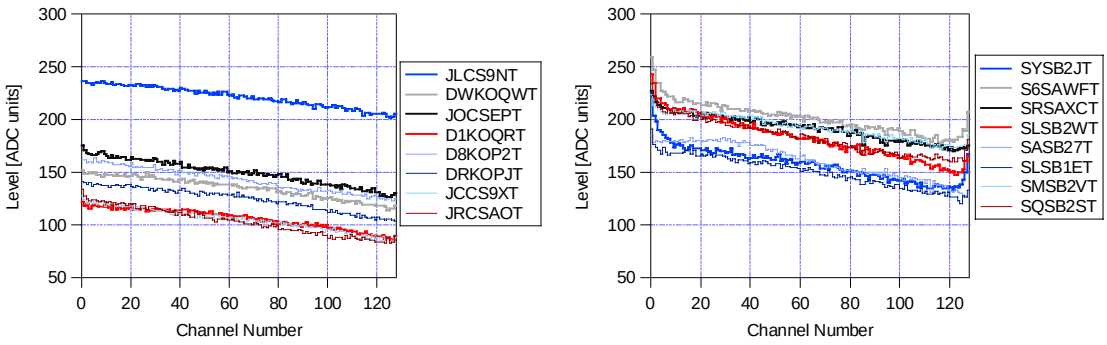


(a) V125. *(b) V250.*

Figure 4.31: Changes in power consumption after irradiation and annealing.

The power consumption after annealing shows some small recovery towards pre-irradiation values, Fig. 4.31.

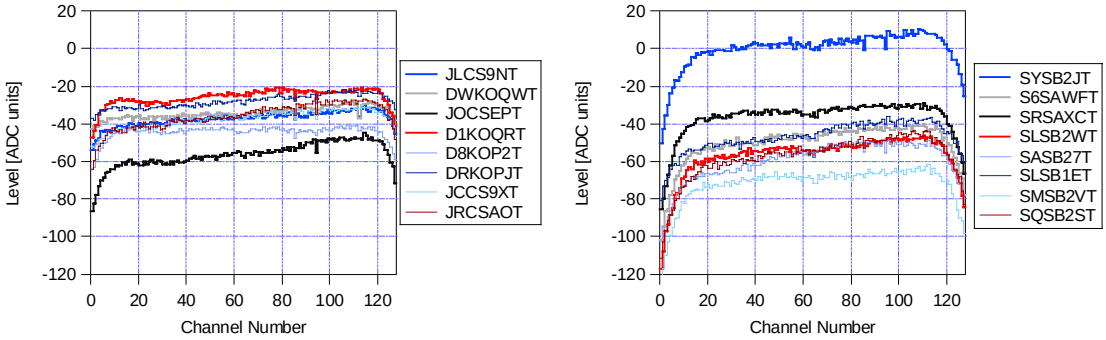
4.3.5 Pedestals



(a) Engineering run. *(b) Third production lot.*

Figure 4.32: Differences between 10 Mrad and pre-rad pedestals.

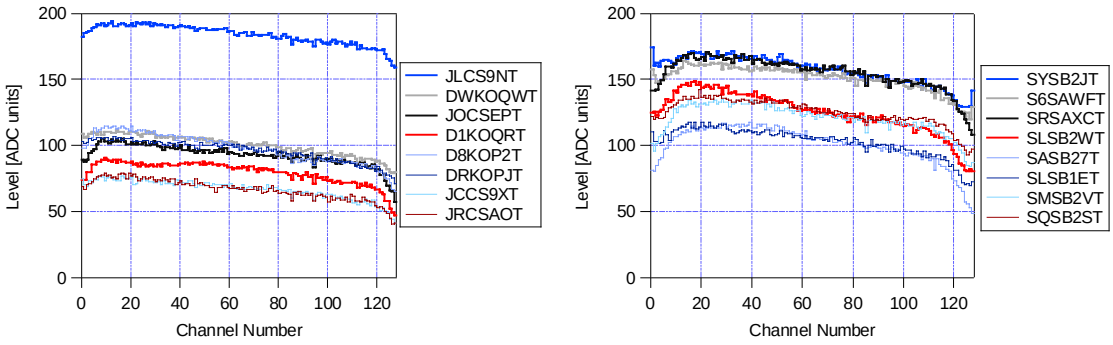
The net effect of radiation on the pedestals is shown in Fig. 4.32. The pedestals before irradiation are subtracted from those after irradiation. There is a gradient in the pedestals (–0.345 ADC units per channel) with the lower numbered channels showing higher shifts in pedestals after irradiation. This might be expected since the lowest numbered channels receive more irradation, see Section 4.3.2.1. Some of the first and last few channels show higher shifts, especially for chips from the third production lot.



(a) Engineering run. *(b) Third production lot.*

Figure 4.33: Differences between post-anneal and 10 Mrad pedestals.

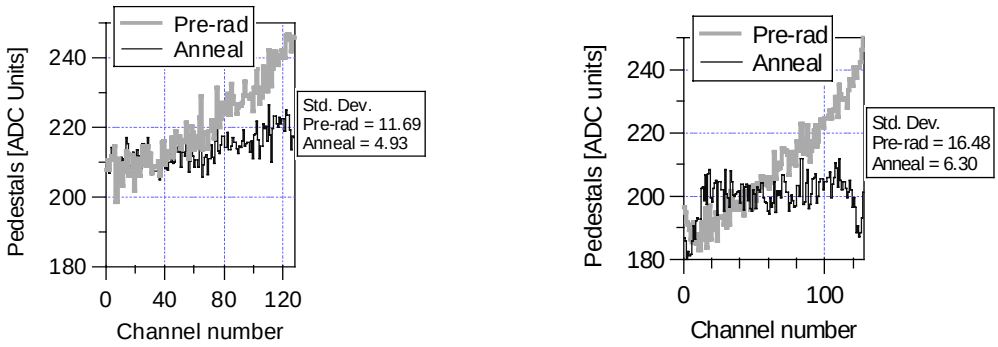
Fig. 4.33 shows the effect of annealing, with the post-irradiation pedestals subtracted from those obtained after annealing. The negative shifts indicate that there is a recovery towards the pre-irradiation values after annealing. A flat response across all channels would be expected since the annealing temperature is the same for all channels. This is not the case however. Ignoring the edge channels ($0 \rightarrow 10$ and $117 \rightarrow 127$), there is a slight gradient (0.116 ADC units per channel number), with channels towards channel 10 showing a higher recovery. Channels $0 \rightarrow 10$ and $117 \rightarrow 127$ show even higher recovery. These results seem to indicate that channels which are more sensitive to radiation-induced shifts in pedestals tend to recover more after annealing. The anomalous edge channel effect could be caused by differences between edge and interior channels due to design features (e.g. geometry, layout).



(a) Engineering run. *(b) Third production lot.*

Figure 4.34: Difference between post-anneal and pre-rad pedestals.

Fig. 4.34 shows the cumulative effects of irradiation and annealing, where the pedestals obtained before irradiation are subtracted from those obtained after annealing.



(a) Engineering run, chip DWKOQWT. *(b) Third production lot, chip SLSB2WT.*

Figure 4.35: Pedestals, pre-rad and after annealing.

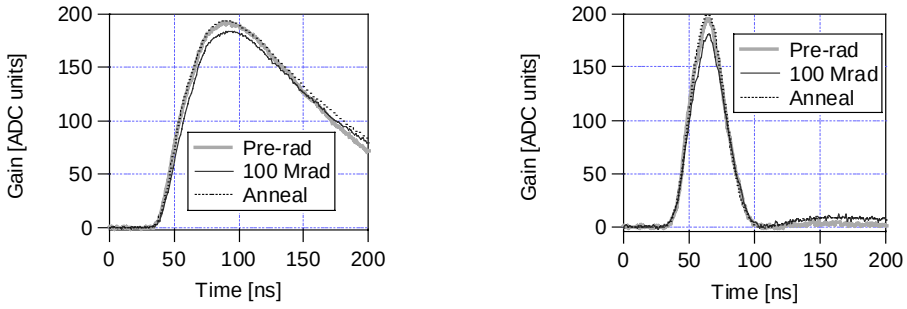
Fig. 4.35 shows the shape of the pedestals before irradiation and after annealing for two chips. Before irradiation, there is a clear pedestal gradient due to a power supply droop across the chip, reported in [125]. After irradiation and annealing, the pedestals are flatter, with a much tighter distribution and lower standard deviation. This is not an indication that irradiation and annealing improve the shape of the pedestals. It is mostly a result of the fact that the irradiation field is non-uniform and channels at the lower end of the chip receive more radiation, leading to greater shifts in that area of the chip and working to offset the initial pre-rad gradient. In a uniform irradiation field, the spread in pedestals should remain essentially the same after irradiation.

The effect observed at the edges of the chip ($0 \rightarrow 10$ and $117 \rightarrow 127$), with a lower shift after irradiation and annealing compared to channels in the middle of the chip, is not crucial in terms of chip operation. It corresponds to a shift of ~ 25 ADC units in the worst case (comparing ch.115 with ch.127 on chip SLSB2WT) compared with the ~ 70 ADC units range of the pre-rad pedestals.

Before irradiation, pedestals are very stable and are unique to a chip. It was previously thought that they offered a means of identifying a chip, acting as a fingerprint [124]. This technique could have helped identify a chip on a detector module in the Tracker for monitoring purposes. The shape of pedestals is clearly affected by radiation, which puts a limit to the use of this identification technique once the chips have been irradiated.

4.3.6 100 Mrad results

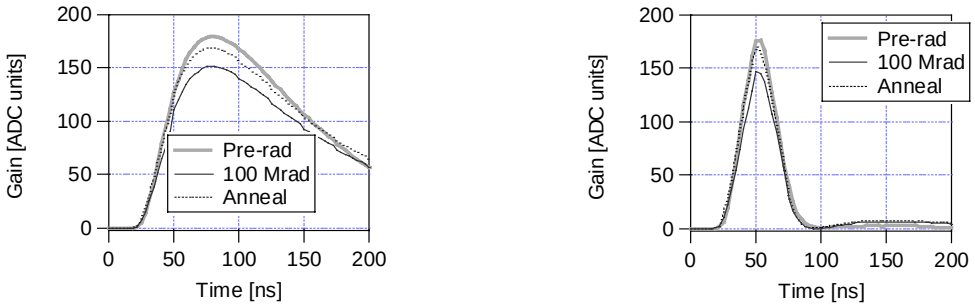
An APV25 was irradiated in several steps to 100 Mrads and annealed.



(a) Peak mode. *(b) Deconvolution mode.*

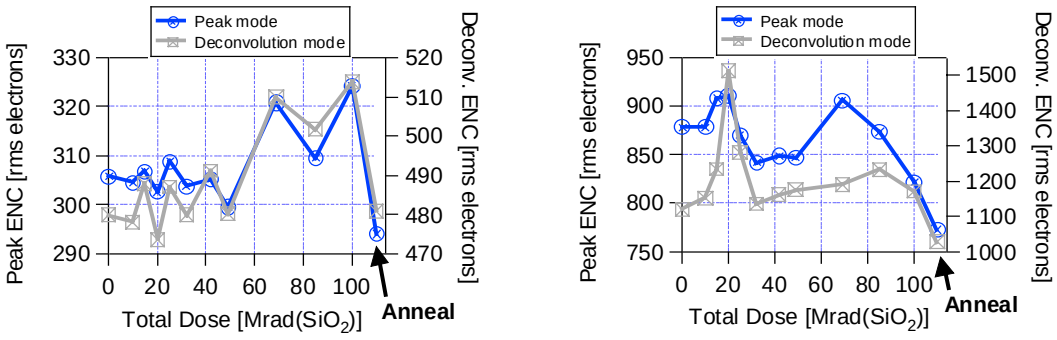
Figure 4.36: Pulse shape following 100 Mrad exposure, 2 MIP.

Fig. 4.36 shows the pulse shapes for a 2 MIP externally applied pulse. There is very little degradation in the gain after 100 Mrad and the output obtained after annealing is virtually indistinguishable from that obtained before irradiation. Fig. 4.37 shows the response to an internal calibrate pulse. There is a significant loss in gain after irradiation with a small recovery after annealing in both peak and deconvolution modes.



(a) Peak mode. *(b) Deconvolution mode.*

Figure 4.37: Internal calibrate pulses following 100 Mrad exposure.

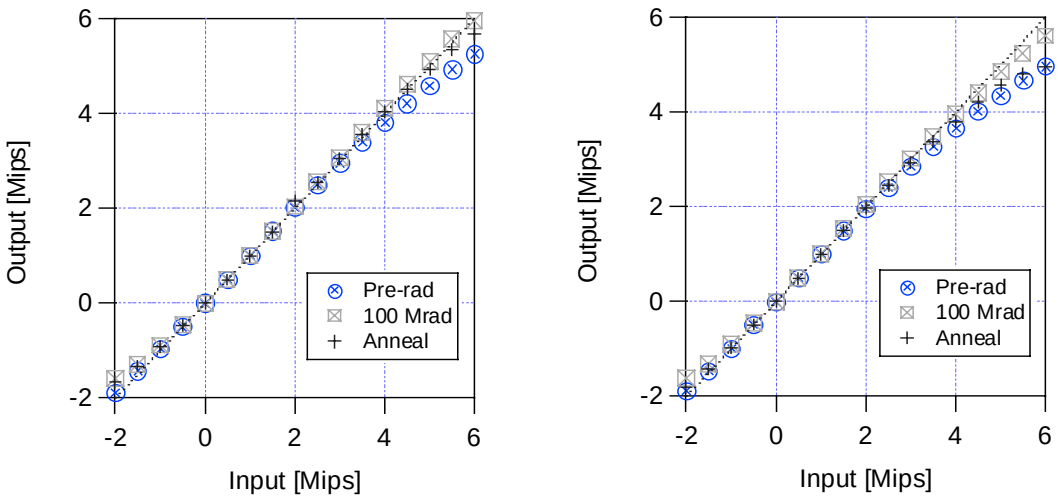


(a) Baseline noise. *(b) Two channels with high capacitance.*

Figure 4.38: Noise dependence on total dose.

Fig. 4.38 shows the baseline noise and the noise for the two channels with high input capacitance. After irradiation, it is within ± 10 % of its value before irradiation.

The maximum output amplitude as a function of input signal amplitude is shown in Fig. 4.39 where the output has been normalised to the 1 MIP output amplitude. The results suggest that linearity does not degrade after irradiation and annealing and are consistent with previously reported observations for non-irradiated chips with good linearity over a 3 MIP range (–1 MIP to 2 MIP) and a gradual fall-off beyond this range [125].



(a) Peak mode. *(b) Deconvolution mode.*

Figure 4.39: Linearity.

4.4 Summary

The extensive total dose tests conducted on individual transistors have revealed small threshold voltage shifts and very little change in the noise characteristics after 10 Mrad(SiO_2). As was expected from these results, tolerance of the APV25 to the total dose levels to which it will be subjected has been demonstrated, with no significant degradation after 10 Mrad(SiO_2). No correlation has been found between sensitivity to radiation damage and low yield areas in the cases where chips were chosen from areas of low yield.

Chapter 5
SEU and SEGR Results

Measurements of the SEU saturation cross-section and threshold LET were made at heavy ion and pion beam facilities with tests on the APV25. The susceptibility to SEGR was inferred from the SEU tests and from measurements on discrete transistors.

5.1 Single Event Upsets in the APV25

The ideal SEU measurement is the SEU rate in a radiation environment equivalent to that of the final system, for example low energy protons and pions for LHC applications. An alternative is the use of heavy ions, which allows a measurement of the dependence of upset cross-section on incident LET by varying the ion species and beam energies to cover a wide LET range.

Typically, for heavy ion SEU data, the upset cross-section, σ, of the device is plotted as a function of ion LET and is fitted with the widely used Weibull function. However, the Weibull function has no underlying physical significance, although it provides a convenient method for parameterising data and extracting the threshold LET and saturated cross-section.

To predict the upset rate in the complete CMS Tracking system, a full evaluation of the digital circuits in the APV25 has been performed by exposing the chip to a beam of heavy ions and to 300 MeV/c pions. Extensive simulations of SEU in the APV25 were carried out and a model was developed to predict upset cross-sections. The model provides a physically meaningful alternative to the Weibull fit, based on the concept of multiple upset modes within a sensitive storage cell.

5.1.1 Simulations of SEU in the APV25

In the APV25 the sources of SEU are digital pointers of the pipeline memory, the FIFO address memory, the I^2C control logic and data registers and main control logic. They comprise three types of digital memory element: simple D Flip-Flop (DFF), D Flip-Flop with set (DFF-set) and D Flip-Flop with reset (DFF-reset). Each circuit responds differently to deposited charge with characteristic upset thresholds and cross-sections, even though underlying physical mechanisms are identical in each case. Each type of DFF contains master and slave sections, with either being vulnerable to SEU depending on the state of the clock. The I^2C registers are clocked only during the chip set-up

procedure. Consequently only the slave need be considered when predicting the behaviour of the I^2C registers. Simulations of the I^2C registers, which are made up of simple DFFs, are presented here.

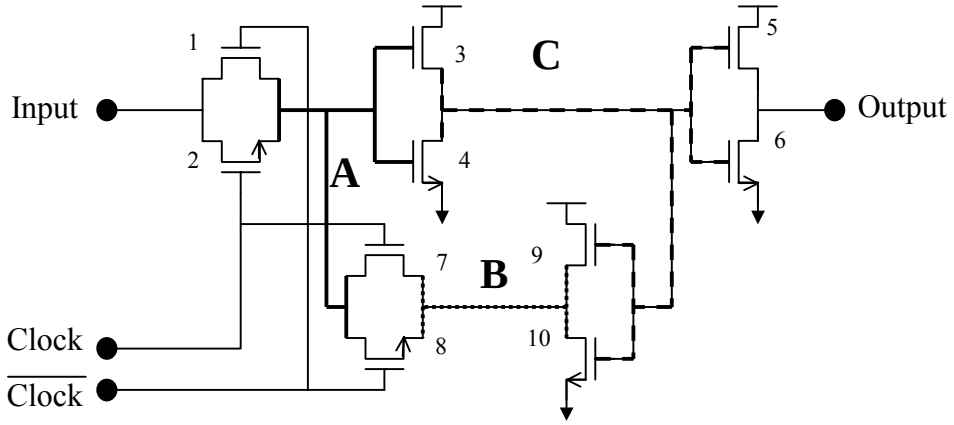


Figure 5.1: Schematic of a simple DFF slave.

In the simple DFF, there are three nodes where charge can give rise to an upset, which are labelled A, B and C in Fig. 5.1. Each node has two critical charges, one for the state transition 1 to 0, and the other for 0 to 1. Table 5.1 summarises the sensitive implants, the transistor and node to which they belong, and their surface area. By summing the appropriate combination of areas, an estimate of the normal incidence upset cross-section can be made.

Table 5.1: Sensitive implants of the simple DFF.

Sensitive implant	Implant type	No. of transistor	Node	Surface area [μm^2]
1	n-source	2	A	3.85
2	n-drain	4	C	0.65
3	n-drain	8	A	0.65
4	n-source	8	B	3.85
5	n-drain	10	B	0.65
6	p-source	1	A	4.97
7	p-drain	3	C	2.77
8	p-drain	7	A	1.96
9	p-source	7	B	4.97
10	p-drain	9	B	2.77

To establish the critical charge, Q_{crit}, for each mode the circuit was modelled in HSPICE[8]. A software tool for simulating semiconductor devices called EVEREST[9] was used to investigate the charge collection efficiency of both n- and p-implants. The simulations were based on some assumptions of transistor geometry and doping because

[8] HSPICE, META-SOFTWARE, INC. 1300 White Oaks Road, Campbell, CA 95008, USA.
[9] J.V.Ashby, R.F.Fowler and C.Greenough, Mathematical Software Group, Department for Computation and Information, Rutherford Appleton Laboratory, Chilton, DIDCOT, Oxfordshire, OX11 0QX, U.K.

of the restricted access to process details by the manufacturers. The transistor geometry was modelled on an NMOS transistor from the APV25 digital circuitry (channel length = 280 nm, width = 3.2 μm, drain area = 0.652×10^{-12} m^2, source area = 4.36×10^{-12}m^2), Fig. 5.2. For NMOS (PMOS) transistors, doping levels were N_A (N_D) = 2×10^{16} cm^{-3} and N_D (N_A) = 9×10^{17} cm^{-3}.

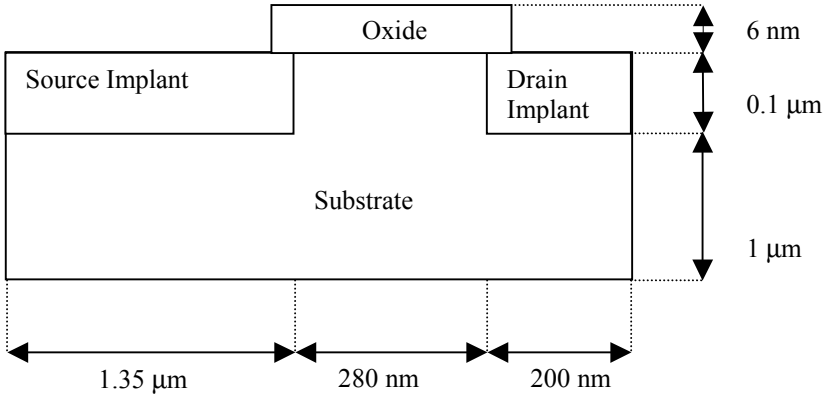


Figure 5.2: Transistor geometry used in EVEREST simulations.

In this study, charge was deposited beneath the drain implant, approximately 0.8 μm from the drain implant/substrate interface. The exact location is not important since the main objective was to look at the difference in charge collection between NMOS and PMOS transistors.

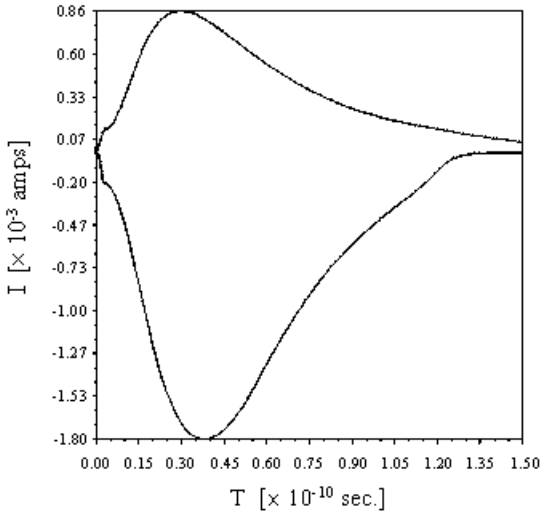


Figure 5.3: EVEREST output after a charge deposition event of 1.5 × 10^6 electrons. The positive going line is the PMOS device hole current at the drain, the negative going line is the NMOS device electron current at the drain.

Fig. 5.3 shows charge collection for the deposition of 250 fC, equivalent to 1.5×10^6 e$^-$. The charge collection efficiency was found to be 48 % for p-implants and 95 % for n-implants.

Table 5.2 shows, for each mode of upset, the simulated critical charge, the sensitive areas and the implant type in which the charge must be collected. It is clear that there should be a number of distinct modes of upset each with a different threshold LET.

Table 5.2: Sensitive area and critical charge for six modes in a DFF slave.

	Upsets from 1–0			Upsets from 0–1		
	Q_{crit} [fC]	n or p	σ [μm^2]	Q_{crit} [fC]	n or p	σ [μm^2]
Hit on A	196	n	7.7	212	p	9.94
Hit on B	304	n	1.3	306	p	4.73
Hit on C	284	p	2.77	260	n	0.65
Total	–		11.77	–		15.32

The theoretical SEU curve can be determined by converting Q_{crit} into an equivalent threshold LET and by choosing appropriate values for the saturating SEU cross-section for each mode. Since 3.6 eV is required to generate an electron/hole pair in silicon, the equivalent LET is given by:

$$LET_{th} = \left[\frac{Q_{crit}}{\alpha e} \times 3.6 \right] \frac{1}{z\rho} \qquad \text{.....eq. (5.1).}$$

where the quantity in brackets is the critical energy, E_{crit}, α is the charge collection efficiency from the EVEREST simulations, Q_{crit} is the critical charge from the SPICE simulations, z is the sensitive depth of the implants (the charge collection depth) and ρ is the density of silicon.

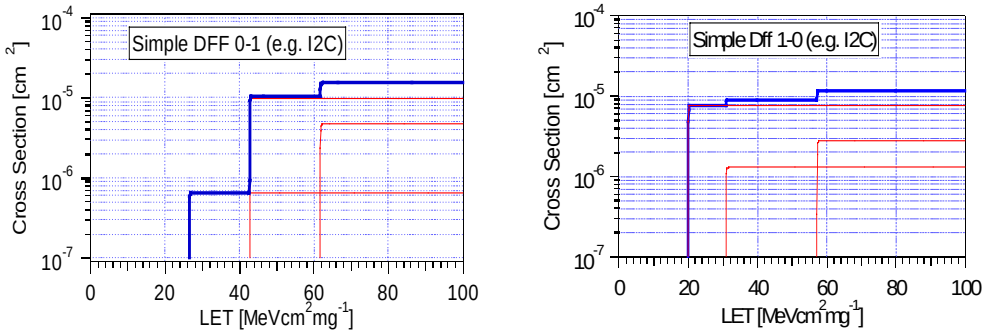
The predicted sensitive areas were taken to be the sum of the areas of the sensitive implants and are equivalent to the heavy ion SEU cross-section. The I^2C registers are programmable and therefore their state is known and the appropriate saturating cross-section was calculated to be σ= 1566 μm^2.

Using the assumption that each mode has a threshold LET before which no SEUs occur and after which the saturating cross-section is reached (i.e. an abrupt step-like function), the total SEU cross-section can be obtained by summing cross-sections for each mode:

$$\sigma = \sum_{i=0}^{N_n} \sigma_n^i (LET) + \sum_{i=0}^{N_p} \sigma_p^i (LET) \qquad \text{..... eq. (5.2).}$$

where N_n is the number of n-modes and N_p is the number of p-modes. 1–0 and 0–1 transitions must be considered separately. Each component of σ_n^i and σ_p^i can be represented by a single Weibull function, eq. (2.21), and each mode has its own values of LET_{th} and σ_{sat}.

Cross-section predictions for a simple DFF for both 0 → 1 and 1 → 0 transitions are shown in Fig. 5.4 assuming a sensitive depth of 1 µm, as proposed for a 0.6 µm process [127] and used since for 0.25 µm technologies [54].



(a) 0 → 1 transitions. *(b) 1 → 0 transitions.*

Figure 5.4: SEU Cross-sections predicted by the model.

They illustrate the contribution of different modes for (a) 0 → 1 transitions and (b) 1 → 0 transitions in a simple DFF.

5.1.2 Heavy Ion Beam Tests

Heavy ion irradiations were performed at the SIRAD irradiation facility located at the 15 MV Tandem accelerator of the INFN Legnaro National Laboratory (LNL) in Italy. Four APV25 chips were subjected to high fluences from heavy ions with varying LET values. Aluminium masks, ~1 mm thick, were machined to expose specific areas of the four chips in the beam, namely the pipeline logic, FIFO, I^2C registers and control logic, Fig. 5.5.

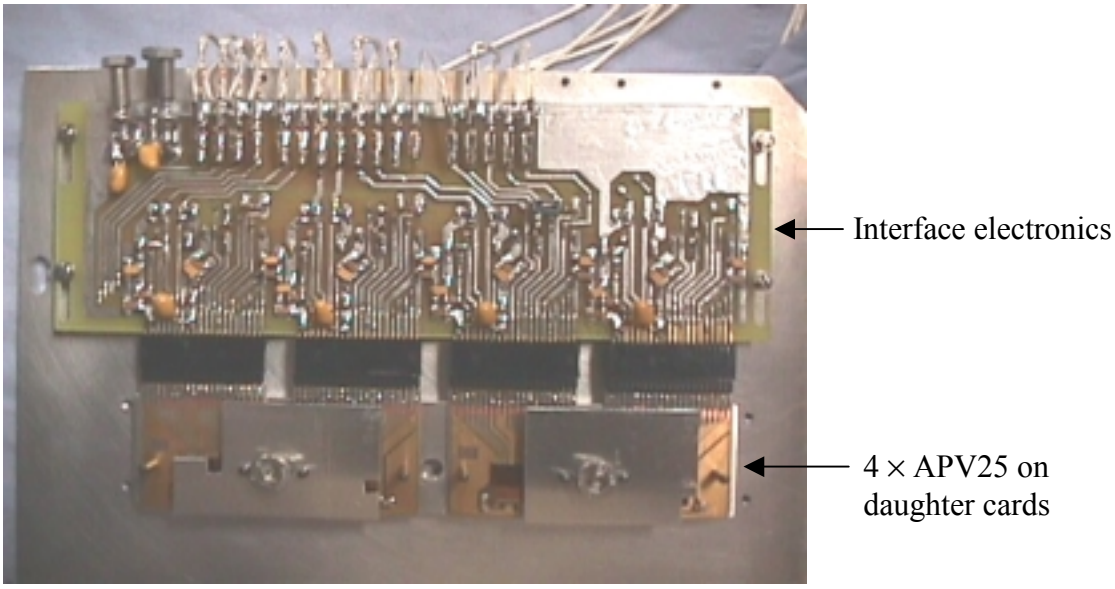


Figure 5.5: APV25 SEU test board containing interface electronics, four APV25 chips and precision-machined masks obscuring most of the APV25s.

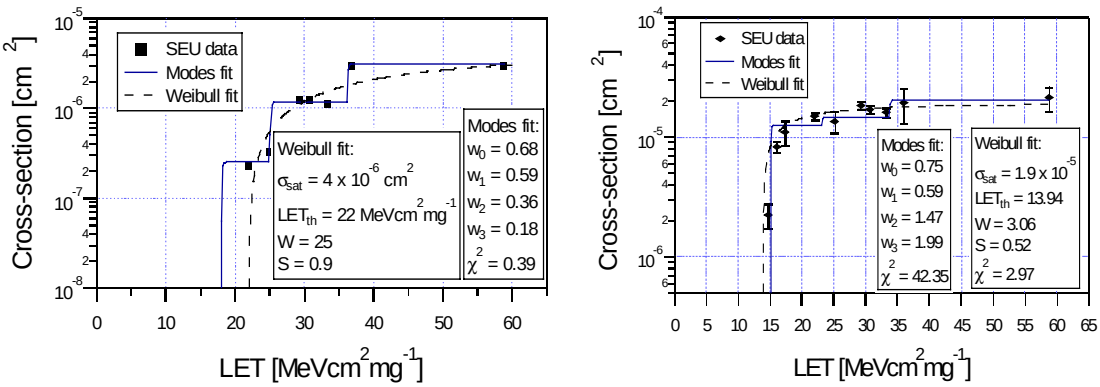
Table 5.3 gives a summary of the ion species used, along with their effective LETs and the total fluences reached. The effective LET in the sensitive volume (SV) takes into account the slight loss of energy in the material above the SV.

Table 5.3: Fluences received by the four APV25 chips.

Ion Details				Fluence [cm^{-2}]			
Ion	A	Effective LET $MeV.cm^2.mg^{-1}$	Energy [MeV]	Pipeline logic	FIFO & I^2C registers	Control logic	Whole chip
Si	28	9.7	145	1.7×10^9	5.5×10^8	–	–
		11.2	100				
Cl	35	13.5	160	8.3×10^8	1.1×10^9	–	–
		14.8	130	1.2×10^8	3.4×10^8	3.8×10^8	2.9×10^8
		16.1	107	9.3×10^7	6.6×10^8	4.8×10^8	6.9×10^8
		17.4	87	8.6×10^7	1.4×10^8	3.2×10^8	1.8×10^8
Ti	48	22	178	3.5×10^8	2.1×10^9	6.1×10^8	7.0×10^8
		25.2	115	1.7×10^8	3.7×10^8	5.2×10^8	2.0×10^8
Ni	59	29.3	237	1.4×10^8	8.4×10^8	3.6×10^8	4.0×10^8
		30.7	200	2.3×10^9	8.9×10^8	–	–
		33.3	138	2.5×10^8	7.1×10^8	4.4×10^8	2.8×10^8
Br	80	36	100	1.6×10^9	8.2×10^8	–	–
I	127	58.8	250	6.0×10^7	9.4×10^7	2.2×10^8	9.0×10^7
All	–	–	–	7.7×10^9	8.6×10^9	3.3×10^9	2.8×10^9

SEU events in the I^2C registers can be observed by writing defined values, reading back after an interval, and comparing with initial values. In this case it is possible to detect individual bits that have been upset. For the I^2C test a simple 8-bit pattern is written followed by the sensitive time (ST), an interval during which SEUs can occur, and then a read. The number of upsets per ST is kept well below 1 on average to make sure that only one error, and not more, is registered, effectively preventing undercounting. The ST is on the order of a few μs and the bit pattern can be varied to establish the cross-section for both 1 to 0 and 0 to 1 transitions.

All cross-sections in this section are plotted against effective LET. Fig. 5.6 shows the SEU cross-sections in the I^2C registers for $0 \rightarrow 1$ transitions and for $1 \rightarrow 0$ transitions. The I^2C registers illustrate clearly the effects predicted in Section 5.1.1. As expected, it is difficult to see any structure in the data for upsets from 1 to 0. However comparing Figs. 5.4 (b) and 5.6 (b), it can be seen that the overall shape is similar to expectations. The data for $0 \rightarrow 1$ transitions display clear steps very close in appearance to predictions, Figs. 5.4 (a) and 5.6 (a).



(a) 0 → 1 cross-section. *(b) 1 → 0 cross-section.*

Figure 5.6: I^2C registers cross-section vs. LET, showing Weibull and Modes fits.

For all circuits in the APV25, the observed threshold LET is greater than 13 MeV.cm^2.mg^{-1}. This is much higher than the threshold LET of ~ 4 MeV.cm^2.mg^{-1} reported for different designs of memory cells in the same 0.25 μm technology by [128]. The decreased SEU sensitivity of the APV25 can be attributed to the increased transistor size typical of the use of radiation tolerant layout rules, which leads to increased parasitic capacitance and drive capability.

By fitting both a single Weibull function and the predictions of the model developed in Section 5.1.1, a comparison can be made. The cross-sections from the model are calculated from:

$$\sigma = w_2 \sum_{i=0}^{Nn} \sigma_n^i \left(LET, w_0\right) + w_3 \sum_{i=0}^{Np} \sigma_p^i \left(LET, w_1\right) \qquad \text{.....eq. (5.3).}$$

where N_n is the number of n-modes and N_p is the number of p-modes. Each of the $N_{n/p}$ components of σ_n^i and σ_p^i can be represented by a single Weibull function:

$$\sigma_{n,p}^i = \sigma_{nsat,psat}^i \left(1 - \exp\left\{-\left[\frac{LET - \left(w_{0,1} LET_{nth,pth}^i\right)}{W_{n,p}}\right]^{s_{n,p}}\right\}\right) \qquad \text{.....eq. (5.4).}$$

Each mode has its own values of LET_{th} and σ_{sat}, taken directly from the simulations. W_n, W_p , s_n and s_p are fixed parameters whose values were chosen to make the individual Weibull functions close approximations to step functions for computational convenience.

The fitting parameters *w0* and *w1* vary LET thresholds for the n and p modes individually to account for the difference between the true sensitive thickness and the assumed value of 1 μm. Therefore the true sensitive thickness, for both n and p modes, can be extracted after fitting and is given by the inverse of *w0* and *w1*. *w2* and *w3* perform the same function for the saturating cross-section. Values of *w0* and *w1* were chosen to position the steps to correspond to observed steps in the data.

In Fig. 5.6 (a) which shows the $0 \rightarrow 1$ cross-section for the I^2C registers, both Weibull and model fits describe the data with small χ^2 but visually the measured points display clear plateaus which match the theory. Extracting the sensitive depths gives 1.47 ± 0.15 μm for the n modes and 1.69 ± 0.09 μm for the p modes. Fig. 5.6 (b) shows the $1 \rightarrow 0$ cross-section for the I^2C registers fitted with a Weibull function and the model. These data demonstrate that low statistics (due to the low cross-section) combined with expected small steps (Section 5.1.1) can make it difficult to see structure in the data, and in this case neither fit is more convincing. The extracted sensitive depths are 1.33 ± 0.02 μm for the n modes and 1.69 ± 0.09 μm for the p modes.

All the extracted values of σ_{sat} are shown in Table 5.4 along with geometrical predictions, which are taken as the sum of the sensitive areas from all modes. The pipeline and I^2C σ_{sat} predictions are close to the measured values with the exception of the I^2C $0 \rightarrow 1$ transitions. The average predicted SEU cross-section for the APV25 in the Tracker is $\sim 10^{-12}$ cm^2.

Table 5.4: Comparison between predicted and measured cross-sections. Statistical errors are smaller than the precision of the values quoted.

	σ_{sat} [cm^2]				
	Pipeline	FIFO	I^2C ($1 \rightarrow 0$)	I^2C ($0 \rightarrow 1$)	Control
Predicted	1.1×10^{-4}	8×10^{-6}	1.3×10^{-5}	1.7×10^{-5}	2.3×10^{-5}
Measured	1.0×10^{-4}	3×10^{-6}	2.1×10^{-5}	0.3×10^{-5}	0.7×10^{-5}

From the heavy ion cross-section data and CMS simulations of secondary particle energy spectra [52], upset rates for the APV25 during CMS operation can be calculated. Table 5.5 shows the predicted SEU rates in the CMS Tracker.

Table 5.5: Predicted upset rates in the CMS Tracker.

Tracker region	No. APVs	No. SEU/layer/s	Seconds/SEU	No. SEU/hour	Fraction chips/hour
Inner barrel	14400	1.46×10^{-2}	68.6	52	0.36 %
Outer barrel	29232	4.1×10^{-3}	243.7	15	0.05 %
Inner endcap	4416	5.15×10^{-3}	194.2	19	0.42 %
Forward endcap	30208	8.58×10^{-3}	116.5	31	0.10 %
Total	78256	3.24×10^{-2}	30.9	116	0.15 %

To verify the predicted rates, a measurement of the cross-section in a representative radiation environment was made by exposing APV25 chips to a 300 MeV/c pion beam at the PSI, which is the closest environment to that of the Tracker in energy of particles.

5.1.3 Pion Beam Test

A 300 MeV/c pion beam test was carried out at the πE1 beam line of the Paul Scherrer Institute (PSI) in Switzerland to study SEUs in eight APV25 chips. A total fluence of $\sim 2 \times 10^{14}$ cm^2 was accumulated in several runs with an average flux of 10^9 cm^{-2}.s^{-1}. The eight chips tested were operated in a cooled environment at –10 °C with a dry nitrogen atmosphere for approximately two thirds of the measurement time. The temperature was around 20 ^{o}C during the remaining measurement period.

The pion beam test consisted of a measurement loop used for all chips. When an error was detected, it was examined and the details stored, following which all chips were reset and initialised. The chips were read out at a rate of several hundred Hz.

In total, about 3000 SEUs were observed on all eight APV25 chips, or approximately one in 10^5 events. Since 300 MeV/c pions penetrate several cm of material, masking specific areas of the chips was not possible. From the event analysis, the origin of the upset could only be partially reconstructed since it was not possible to distinguish between errors in the pipeline and those in the control logic blocks. It is therefore only possible to state a combined error rate in contrast to the heavy ion tests.

The cross-section at 20 ^{o}C is $\sigma = 1.99 \times 10^{-12}$ cm^2 and is $\sigma = 2.25 \times 10^{-12}$ cm^2 at –10 ^{o}C. The pion cross-section is lower than with heavy ions by a factor of approximately 10^8 due to the fact that only secondary reactions (such as recoil Si atoms) deposit sufficient charge for an upset while ordinary pion interactions produce mostly minimum ionising secondaries. 96 % of all upsets affect the data flow either in the pipeline logic, the FIFO or the control logic. The remaining SEUs were observed in the I^{2}C registers.

It is possible to directly extrapolate the pion SEU cross-section to obtain the upset rates in the CMS Tracker. Since neither particle types nor energy spectra are taken into account, this simple prediction should be regarded as a worst-case scenario including a considerable safety margin with respect to normal CMS operation. Table 5.6 shows the predicted SEU rates in two sub-sections of the CMS Tracker. These rates are up to a factor 3 higher than the more detailed extrapolation of Table 5.5.

Table 5.6: Predicted SEU rates in the CMS Tracker calculated from the pion SEU cross-sections.

Tracker region	Avg. flux [cm^{-2}s^{-1}]	No. APVs	Seconds/SEU	No. SEU/hour	Fraction chips/hour
Inner barrel	1.04×10^6	14400	29.7	121	0.84 %
Outer barrel	1.80×10^5	29232	84.7	43	0.15 %

5.2 Single Event Gate Rupture Results

5.2.1 Speculative Oxide Breakdown Mechanism

It has been suggested that the gate oxide of the 0.25 μm CMOS process might suffer a local catastrophic failure when exposed to CMS particle fluences. Such a failure mode was attributed to the type of damage clusters normally associated with crystalline silicon which might allow an electrical short to develop across the oxide. The oxide is usually assumed to be amorphous and it is therefore difficult to know with confidence whether ideas on cluster formation in silicon can be related to oxides. The following assumptions were made to estimate the magnitude of such an effect, based on a simple linear model:

- Bulk damage clusters are 5 → 10 nm in linear dimensions;
- On average, about 3 clusters are produced per knock-on atoms;
- 240 MeV/c pions are equivalent to 1 MeV neutrons in numbers of clusters per incident particle;
- The cross-section of 1 MeV neutrons on silicon is about 3 barn;
- For σ = 3 barn, mean free path in silicon $\lambda \approx 7$ cm (= $1/n\sigma$, $n = N_0.\rho/A$).

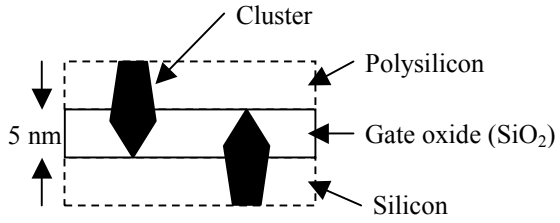


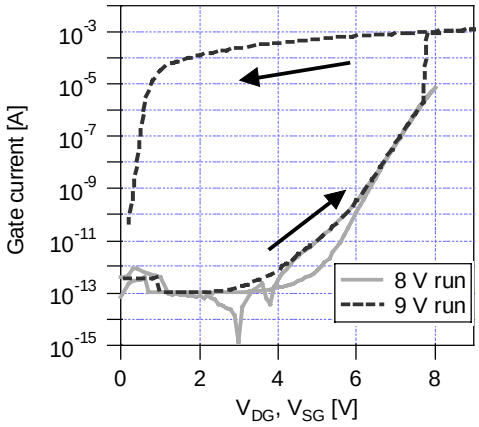
Figure 5.7: Schematic diagram of cluster damage in the gate oxide.

The gate oxide is ~ 5 nm thick. For a 10 nm cluster size, the thickness of interest for possible interactions generating knock-on atoms (in the oxide or 5 nm of material on either side) is 15 nm, Fig. 5.7. There are 3 clusters per incident particle. Assuming that an overlapping cluster has 100 % chance of causing such oxide damage, the probability of a cluster in the region of interest per incident neutron is $\approx 3 \times 15$ nm/7 cm $\approx 6.4 \times 10^{-7}$. This corresponds to $\approx 1.6 \times 10^{6}$ neutrons (pions) incident per oxide puncture.

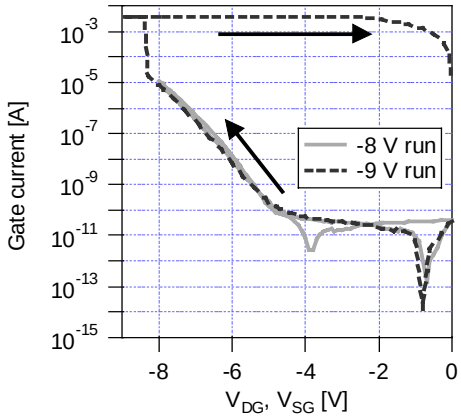
The uncertainties in this calculation are large and a model based on a super-cluster with a tree-like configuration could be more appropriate. It therefore seems reasonable to adopt a value of $10^{6\pm1}$ neutrons(pions)/oxide puncture.

5.2.2 SEGR in Discrete Transistors

As was seen in Section 2.2.2.2, the breakdown field, E_0, is a good indicator of the robustness of a given oxide. A batch of transistors was tested to determine their intrinsic gate oxide breakdown voltage. The test consisted of applying an initial gate bias to the transistor, usually 0 V, increasing this bias in steps of 100 mV up to a user defined maximum bias and ramping the bias in steps of 100 mV back to its initial level. Runs were taken with different values for the maximum bias until a high enough maximum bias was selected that caused a gate breakdown. The oxide was considered defective when the gate current remained high for bias values between maximum and initial.



(a) Unbonded PMOS, D10.



(b) Bonded NMOS, N1.

Figure 5.8: Oxide breakdown tests in the lab.

In Fig. 5.8, it can be seen that no breakdown occurs for the $0 \rightarrow 8 \rightarrow 0$ V sweep whereas the $0 \rightarrow 9 \rightarrow 0$ V sweep does cause a breakdown. In all transistors tested, the breakdown voltage was observed to be greater than 7.5 V, corresponding to a breakdown field of 15 MV/cm. The corresponding breakdown current is > 1 μA.

Discrete transistors were placed behind the stack of eight APV25s during the pion beam test described in Section 5.1.3. The aim was to try and detect SEGR by applying a constant bias across the gate and measuring the gate current to identify any breakdowns, characterised by a non-reversible high-current state.

Table 5.7 lists all the transistors that were exposed to the pion beam. Chips 10, 11 and 12 are identical and therefore contain the same number of transistors. Because transistors of a similar type share common gate and source terminals, the gate area quoted in Table 5.7 is the sum of all gate areas for the particular type of transistor (e.g. the PMOS gate area is the sum of 11 PMOS transistors that share a common gate). Some of these were not biased during irradiation. They were all tested after irradiation and a few showed failures which are most likely due to handling problems since none of

the transistors carried ESD protection measures. None of the transistors suffered breakdowns during their exposure to pions.

Table 5.7: Transistors exposed to the pion beam.

Values corresponding to the exposure times during which the transistors were biased are in bold font.

		Chip 10	Chip 11	Chip 12
PMOS	Gate area [μm^2]	5420	5420	5420
	Fluence [cm^{-2}]	1.26×10^{13} **(3.6×10^{12})**	1.86×10^{12}	**3.21×10^{12}**
	No. of Pions	6.83×10^{8} **(1.95×10^{8})**	10^{8}	**1.74×10^{8}**
	No. of Breakdowns	1*	0	0
NMOS	Gate area [μm^2]	500	500	500
	Fluence [cm^{-2}]	1.26×10^{13} **(6×10^{10})**	**1.86×10^{12}**	3.21×10^{12}
	No. of Pions	6.3×10^{7} **(3×10^{5})**	**9.3×10^{6}**	1.61×10^{7}
	No. of Breakdowns	1+	1+	1*
NFET	Gate area [μm^2]	432	432	432
	Fluence [cm^{-2}]	1.26×10^{13}	1.86×10^{12}	3.21×10^{12}
	No. of Pions	5.44×10^{7}	8.04×10^{6}	1.39×10^{7}
	No. of Breakdowns	0	0	0

* *Transistors measured on 01/02/2001, following PSI beam test. Most likely damaged outside pion beam, during handling.*

\+ *The gates were broken with a high oxide field sweep at PSI.*

The SEGR tests on discrete transistors provide initial statistical evidence that the postulated gate rupture mechanism is not applicable in the context of the amorphous SiO_2, with 3.79×10^8 pions incident on biased transistor gates where 10^6 pions would be expected to cause a breakdown.

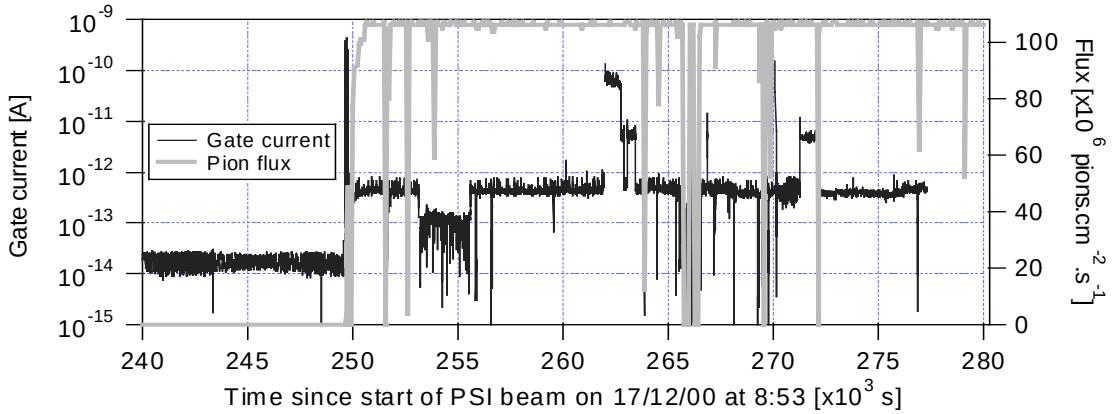


Figure 5.9: Chip10, PMOS transistor current vs. Time for a 2 V gate bias. The pion beam is switched on at 250×10^3 s on the time scale shown here.

The transistor tests enable measurements of the currents flowing through the gate during irradiation. Fig. 5.9 shows the gate current as a function of time for a PMOS transistor

exposed to pions. The pion beam is switched on around 250×10^3 s and it can be seen that the gate current beyond this point is higher. At no point does it exceed a few $\times 10^{-10}$ A, four orders of magnitude lower than the breakdown threshold.

The increase in current is most likely due to ionisation in the oxide, substrate, and source and drain implants. A silicon detector was placed in proximity of the devices being irradiated at PSI and a dose rate of ~ 2.6 rad/s was deduced from its current.

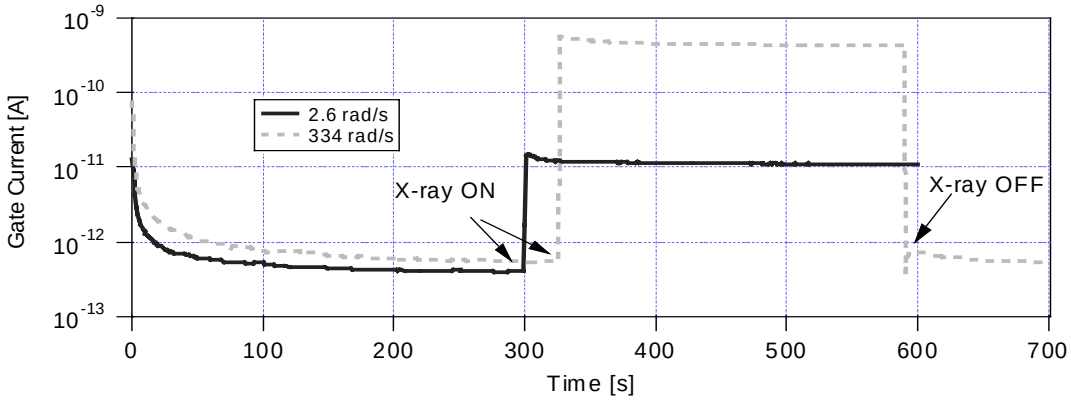


Figure 5.10: PMOS transistor current vs. Time for a 2 V gate bias. The 10 keV X-ray beam is switched on around 300 s.

Fig. 5.10 shows how the gate current varies under 10 keV X-ray irradiation. The gate current increases when the transistor is exposed to X-rays as expected.

Discrete transistors from the 0.25 μm CMOS process have also been exposed to heavy ions [22]. PMOS transistors with W/L = 2000/0.36 μm were exposed to 277 MeV iodine ions with an LET of 58.8 MeV.cm^2.mg^{-1} (compared with a CMS maximum LET of 15 MeV.cm^2.mg^{-1}) in steps up to a dose of 300 Mrad(Si) and to 134 MeV silicon ions with an LET of 9.27 MeV.cm^2.mg^{-1} up to a dose of 500 Mrad(Si). The transistors were not characterised during irradiation but within 20 minutes of the end of each exposure. They were biased with a low negative voltage applied to the gate and drain contacts ($V_{GS} = V_{DS} = -0.6$ V) with the source and backside terminals grounded ($V_{BS} = 0$). An excess leakage current through the gate was detected for $|V_G| > 1.6$ V after I exposure and for $|V_G| > 3.4$ V after Si exposure. These measurements provide more evidence that the 0.25 μm process should be free from breakdowns associated with its oxide.

5.2.3 SEGR in the APV25

5.2.3.1 SEGR with Pions

Pions with a momentum below 1 GeV/c are the dominant source of radiation in the inner part of the CMS detector, with the most damaging type believed to be 300 MeV/c pions due to their high nuclear interaction cross-section. The pion fluence at CMS at a radius of 22 cm, the inner barrel layer, over 10 years of operation is 10^{14} cm^{-2}.

From Section 5.2.1, $10^{6\pm1}$ pions are needed to observe a breakdown in a transistor. The APV25 has an active area of 7 mm × 6 mm = 4.2×10^7 μm^2 covered by approximately 200 000 transistors, each with an average area of ~ 200 μm^2. Assuming the average transistor gate oxide covers 10 % of its area, the fluence needed to observe a breakdown in one transistor is 10^6 pions/20×10^{-8} cm^2 = 5×10^{12} cm^{-2}. This corresponds to 5×10^{12} cm^{-2}/200 000 = $2.5 \times 10^{7\pm1}$ pions.cm^{-2} to observe a breakdown.

At PSI, the average flux delivered to the eight APV25 chips was 10^9 cm^{-2}s^{-1}. The eight APV25 chips provide much better statistics than the pion tests on discrete transistors since they were exposed to an average flux that was an order of magnitude higher over longer periods. A total fluence of almost 2×10^{14} cm^{-2} was reached in several runs, exceeding the CMS lifetime pion fluence. A failure in any one of the 1.6 million transistors would have been visible. The supply current measurements of the chips did not reveal any irregularity during the whole irradiation period, indicating that there was no SEGR-like damage in any of the chips.

5.2.3.2 SEGR with Heavy Ions

The tests designed to assess SEU susceptibility by exposing four APV25 chips to heavy ions (described in Section 5.1.2) would have been very sensitive to a broken transistor.

Although heavy ions do not stop in the region of interest very often, they must generate knock-on atoms at all points along their path and some of the knock-on atoms must be in the few × 10 keV range adequate to produce the type of damaging clusters postulated in Section 5.2.1. The kinetic energies of each ion are ≈ 100 MeV. It has been calculated that a 100 MeV silicon ion generates about 3×10^{-6} clusters/nm of path traversed, with a typical cluster size of about 40 nm[10]. The probability of a cluster overlapping the oxide is ~ 2×10^{-4} per incident ion, which is considerably higher than for neutrons, corresponding to ~ 4×10^3 ions/oxide puncture.

The pipeline logic provides the best statistical test of the damage cluster effect. It consists of 16 896 transistors, with a combined gate area of 5×10^{-3} cm^2. The number of

[10] Mika Huhtinen (CERN, Geneva, Switzerland) performed the simulations of cluster rates.

ions required for an oxide puncture in one transistor is 4×10^3 ions $\times$ 16 896 transistors/(5×10^{-3} cm^2) = $\sim 1.4 \times 10^{10}$ ions.cm^{-2}/transistor. This corresponds to a fluence of $\sim 8 \times 10^5$ ions.cm^{-2} for the observation of a transistor failure in the whole pipeline logic.

From the exposure to silicon ions (Table 5.3, Section 5.1.2), about 2 000 gate ruptures would be expected, where a single one would be detected. Without scaling for the atomic number of each ion used in the tests, a total of 9 500 ruptures would have been expected from the chip whose pipeline logic was exposed to heavy ions. It would seem more reasonable to scale the knock-on rate of ions other than silicon with atomic number, in which case far more ruptures would be expected.

No SEGRs were observed in any of the chips exposed to heavy ions. The uncertainties in the calculations are large but the heavy ion environment offers about a factor of $\times$ 400 sensitivity to damage clusters compared to pions.

5.3 Summary

The heavy ion beam test results suggest a value of 0.15 % of chips affected by SEU per hour. Experimental measurements of the APV25 cross-section in a 300 MeV/c pion beam yield a value for the upset rate that is up to 3 times higher than that from the heavy ion beam tests. This is to be expected since the 300 MeV/c pion beam represents a 'worst-case' environment with a considerable safety margin. SEU should not pose a problem for the APV25 at CMS provided that a periodic reset is applied to the APV25 chips with an interval of the order of minutes.

No SEGRs have been observed in any of the tests conducted with pions and heavy ions on discrete transistors and APV25 chips. There is therefore no evidence to suggest that the breakdown mechanism postulated in Section 5.2.1, based on cluster formation in crystalline silicon, is a threat to the normal operation of the amorphous gate oxide. The highest LETs expected in the Tracker should rarely exceed 15 MeV.cm^2.mg^{-1}. This, combined with the relatively low electric field across APV25 oxides (< 5 MV/cm), makes it very unlikely that SEGR will pose a problem for CMS electronics.

The results reported here indicate that the 0.25 μm process, with the implementation of suitable design rules, is capable of surviving the harsh CMS radiation environment.

Chapter 6
Low Temperature Operation of the APV25

The APV25 will be operated in a cooled environment at CMS because of the requirements imposed by the operation of the silicon detectors. These suffer two main effects under irradiation. First, reverse annealing leads to an increase in depletion voltage. Second, the radiation-induced leakage current produces a significant amount of heat which increases exponentially with temperature. The amount of power that can be removed by the cooling system increases only linearly with temperature. If the power dissipated by the silicon detector increases faster than the power removed by the cooling system, 'thermal runaway' occurs, eventually leading to a loss of control over temperature and leakage current. The risk of thermal runaway imposes the strongest limits on the cooling performance of the detector modules. With a safety factor of two on the power dissipation in silicon, the cooling fluid flowing through the module needs to be –20 ^{o}C in order to guarantee safe operation [2]. The silicon is then around –10 ^{o}C and exceeds 0 ^{o}C only during maintenance.

Detailed investigations of the APV25 are usually made at room temperature. The readout chip has been used in beam tests at PSI and CERN in –10 ^{o}C environments but usually with the aim of testing the silicon detectors, prototype readout chains or radiation effects such as SEU. The 'low temperature' studies were carried out specifically to assess the operation of the APV25 down to –30 ^{o}C.

6.1 Measurement Setup

The easiest way to control the temperature of transistors is to place them in a stable environment. For this reason, instead of using Peltier devices for example, an environmental chamber[11] was acquired. It was chosen to have a temperature range of between –40 ^{o}C and 130 ^{o}C and can be used for annealing devices at 100 ^{o}C, as described in Chapter 4, as well as studying how device parameters change with temperature. The chamber consists of heating and cooling systems and can be set to reach any temperature in the range described above to within 0.1 ^{o}C.

The test setup for measuring static parameters for the individual transistors was essentially the same as that described in Section 4.2.2.2, with a slight increase in the

[11] Model BS125-40, Design Environmental Limited, 32 Rassau Industrial Estate, Ebbw Vale, Gwent, NP3 5SD, UK.

length of cables connecting the transistors in the environmental chamber to the equipment located outside the chamber. The noise measurements for individual transistors reported in Chapter 4 were carried out in a Faraday cage because of the sensitivity of the measuring equipment to electrical interference. It was not possible to repeat these noise measurements in the environmental chamber.

The APV25 test setup for low temperature studies was intentionally built to be similar to that used in QA measurements of diced chips described in Section 4.3.2.3, providing a backup in case the latter failed. Electrical interference from the environmental chamber disrupted the testing sequence, affecting I^2C transactions and the Programmable Edge Generator (PEG). I^2C transactions are frequently required during the automatic pulse shape finder routine and mapping of the internal calibrate pulse. The PEG is used to provide the trigger for the external pulse generator. With the exception of the APV25 noise measurements, all other aspects of chip testing were affected by the electrical interference. This interference was found to coincide with the switching of the cooling mechanism, consisting of a compressor with a high start torque. Snubbers were fitted to the three solenoids associated with the cooling unit in an effort to try and reduce the electrical interference, with little effect. The chamber has a programmable interface which was used to control the cooling cycle, thus enabling measurements of the APV25 during time windows free of electrical interference.

To control humidity, the chamber has a built-in nitrogen purge system, which requires the connection of an external nitrogen source. The system has an interlock to ensure that no further nitrogen flows into the chamber when a user opens the chamber door. A micro-switch connected to the chamber door was found to be defective upon delivery of the chamber. This problem was addressed but all measurements taken below 0 ^oC reported here were carried out without nitrogen. In all cases, only a small amount of condensation was observed, usually on the stainless steel chamber walls.

One of the main difficulties came from determining the actual temperature of the APV25 in the chamber. Initially, a resistive type device (RTD) was placed on the PCB on which the APV25 was glued. This method showed a chip temperature that was ~ 8 ^oC higher than that of the chamber. The RTD was then glued directly onto the surface of the chip, which was found to be ~ 18 ^oC higher than the chamber temperature. This only provides a lower limit for the true junction temperature of MOS devices which is of interest when predicting noise behaviour.

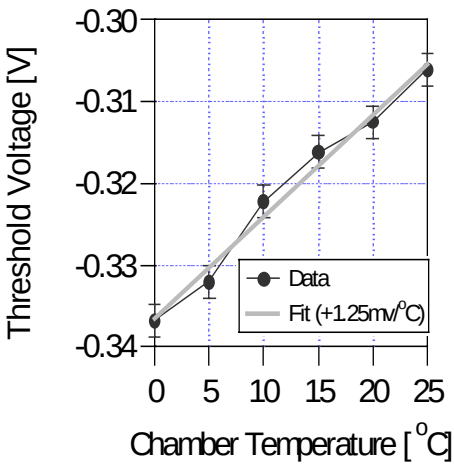
6.2 Transistor Results

The dependence of static parameters such as threshold voltage and transconductance on temperature was studied for two main reasons:

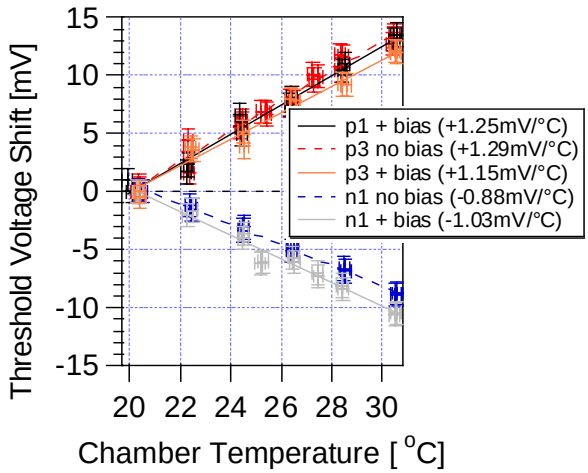
- The continuous monitoring of threshold voltage during irradiation (Section 4.2) required some calibration to take into account the temperature fluctuations within the X-ray cabinet,
- Determining the '*X*' term of eq. (2.25) which represents the relative contributions of lattice and impurity scattering and can only be extracted experimentally.

6.2.1 Threshold Voltage

The threshold voltage was calculated using the method described in Section 4.2.3, at different temperatures in the range 0 → 35 °C. The change in threshold voltage as a function of temperature is seen to be around +1.25 mV/°C for PMOS transistors and –1 mV/°C for NMOS transistors, Fig 6.1.



(a) PMOS over a 25 °C range.



(b) PMOS and NMOS over a ~10 °C range, taken from [31].

Figure 6.1: (a) PMOS threshold voltage and (b) PMOS and NMOS threshold voltage shift.

Fig. 6.2 shows the threshold voltage shift in an NMOS transistor as predicted by theory (Section 2.1) for different values of N_A. To calculate the threshold voltage in Fig. 6.2, values of n_i were taken from a graph with a logarithmic scale leading to large errors [11]. The results point to a value of N_A in excess of 10^{16} cm^{-3} for the 0.25 µm process since the slope in Fig. 6.2 decreases with increasing N_A with a minimum slope of –1.89 mV/°C (c.f. –1 mV/°C in Fig. 6.1 (b)).

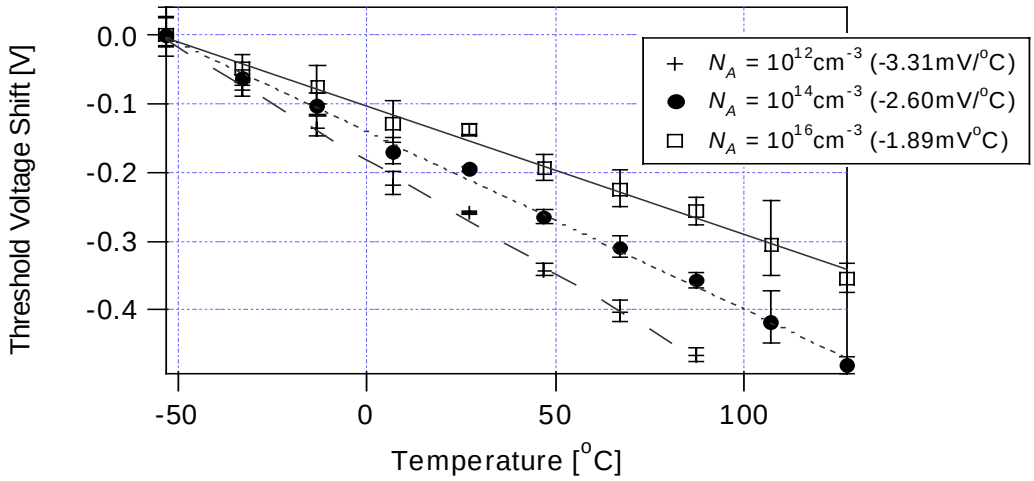


Figure 6.2: NMOS threshold voltage shifts as a function of temperature as predicted by theory for different values of the drain and source doping concentrations.

6.2.2 Transconductance and Mobility

The temperature dependence of transconductance is given by the following expression:

$$g_m(T) = g_m(T_0)\left(\frac{T}{T_0}\right)^X \qquad \text{…eq. (6.1).}$$

where $g_m(T_0)$ is the transconductance at a reference temperature T_0 and X is a factor which takes into account the compensating contributions of lattice and impurity scattering. As mentioned in Section 2.3.2, X is usually quoted to be $X = -1.5$ which effectively assumes lattice scattering is the major component and impurity scattering is negligible. This is true at high temperatures where impurity scattering is less significant.

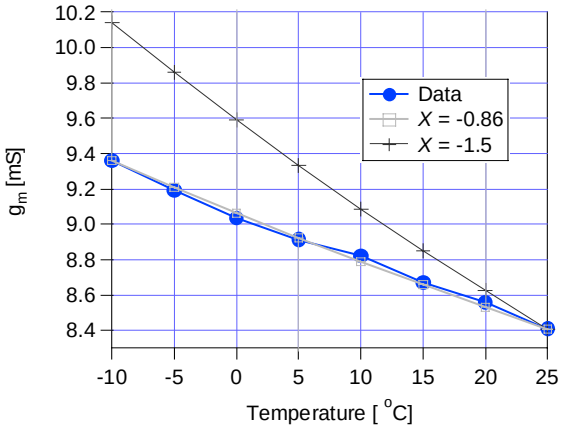


Figure 6.3: Temperature dependence of transconductance in a PMOS transistor. The data were collected for I_D = 400 μA.

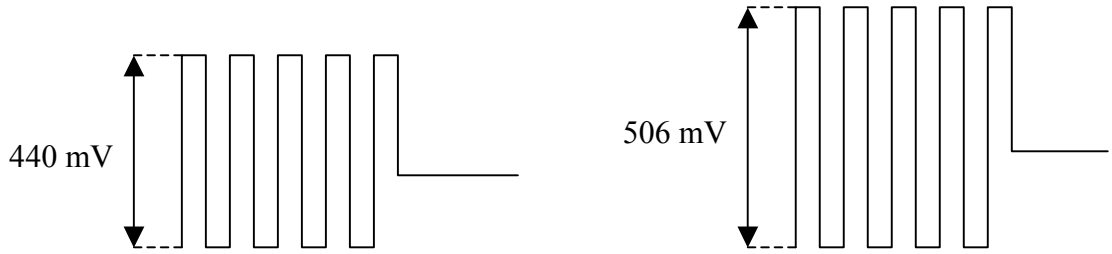
$X = -0.86$ is a good match to the data as can be seen from Fig. 6.3, indicating that the contribution from impurity scattering cannot be neglected. Because the value of X is

derived from a transistor similar to the preamplifier input PMOS in the APV25, it can be used to predict how noise in the APV25 should vary with temperature.

6.3 APV25 Results

6.3.1 Chip Output

The chip was biased using a constant external reference source. The amplitude of the chip output was found to increase as it was cooled, Fig. 6.4.



(a) 43 °C. *(b) –11 °C.*

Figure 6.4: Chip output at two different temperatures, (a) 43 °C, (b) –11 °C.

The increase in output is around 15 % over the 54 °C drop in temperature. The chip output is a combination of internal currents, which are sensitive to threshold voltage shifts due to temperature. For example, in an NMOS transistor, V_{th} is typically around 450 mV at 25 °C. It would therefore increase by 12.5 % at 1 mV/ °C over the 54 °C range (from 43 °C to –11 °C). Such a shift could account for some of the observed increase in chip output. However, there is a conflicting argument. The chip reference current is generated from an external voltage applied across an external resistor. The resulting current is then fed into an NMOS device in the APV25. As the temperature decreases, the current through the NMOS transistor should decrease, leading to a reduced reference current. In addition, there is a decrease in internal resistances by up to 0.15 % per °C depending on the type of resistance.

The change in chip output is not in itself a problem but must be taken into account when the output is fed into the ADC to ensure the full range can be digitised for all temperatures. This condition can be met by tuning the APV25 output before it reaches the ADC input, using an additional gain stage. Another consequence of the fluctuation in the chip output is that the APV25 noise as it appears in digitised form is relative. For comparison, the noise has to be quoted in terms of absolute value by referring it to an external pulse of known magnitude for each temperature.

6.3.2 Current Consumption

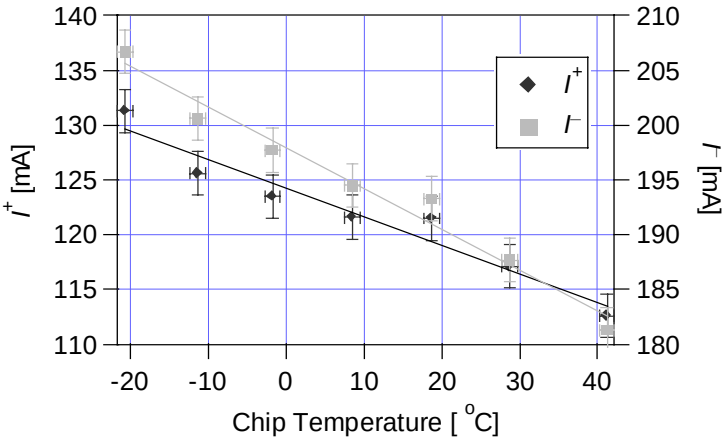


Figure 6.5: Power supply currents.

If the bias generator settings are left unchanged, the power supply currents, I^+ and I^-, increase as the temperature decreases, Fig. 6.5. This result is expected since all internal chip currents are higher as a consequence of the drop in temperature. It is consistent with the observed increase of 15 % in Section 6.3.1. By adjusting the bias generator settings, the power consumption can be controlled, allowing the same values at –20 °C as those at 40 °C.

6.3.3 Pedestals

The baseline was found to increase with decreasing temperature in both peak and deconvolution modes.

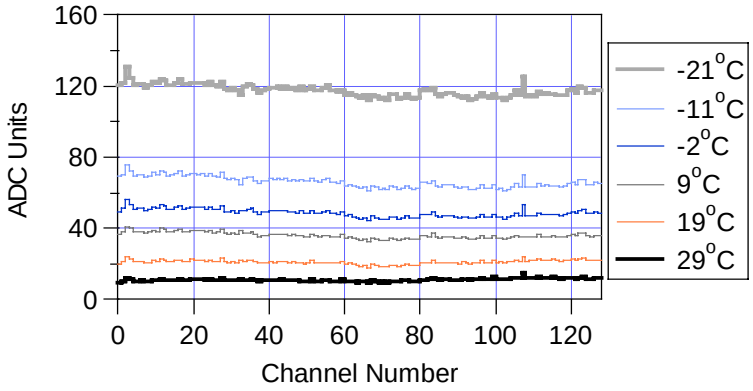


Figure 6.6: Peak mode pedestals. The pedestals at 41 °C are subtracted from all other pedestals.

Fig. 6.6 shows the peak mode pedestals. The baseline level can be adjusted using VPSP. At 43 °C, VPSP was set to 28 whereas at –11 °C, VPSP was set to 30. A drop of 2 in the value of VPSP over a 54 °C range corresponds to a shift of 15 mV since the resolution of the VPSP bias generator is 7.5 mV. The small shift in the baseline levels with temperature illustrates the stability of the pedestals. Although continuous monitoring of the temperature will be required, once a value for VPSP is chosen, it should not be

changed on account of the small temperature fluctuations in the Tracker environment. The change in VPSP due to radiation is larger, ~ 7 bits, although this occurs over a much longer time period.

6.3.4 Pulse Shape

6.3.4.1 External Pulse Shape

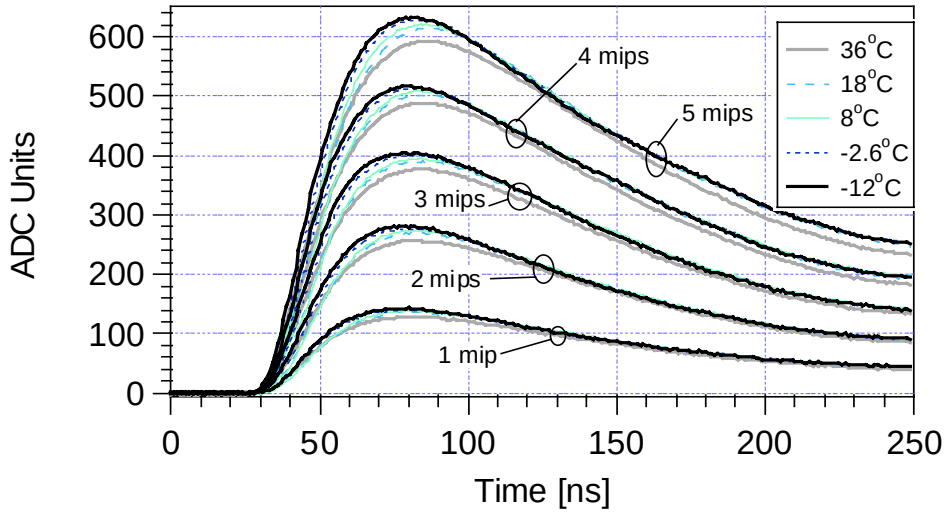


Figure 6.7: External pulse shapes from 1 to 5 MIP in Peak mode for various temperatures.

The two bias registers that determine the shape of the pulse are ISHA and VFS. ISHA governs the rise time whilst VFS determines the shape of the tail of the pulse. Fig. 6.7 shows external pulse shapes for a range of temperatures over which ISHA and VFS were kept constant. It can clearly be seen that as the temperature decreases, the gain increases and the rise time decreases.

The pulse shape can be recovered by changing VFS and ISHA to obtain the same rise time and tail, Fig. 6.8. In this particular case, at 43 ^{o}C ISHA = 20 and VFS = 50, and at –11 ^{o}C ISHA = 17 and VFS = 55.

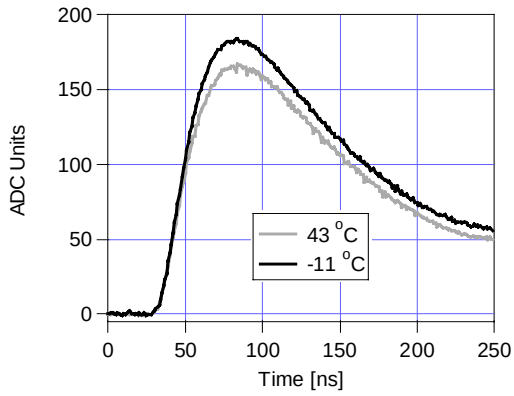
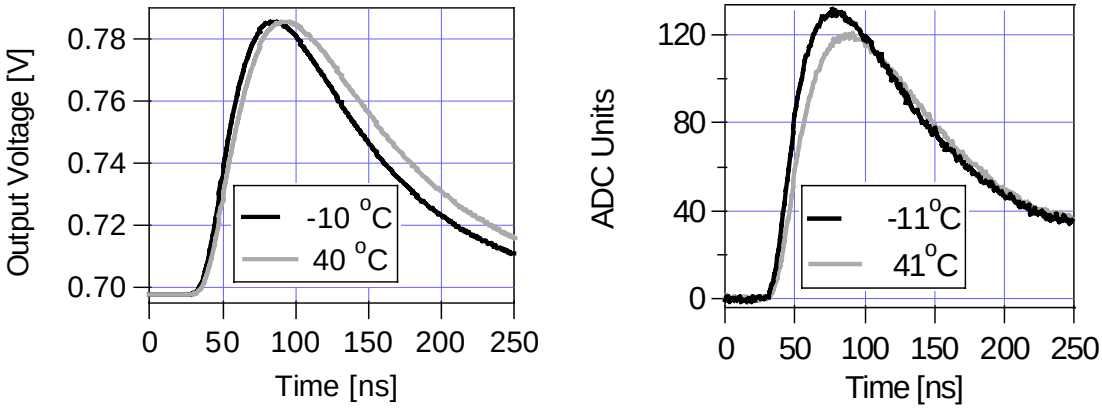


Figure 6.8: 2 MIP external pulse, tuned for the same rise time at –11 ^{o}C and 43 ^{o}C.

6.3.4.2 Comparison with Simulations

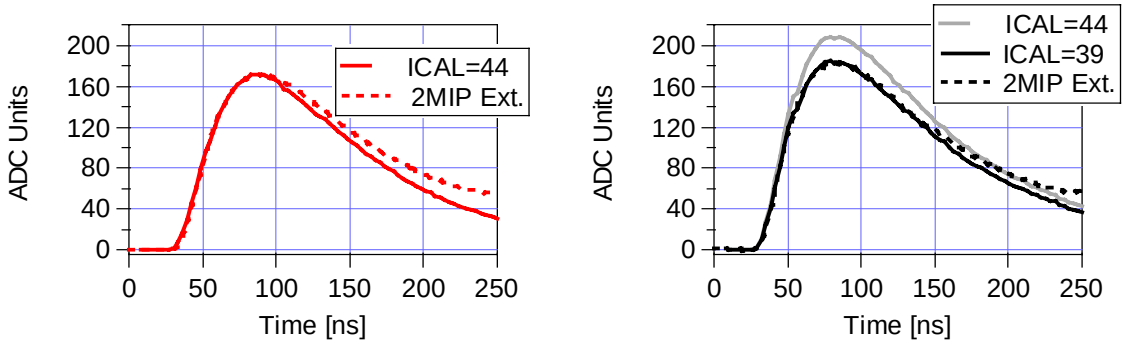
Simulations of the preamplifier and shaper output were carried out in HSPICE to compare with the chip output. The simulations show a decrease in rise time but no increase in gain, Fig. 6.9. This should be expected because the input current for the preamplifier and shaper was not changed. The real chip will see an increase in the input current for its preamplifier and shaper at the lower temperatures, leading to an increase in gain. According to the simulations, the rise time decreases by 8 ± 1 ns for a 50 °C drop in temperature. The error comes from the fact that there is a 3 ns plateau for the maximum output voltage of the 40 °C pulse. The rise time difference for the chip is observed to be 9 ± 1 ns for a 52 °C drop in temperature, which is in good agreement with the simulations.



(a) Preamp and shaper simulation. *(b) Chip output.*

Figure 6.9: Comparison between simulation and real chip output for a 1 MIP input.

6.3.4.3 Calibrate Pulse



(a) T = 44 °C. *(b) T = –9 °C.*

Figure 6.10: Internal calibrate pulse.

At a temperature of 44 °C, the bias register setting for the internal calibrate circuit which corresponds roughly to 2 MIP is ICAL = 44. Fig. 6.10 (a) shows the response to an

internal calibrate pulse (solid line) and the response to a 2 MIP equivalent external pulse (broken line) at 44 ^{o}C. Fig. 6.10 (b) shows the response to a 2 MIP external pulse at –9 ^{o}C. The internal calibrate setting that best matches the external pulse at –9 ^{o}C is no longer ICAL = 44 but ICAL = 39. The increase in chip currents affects the internal calibrate circuit, which has implications for its use at different temperatures. For example, the APV25 manual states that for a 1 MIP signal, ICAL = 25 at room temperature. This would no longer be true at –10 ^{o}C.

6.3.5 Noise

The dependence of noise on temperature is given by eq. (2.27), which yields the following expression:

$$S_V(T) = S_V(T_{nom})\sqrt{T^{1-X} \times T_{nom}^{X-1}} \qquad \text{…. eq. (6.2).}$$

where $S_v(T_{nom})$ is the rms noise level at a reference temperature T_{nom}, T and T_{nom} are in Kelvin, and $X = -0.86$, derived from Section 6.2.2.

The decrease in noise that can be expected for the temperature range over which measurements were conducted (57 ^{o}C to –13 ^{o}C, ΔT = 70 ^{o}C) is 19.9 %. This prediction relies on the assumption that the transistor junction temperature, $T_{junction}$, is approximately equal to the measured chip temperature, T_{chip}. It is also assumed that junction temperature decreases at the same rate as the measured chip temperature. In practice, $T_{junction}$ is almost certainly higher than T_{chip}, leading to a smaller decrease in noise over the same ΔT. For example, in the ADC (SPT7860) used to digitise the APV25 output, the junction temperature can reach 175 ^{o}C for operating temperatures up to 70 ^{o}C. In this case, for $\Delta T_{junction}$ = 70 ^{o}C, ΔS_V = 14.6 %. The junction temperature in APV25 transistors is probably not as high as that in the ADC but the uncertainty in its value introduces large errors in the prediction of the decrease in noise.

6.3.5.1 Digitisation Noise

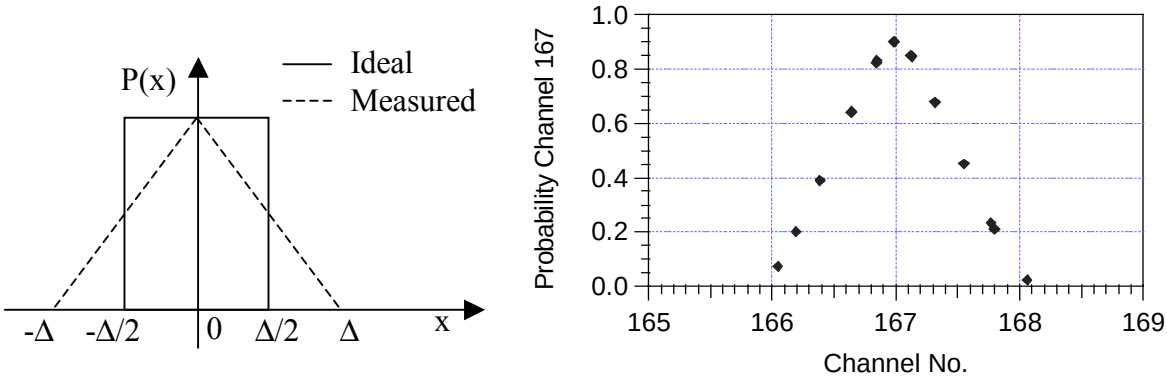
Digitisation noise has to be taken into account since the rms noise level from the APV25 is of the order of 1 ADC count. Ideally, the digitisation noise is given by:

$$\sigma_{ideal} = \frac{\Delta}{\sqrt{12}} = 0.29\Delta \qquad \text{….. eq. (6.3).}$$

where σ_{ideal} is the ideal digitisation noise and Δ is the ADC resolution (1 ADC unit).

In a real ADC, additional noise in the digitisation process affects its resolution. This effect was evaluated by feeding a voltage level from a standard power supply to the ADC, measuring the ADC output for a number of frames and then finely adjusting the

level of the voltage source to scan over three ADC channel numbers. The results are shown in Fig. 6.11 (b).



(a) Ideal vs. measured. *(b) Measured digitisation noise.*

Figure 6.11: Digitisation noise.

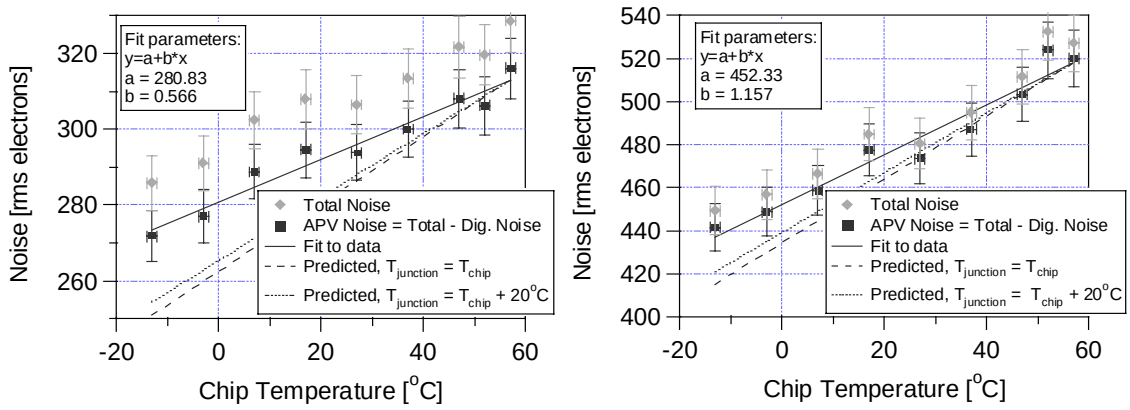
The digitisation noise corresponding to the shape of Fig 6.11 (b) is given by:

$$\sigma_{measured} = \frac{\Delta}{\sqrt{6}} = 0.41\Delta \qquad \ldots\ldots \text{ eq. (6.4).}$$

In reality, the power supply used in the measurement of the digitisation noise was not stable to the required precision. The interval corresponding to 1 ADC count is Δ = 2.7 mV. To obtain 10 points between 2 ADC channel numbers, a resolution of better than 0.3 mV is required from the power supply. The likely true digitisation noise is somewhere between the ideal value and the measured value: $\sigma_{ideal} \leq \sigma_{real} \leq \sigma_{measured}$. This has to be subtracted in quadrature from the total noise to obtain the APV25 noise. The technical data sheet for the 10-bit SPT7860 ADC quotes the effective number of bits as 8.5. Exactly how this might affect the digitisation noise has not been determined.

6.3.5.2 Noise with Low Gain

When noise measurements were first carried out in the environmental chamber, the digitisation sequence was in the 'low gain' configuration. The ADC input range is $0 \rightarrow 2$ V. From the test card on which it is mounted, the APV25 output is ~ 500 mV. It was further amplified $\times$ 4 to cover the full ADC range. With this setup, the noise in peak mode (deconvolution mode) is ~ 1 (1.7) ADC unit. Digitisation noise is therefore very significant. The data reported in this section were recorded over several runs.



(a) Peak mode. *(b) Deconvolution mode.*

Figure 6.12: APV25 noise results obtained with the low gain setup.

Fig. 6.12 shows the APV25 noise, which is calculated by subtracting the digitisation noise from the total noise. Each point is an average of up to 48 channels. A fit to the APV25 noise is also shown, along with the predicted behaviour.

To convert noise to rms electrons from ADC units, the following expression is used:

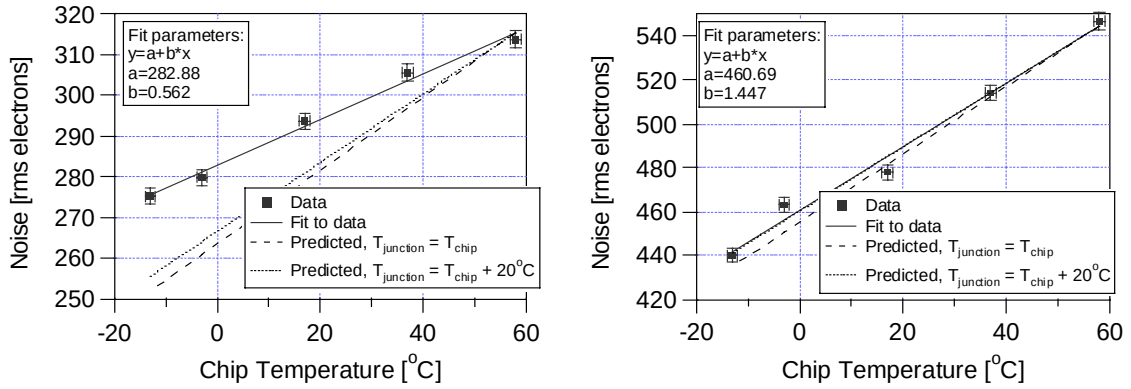
$$\Delta = \frac{1mip}{A_{\max}} = \frac{25000e}{A_{\max}} \qquad \text{..... eq. (6.5).}$$

where Δ is in rms electrons and represents 1 ADC unit and A_{max} is the maximum amplitude of the output pulse obtained when a 1 MIP external pulse is injected into the APV25. An error of ± 2 ADC units was taken to represent the uncertainty in determining A_{max}, which is measured to be ~ 80 ADC units for a 1 MIP signal. This corresponds to an error of ± 2.5 % on the noise when it is expressed in rms electrons. The error on the chip temperature is ± 1 ^{o}C, which takes into account fluctuations during the measurement of the APV25 output pulse. In practice, the higher the chip temperature, the more stable it is.

The predicted decrease in noise is 19.9 % for a temperature drop of 57 ^{o}C to –13 ^{o}C. The actual decrease is 12.7 % in peak mode and 15.6 % in deconvolution mode. For chamber temperatures below ~ 10 ^{o}C corresponding to chip temperatures below ~ 28 ^{o}C, the electrical interference from the chamber cooling unit begins to affect measurements, especially those of the gain (A_{max}) which are required to convert the relative noise in ADC units to absolute noise in rms electrons. It can be seen from Fig. 6.12 (b) that the data follow closely the predicted behaviour down to around 25 ^{o}C. Below 25 ^{o}C, the measured noise is noticeably higher than that predicted.

6.3.5.3 Noise with High Gain

In the 'high gain' configuration, the APV25 output is amplified by a factor of ~17 before it is fed into the ADC. This effectively zooms into the analogue signal at the expense of the APV25 digital header, which can no longer be digitised over the full range. The advantage is that digitisation noise is much less significant, with the noise in peak mode corresponding to ~ 3.5 ADC units (c.f. 1 ADC unit in 'low gain' configuration), whilst it is 6 ADC units in deconvolution mode.



(a) Peak mode. *(b) Deconvolution mode.*

Figure 6.13: APV25 noise results obtained with the high gain setup.

Fig. 6.13 shows the results obtained with the high gain configuration. In peak mode, a 12.5 % decrease in noise is measured over the 57 °C to –13 °C range. The deconvolution mode data show an 18.6 % decrease over the same temperature range. The error in the noise measurement is lower in high gain mode due to the higher A_{max}, A_{max} ~ 270 ± 2 ADC units corresponding to ± 0.7 % in noise when it is expressed in rms electrons.

The 'low gain' and 'high gain' results are broadly similar, with the peak mode data in particular showing very little difference between the two configurations. The data closest to the predicted behaviour were obtained in deconvolution mode with the 'high gain' setup. These data can be considered to be the most reliable data because the magnitude of the signal after digitisation is the highest (~ 6 ADC units) and is least affected by digitisation noise. Regardless of the configuration used, deconvolution mode data match predictions better than peak mode data. There are no obvious reasons for this other than that peak mode noise is smaller in magnitude than deconvolution mode noise by a factor of ~ 1.7 and is therefore more affected by digitisation noise, especially at low temperatures.

6.4 Radiation Damage at Low Temperatures

The X-ray cabinet was held at roughly the same temperature throughout the characterisation of ionising radiation-induced damage on APV25 chips. For this reason, this section does not present results on the temperature dependence of radiation damage. Instead, it brings together the current knowledge on how chip parameters change with ionising radiation and with temperature in an attempt to predict its behaviour in the operational environment at CMS.

To compare the results from radiation studies with those from low temperature studies, it is necessary to establish whether the former would have been temperature dependent. Previous workers have suggested that within the –55 ^{o}C to 125 ^{o}C range, there is no major dependence of the buildup and annealing of radiation-induced charge on temperature [25]. Although annealing of oxide trapped charge through tunnelling and formation of interface traps occur over a longer period of time as temperatures decrease, the final magnitude of both effects remains unchanged.

The difference in temperature between the radiation damage studies and the CMS environment is relatively small (ΔT = 35 ^{o}C). The processes of oxide trapped charge annealing and interface trap buildup occur with a probability, p, that can be described by the following expression:

$$p \propto e^{-E/kT} \qquad \text{……. eq. (6.6).}$$

where E is the activation energy, k is the Boltzmann constant and T is the absolute temperature. If the chip temperature is taken to be 18 ^{o}C higher than its environment, the rate at which oxide trapped charge anneals is reduced by a factor of ~ 6 at –10 ^{o}C compared to 25 ^{o}C (the activation energy for this process is ~ 0.4 eV) and that of interface trap buildup is reduced by a factor of ~ 39 (the activation energy is ~ 0.8 eV). These reductions are negligible compared to the time scales over which the two processes occur at CMS since the dose rate will be relatively low, allowing the tunnel-annealing of oxide trapped charge and the formation of interface traps during irradiation. This essentially means that the results obtained from the radiation damage studies at room temperature do not have to be corrected to relate them to the –10 ^{o}C environment.

Table 6.1: Changes in chip parameters in peak mode.

The low temperature and radiation effects columns show actual results, the CMS column shows predicted changes. The full range for the bias registers (VPSP, ISHA and VFS) is 0 to 255.

		Low temperature studies: $n(-10^oC)-n(25^oC)$	Radiation effects studies: n(anneal)–n(prerad)	CMS
Bias Registers	VPSP	2	7	9
	ISHA	–2	1	–1
	VFS	4	–13	–9
Noise	ΔS_V	–6.5 %	–0.5%	–7 %

Table 6.1 shows the predicted changes in some chip parameters in the CMS environment after 10 Mrad derived from the low temperature and radiation effects studies. The changes in bias register settings are not significant since the range available for each setting is 0 to 255. Because the chip will be operated at –10 ^oC and because no appreciable degradation due to radiation occurs, its noise performance should actually improve when compared with that at room temperature.

The APV25 has been successfully operated at –10 ^oC in a highly ionising radiation environment during a beam test at the PSI.

6.5 Summary

Although the response of the chip changes over a wide range of temperatures, continuous tuning of the bias registers is not necessary in an environment where the temperature fluctuations are small, once a set of bias register values has been chosen for operation in the given environment. In the CMS Tracker, a detector control unit (DCU) ASIC will monitor the temperature on each detector module, allowing for the fine-tuning of the readout system should it be required.

With the change in bias register settings with temperature easily accommodated in the actual range available for each register in the chip, the most significant change with temperature comes from the reduction in noise.

One additional feature of the APV25 version S1 compared to the previous S0 version is that it can generate an internal reference current. The low temperature studies which have so far only been conducted with an external reference current could be extended to look into the behaviour of the chip with its internal reference current enabled.

The combined effects of operating the chip at –10 ^oC in the CMS radiation environment should be similar to those determined from observations made in the separate studies of radiation damage and low temperature operation.

Conclusions

For the first time in a particle physics experiment, a commercial 0.25 μm CMOS technology will be used to manufacture complex electronic components that will be deployed on a very large scale in a hostile radiation environment and operated to the demanding requirements of high speed, low power and low noise. Access to the CMS detector for maintenance purposes will be very limited, placing further demands on reliability. This is the motivation behind the large programme of evaluation necessary to provide the users with the confidence that all components will remain fully functional throughout the 10-year lifetime of the experiment.

The two major types of radiation damage that affect CMOS devices are total dose ionising radiation effects and single event effects. Different approaches are taken to establish the importance of these radiation damage mechanisms. For example, a closer examination of total dose effects is better served from a study of discrete test transistors whereas some single event effects only apply to complex integrated circuits using specific combinations of transistors.

Several discrete transistors have been irradiated to total dose levels far exceeding those that will be reached at CMS. The results from these tests demonstrate exceptional total dose radiation tolerance, attributed to the thin gate oxide that allows tunnelling of electrons to neutralise the radiation-generated positive oxide charge. In addition, the 'enclosed' layout of the NMOS transistors minimises the leakage current that might otherwise limit their use. With the experience gained from the transistor measurements, a total dose testing procedure has been set up for the APV25. In total, 23 chips have been irradiated, with significant changes in operational characteristics observed. The radiation testing procedure will be part of a quality assurance programme, monitoring a subset of the 75 000 APV25 chips that will instrument the CMS Tracker. The plan is to irradiate one chip per wafer (~360 chips) initially, and as confidence builds up, an even smaller sample, probably one chip/wafer for 6 wafers from every production lot of 25 wafers.

SEU tests have been carried out at heavy ion and pion beam facilities. The results match a predictive model derived from simulations of charge collection in MOS transistors and simulations of upset critical charge in memory cells. An estimate of the SEU rate at CMS has been calculated. The estimated rate of 0.15 % upset chips per hour will not be

a problem provided that a reset is applied to the APV25s to refresh digital logic blocks. This relatively low upset rate is partly due to the high LET threshold of the APV25, a consequence of its special design features.

The SEU tests provide the right conditions to measure sensitivity to SEGR. No SEGR have been observed, as expected from evidence that the thinner the gate oxide the more robust it is. Process features such as shallow trench isolation and the application of special design rules help to reduce the sensitivity of the APV25 to SEL, ensuring that no such effects should pose a threat to CMS.

The APV25 will be operated at –10 ^{o}C but most bench tests are still being carried out at room temperature. Studies of the APV25 and discrete transistors have been carried out to assess how their parameters vary with temperature. The most significant conclusion from these studies is that noise decreases with decreasing temperature. Although the observed drop in noise is less than expected, it is nevertheless a beneficial consequence of operation at –10 ^{o}C. Further work will be needed to investigate the discrepancy between expected and observed noise levels and to confirm all measurements on the APV25 when it is operated with its internal reference current, which is the CMS operational mode.

Total dose radiation and low temperature operation will induce shifts in the internal voltage levels of the APV25 chip but these are easily accommodated by the large range of the fully programmable bias generator settings.

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