Thermoelectric Performance of $Si_{0.8}Ge_{0.2}$ Nanowire Arrays

Bin Xu, Chuanbo Li, Kris Thielemans, Maxim Myronov, and Kristel Fobelets

***Abstract*—The output power of a thin-film thermoelectric generator consisting of a Cu–20-μm nanowire (NW) array (NWA)–Si bulk–Cu sandwich with Si or $Si_{0.8}Ge_{0.2}$ NWs is measured and compared to Cu–Si bulk–Cu for small temperature differences around room temperature. The array of NWs is made by metal-assisted chemical etching that retains the Ge concentration in the wires. The conversion of one surface of Si bulk into an array of short—relative to the remaining bulk—Si NWs improves the maximum output power by a factor of two. Using an array of Si NWs in combination with $Si_{0.8}Ge_{0.2}$ increases the maximum output power by a factor of 20. The increased output power, under the same heating power, is due to the lower thermal conductivity and contact resistance of the NWA and SiGe compared to Si bulk. A matrix model is developed to solve the coupled thermal transport equations for an arbitrary number of layers. Fits to the measurement allow the extraction of the electrical contact resistance and the effective internal temperature drop across the semiconductor composite.**

***Index Terms*—Nanowire (NW) arrays (NWAs), SiGe, thermoelectric.**

I. Introduction

THE TOPIC of thermoelectric power generation has seen a revival due to the introduction of nanomaterials. Widespread use of thermoelectricity has been hindered by low efficiencies which are due to the coupling between the thermal and electrical transport properties [1]. Replacing the bulk semiconductor by nanowires (NWs) can uncouple these [2]. Different research groups have investigated the thermoelectric properties of single NWs and confirm a strong reduction of the thermal conductivity in NWs with a diameter less than 100 nm, due to phonon confinement [3], [4]. Simultaneously, the electrical conductivity appears not to reduce at the same rate, resulting in an improved performance factor ZT. BiTe and its compounds are traditional thermoelectric materials for use around room temperature [5]. Silicon, which is popular in microelectronic systems, is not an appropriate thermoelectric material due to its high thermal conductivity but is readily available. Its poor thermoelectric character can however be manipulated by the conversion of a part of the Si bulk into an array of Si NWs. Phonon scattering at the NW boundaries and the increased air fraction reduce the thermal conductivity in the Si NW arrays (NWAs) [6]. Bulk SiGe has lower thermal conductivity than Si due to alloy scattering and is used at temperatures around 1000 °C [5]. In [7], it was shown that alloy scattering and interface effects in SiGe-containing NWs reduce the thermal conductivity to very low levels. Therefore, the combination of SiGe and NWAs promises improvements in the thermoelectric properties of Si-based composites.

Characterization of single NWs gives the physical properties in function of geometrical parameters. However, in order to exploit the improvements of the nanomaterial in thermoelectric systems, a more undemanding structure is needed. In this paper, we use arrays of vertically upstanding Si- and/or SiGe-containing NWs attached to a Si substrate in a thermoelectric generator (TEG). The thermoelectric performance of Si NWAs was investigated in [6], [8], and [9]. Chen *et al.* [6] use metal-assisted chemical etching (MACE) NWAs and show the thermal conductivity reduction of Si NWAs as a function of length. A reduction of ∼14% was obtained for a 35-μm NWA. In [8] and [9], an ∼1.5-μm Si NWA was fabricated with a wire diameter of ∼80 nm using photolithography and consisted of 162 thermocouples. A maximum power of 1.4 nW was generated for an external temperature difference of 70 K and a total surface area of 25 mm^2. We investigate the influence of both Si and SiGe NWAs attached to bulk Si, fabricated via MACE. We measure the output power of the TEGs for small external temperature differences of maximum 6 K around room temperature as a function of load resistance. The measurements show that, even when the length of the NWAs and the thickness of the SiGe layer are small compared to the remaining bulk, the performance of the TEG is improved.

A novel matrix formalism was developed to solve the thermoelectric transport properties of the multilayered composite TEG. Discontinuities in voltage and temperature across the interfaces are taken into account via thin intermediate layers.

Simulations for the different TEGs, fitting the voltage, and temperature drops across the contact interfaces demonstrate that the increased output power is partly due to the lower thermal conductivity of the NWAs and SiGe.

This paper is organized as follows. In Section II, a matrix model is developed for a multilayered TEG. In Section III, the material preparation is explained, followed by the measurements and derivation of the internal temperature difference in Section IV.

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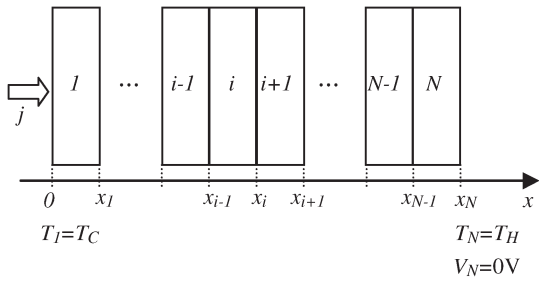

Fig. 1. Multilayered structure with N layers. Definition of the material structure and axis system used in the theoretical derivation and the boundary conditions on temperature and electrical potential.

II. Development of the Matrix Formalism

We assume that heat and current transport are 1-D. The set of coupled differential equations that govern the thermoelectric transport phenomena in each layer i of a multilayered TEG (see Fig. 1) is given by [10]

$$\begin{cases} j = -\sigma_i \frac{dV_i(x)}{dx} - \alpha_i \sigma_i \frac{dT_i(x)}{dx} \\ q_i(x) = j\, \alpha_i\, T_i(x) - \kappa_i \frac{dT_i(x)}{dx} \\ \frac{dj}{dx} = 0 \\ \frac{dq_i(x)}{dx} + j \frac{dV_i(x)}{dx} = 0 \end{cases} \tag{1}$$

where $i = 1, \ldots, N$ is the layer number, N is the total number of layers, j is the current density, V is the electrostatic potential, T is the temperature, q is the heat flux, σ is the electrical conductivity, κ is the thermal conductivity, and α is the Seebeck coefficient. Since the temperature range is small, the Thompson effect can be neglected. Under these assumptions, it is possible to describe the thermoelectric transport through a multilayered system in terms of a matrix formalism. This allows easy implementation in Matlab [11] and avoids the need for finite-element methods.

The solution of (1) in one layer i gives quadratic equations for $T_i(x)$, $q_i(x)$, and $V_i(x)$ in function of integration constants: C_{t_i}, D_{t_i}, and D_{v_i}. The integration constants can be found by imposing continuity at each interface x_i

$$\begin{aligned} T_{i+1}(x_i) - T_i(x_i) &= 0 \\ q_{i+1}(x_i) - q_i(x_i) &= 0 \\ V_{i+1}(x_i) - V_i(x_i) &= 0. \end{aligned} \tag{2}$$

Discontinuities in temperature and voltage, due to thermal and electrical interface resistances, are taken into account by introducing thin intermediate layers with appropriate material constants. In addition to (2), there are three boundary conditions

$$\begin{aligned} T_N(x_N) &= T_H \\ T_1(0) &= T_C \\ V_N(x_N) &= 0V. \end{aligned} \tag{3}$$

where T_H and T_C are the hot and cold temperatures, respectively. One of the nodal voltages (at x_N) is grounded, and the potential at $x = 0$, $V_1(0)$ follows from the calculations. The solution for all integration constants can be found by rewriting (2) and (3) in matrix form

$$A_{i+1}(x_i)\, Y_{i+1} - A_i(x_i)\, Y_i - R_{i+1,i} = 0 \tag{4}$$

where $A_l(x_k)$ is a $3 \times N$ by $3 \times N$ matrix, where $A_i(x_k) = 0$ for all $k \neq i$ and $i + 1$. The nonzero elements are a function of the material parameters in layers i, $i + 1$, and x_i. $R_{I+1,i}$ is a $3 \times N$ vector with material constants that result from (2) and (3), and Y_i is a vector with the $3 \times N$ integration constants. Equation (4) transforms problem (1) into simply solving a system of linear equations.

To calculate the output power P_{out} as a function of load resistance R_L for a given temperature difference $\Delta T = T_H - T_C$, we impose the condition

$$V_1(0) - V_N(x_N) = R_L j A \tag{5}$$

where A is the cross-sectional area. Since $V_1(0)$ is a function of the current j, (5) needs to be solved using a nonlinear equation solver to find the current for a given load.

The validity of this approach was checked against the results in [10] and calculations of P_{out} of a Si layer by splitting the Si in different Si partitions with the same total thickness.

With this matrix formalism, the influence of the thermal and electrical interface discontinuities on the output power of the TEG is studied. A five-layer structure, consisting of Cu–intermediate layer–Si bulk–intermediate layer–Cu, was simulated for different values of κ and σ ($\alpha = 0$) for the interface layers. The other layers have parameter values taken from literature. These simulations show that P_{out} of the thin TEG is mainly limited by the total electrical contact resistance R_c and the effective internal temperature drop ΔT_{int}. Fig. 2(a) and (b) shows the influence of the electrical and thermal interface discontinuities at the Cu–semiconductor junctions on P_{out} for 500-μm p-Si bulk, respectively. The external temperature drop is $\Delta T_{\text{ext}} = 3$ K. Fig. 2(a) shows the P_{out} as a function of R_L, for different values of R_c. R_c influences both maximum P_{out} as well as the total resistance of the TEG R_{TEG}. R_{TEG} can be extracted from the maximum power dissipated in the load resistance, where $R_{\text{TEG}} = R_L$ [12]. Since the semiconductor layer is very thin, the main contribution to R_{TEG} is the contact resistance.

Fig. 2(b) shows that a change in the thermal conductance of the contact interface κ_c influences P_{out} only. P_{out} increases when ΔT_{int} increases. Thus, P_{out} of the thin TEG will be strongly influenced by the electrical resistivity and thermal conductivity of the interfaces. Reducing R_c by a factor f increases P_{out} by approximately the same factor. Increasing κ_c by a factor of ten increases P_{out} by a factor of approximately three, or reducing the temperature drop across the interface will reduce the required heating power for the same ΔT_{int}.

III. Material Preparation

A relaxed $Si_{0.8}Ge_{0.2}$ layer was grown epitaxially on lowly doped p-Si (100) substrates using reduced-pressure chemical

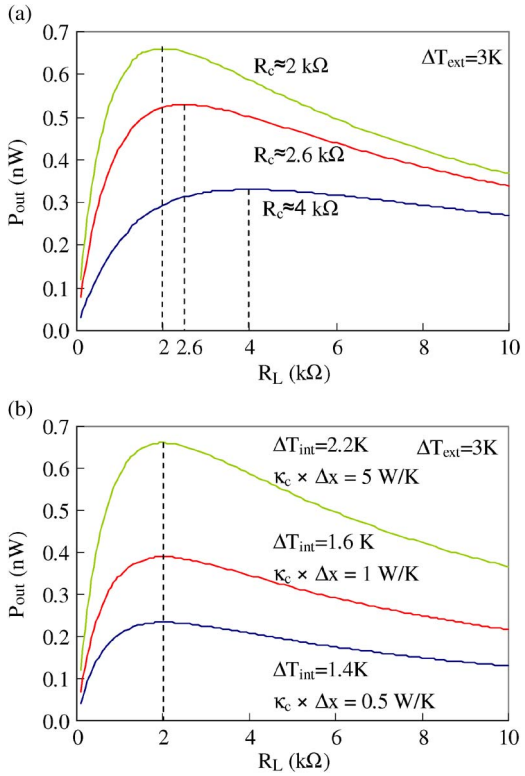

Fig. 2. Simulated output power as a function of load resistance for a 500-μm-thick Si substrate with Cu contacts. The external temperature difference is $\Delta T_{\text{ext}} = 3$ K. An additional $\Delta x = 1$ μm interfacial layer is introduced between Cu and Si representing the electrical and thermal contact resistances of the system. (a) Influence of the total electrical contact resistance R_c. The contact resistivity in each case is $\rho_c = 10^{11}$, 1.3×10^{11}, and 5×10^{11} $\Omega \cdot \mu$m. (b) Influence of the thermal contact conductivity κ_c. The internal temperature difference across the Si bulk is ΔT_{int}.

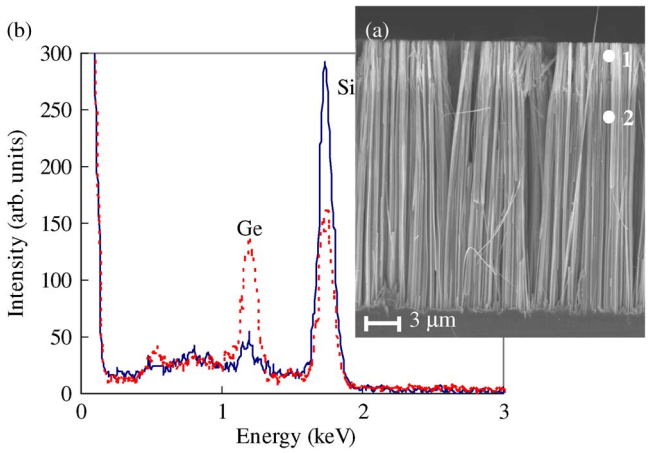

Fig. 3. (a) SEM cross section of a $Si_{0.8}Ge_{0.2}$ NWA after one-step MACE. (b) EDX spectrum of the $Si_{0.8}Ge_{0.2}$ NWA taken at spots (dashed line) 1 and (full line) 2 of (a).

vapor deposition [13]. The resistivity of the p-Si substrate for the SiGe-containing samples is $\rho_{\text{Si}} = 2.7\ \Omega \cdot$ cm, measured by the four-point-probe (4pp) technique. A linearly graded relaxed $Si_{0.8}Ge_{0.2}$ layer (3 μm) was deposited first to overcome the lattice mismatch between Si and SiGe, followed by a 2-μm-thick constant composition layer. The SiGe layer is unintentionally p-doped.

MACE [14], [15] is known to offer a simple and cost-effective way to prepare large-area arrays with long vertically upstanding crystalline Si NWs. MACE is mainly used to etch Si; SiGe is easily attacked by the oxidizing agents in the chemical mixture. Experimental results show that MACE side etching first attacks the defect-rich relaxed $Si_{1-x}Ge_x$ buffer layer, underetching the NW structure [16]. We have developed an adapted etching process based on [17] to avoid the removal of the SiGe layers during etching of SiGe NWs. A single stage $AgNO_3(0.06\ \text{M}) : HF(40\%)$ solution can be used for the etching of SiGe NWs. We have shown that arrays of $Si_{1-x}Ge_x$ NWs with x up to 40% can be fabricated using this one-step MACE process [18]. The etch rate decreases nonlinearly with increasing Ge concentration for the same etch conditions. Scanning electron microscopy (SEM) [Fig. 3(a)] and energy-dispersive X-ray (EDX) spectroscopy [Fig. 3(b)] characterize the SiGe-containing NWAs. The EDX results indicate that the SiGe NWAs are properly prepared with limited side etching using one-step MACE, even for longer etching times. EDX at the top of the NWs in the array [dot 1 in Fig. 3(a)] clearly indicates the presence of Ge. At ~6-μm depth [dot 2 in Fig. 3(a)], the Ge peak is much reduced as it lies inside the Si bulk.

Different NWA-based samples are prepared, all with an NW length of approximately 20 μm and a diameter distribution of 50 nm $< d <$ 250 nm. For the Si bulk and Si NWA, the p-type substrate is $\rho_{\text{Si}} = 5.6\ \Omega \cdot$ cm, determined by 4pp measurements. Small doping densities were chosen to simplify NW fabrication processes and are thus not optimized for thermoelectric performance. For optimization of the output power, the doping concentration needs to be increased to increase the available carrier density [19], [20]. Measurements on NWAs, with different lengths between 40 and 100 μm, allow the extraction of the resistivity of the NW-bulk composite by plotting the total resistance as a function of NW length. An average resistivity of $\rho_{\text{SiNWA}} = 84\ \Omega \cdot$ cm is found. These measurements have a relatively large error (50%) since the total number of NWs in contact with the metal probe varies from sample to sample due to the variation of the length of the NWs in the array. The sample resistivity ρ_{sample} is $0.27\ \Omega \cdot \text{cm} < \rho_{\text{sample}} < 1.6\ \Omega \cdot$ cm, with the upper limit for an error of a factor of ten in ρ_{SiNWA}. Five samples are used for the TEG: bulk Si; SiGe on bulk Si; a 19-μm Si NWA on 480-μm bulk Si (S1); and a 19-μm SiGe/Si NWA on 490-μm bulk Si (S2). These NWs are composed of a constant composition SiGe layer, followed by a graded SiGe layer and a Si layer. The third NWA-based sample (S3) uses the same material as S2; however, a 20-μm Si NWA is etched at the back of the substrate, and the SiGe layer has been left unetched. The thickness of the remaining Si substrate is 480 μm.

IV. Experimental Setup and Measurements

Due to the submillimeter thickness of the thermoelectric (TE) leg, a setup was built to allow contacts for temperature and voltage measurement. A schematic drawing of the setup is given in Fig. 4. Two small Cu blocks, with an area of 2 cm $\times$ 2 cm and

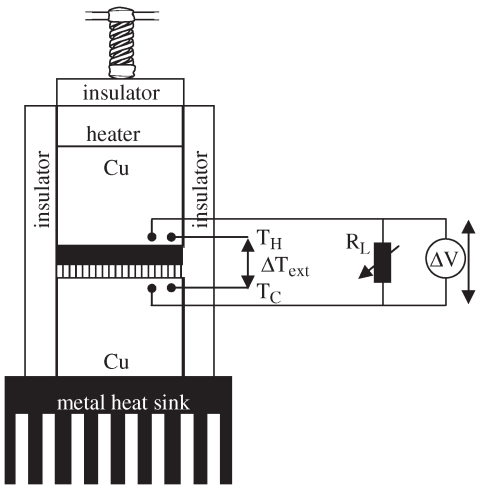

Fig. 4. Schematic drawing of the setup to measure the output power of the TEG. The sample is the black and vertically hatched structure between the Cu blocks. NWA is oriented toward T_C.

a thickness of 0.5 cm, are used as contacts to the sample with a cross-sectional area of 1.5 cm × 1.5 cm. For the NWA side, the effective transport cross-sectional area reduces by approximately 50%, as derived from SEM. The Cu block also provides contacts for the Cu/constantan thermocouples connected to a Fluke 52II digital thermometer and the Cu leads connected to a high-impedance Keithley 2000 multimeter and/or load. In order to decrease the electrical and thermal resistances between the Cu blocks and the sample, a pressure of 200 N is applied in all measurements. No metal contacts are evaporated onto the TE leg to prevent large temperature drops due to the metal–metal interface roughness which have been found to be larger than the Cu block—semiconductor thermal contact resistance [21]. A 10 cm × 10 cm black metal heat sink with cooling fins is used for the cold side. The sides of the TE structure are insulated with a 0.5-cm-thick layer of polystyrene, and the setup is placed in a glove box at atmospheric pressure and room temperature to prevent influences from external air flow variations. Heat is provided by a power resistor clamped to the top of the structure.

Current–voltage measurements were done using an Agilent 4155B semiconductor parameter analyzer. These measurements show that the Cu–semiconductor pressure contacts have a nonlinear character due to the work function difference between semiconductor and Cu and the nano air gaps at the junction. The resistance extracted at the $P_{\rm out}^{\rm max}$ bias point $R_{\rm IV}$ is on the order of kΩ (Table I). We note that $R_{\rm IV}$ for the NWA-based samples is lower than that for bulk. Moreover, since the contact potential barrier is lower for SiGe–Cu than for Si–Cu, due to the work function difference, its contact resistance is lower.

The temperature drop across the TEG is investigated by measuring $\Delta T_{\rm ext}$ with and without the use of silver (Ag) foil. The Cu–semiconductor interfaces present a thermal interface resistance due to tiny air gaps that result from the surface nanoroughness and difference in phonon momenta between materials. A thin layer (∼0.25 mm) of Ag foil is malleable and a good thermal conductor. Adding Ag foil between semiconductor and Cu decreases the thermal interface resistance. The results of the measurements, on a SiGe NWA sample, are given in Fig. 5. These measurements show that $\Delta T_{\rm ext}$ is higher when no Ag foil is used. The difference between $\Delta T_{\rm ext}$ without (x) and with (+) Ag foil is lost across the contact interface. Fig. 5 shows that approximately 50% of $\Delta T_{\rm ext}$ is lost across the interfaces at high heater power levels. This gives an estimation of the temperature loss across the interface.

TABLE I
MEASURED PARAMETERS. $\Delta T_{\rm EXT}$ IS THE MEASURED TEMPERATURE DIFFERENCE, $P_{\rm OUT}^{\rm MAX}$ IS THE MAXIMUM OUTPUT POWER, $R_{\rm TEG}$ IS THE RESISTANCE OF THE TEG DETERMINED FROM THE MAXIMUM POWER POINT, $R_{\rm IV}$ IS THE RESISTANCE OF THE TEG DETERMINED FROM CURRENT–VOLTAGE MEASUREMENTS, AND $V_{\rm OC}$ IS THE OPEN CIRCUIT VOLTAGE

System	ΔT_{ext} (K)	P_{OUT}^{MAX} (nW)	R_{TEG} (kΩ)	R_{IV} (kΩ)	V_{oc} (V)
Si bulk	2.7	0.16	3.6	3.4	1.6
SiGe/Si bulk	3.3	0.31	4.3	3	2.3
S1	3.4	0.34	2.4	2	1.9
S2	4.9	1.08	1.8	0.9	2.6
S3	5.7	3.14	1.3	0.6	4.1

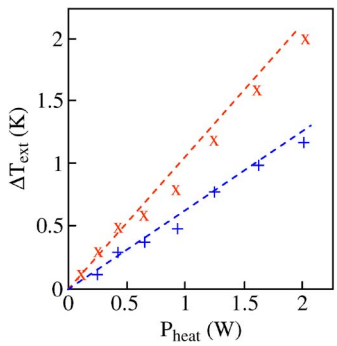

Fig. 5. Measured temperature difference $\Delta T_{\rm ext}$ as a function of heater power $P_{\rm heat}$ for a SiGe NWA sample between two Cu blocks (x) without and (+) with Ag foil at the interfaces. The markers are measurements; the dashed lines are a guide to the eye only.

The Seebeck coefficient α is extracted from the slope of the ΔV versus ΔT plot measured using the Ag foil and a pressure of 200 N. These plots, consisting of a minimum of five measurement points within a temperature range $\Delta T =$ 6 K above room temperature, are linear with very small offset voltage. α is independent of the Ge concentration and NW length ($\leq 20\ \mu$m) and has a value between 1.05 and 1.1 mV/K, which is consistent with the theoretical expected values for a Si wafer of $\rho \approx 5\ \Omega \cdot$ cm [22]. This is not surprising as the NW length and SiGe layer thickness are very small compared to the remaining Si bulk.

The open circuit voltage $V_{\rm oc}$ and $P_{\rm out}$ as a function of R_L are measured for the different TEGs without the use of Ag foil, under 200-N pressure. For all measurements, the heating power $P_{\rm heat}$ supplied is the same. Key performance parameters $\Delta T_{\rm ext}$, $P_{\rm OUT}^{\rm MAX}$, $R_{\rm TEG}$, and $V_{\rm oc}$, extracted from the measurement, are summarized in Table I.

Table I shows that $\Delta T_{\rm ext}$ increases for NWA- and SiGe-based TEGs. $P_{\rm out}$ is generated for very small $\Delta T_{\rm ext}$ in the same range as those in [8] and [9]. Improvements in $P_{\rm out}$ of factors of

TABLE II
MATERIAL PARAMETERS USED IN THE SIMULATIONS AND SIMULATION RESULTS FOR δT_{INT} AND V_{OC}

Material	α (mV/K)	κ (W/mK)	ρ (Ω cm)	ΔT_{int} (K)	V_{oc} (mV)
Si bulk	1.05	130	5.6	1.5	1.5
SiGe bulk	1.13	20	2.7	2.1	2.3
Si NWA	1.05	13	84	1.8	1.8
SiGe NWA	1.13	2	41	2.7	2.8
Si NWA/SiGe	/	/	/	3.7	4

TABLE III
PARAMETERS FOR THE INTERFACIAL LAYER. σ_c IS THE ELECTRICAL CONDUCTIVITY, AND κ_c IS THE THERMAL CONDUCTIVITY

System	$\sigma_c \times 10^{-11}$ (S/μm)	$\kappa_C \times 10^{-6}$ (W/ μm K)
Si bulk	0.56	0.96
SiGe/Si bulk	0.47	1.79
S1	0.84	0.56
S2	1.15	0.6
S3	1.6	1.31

∼2 and ∼20 are obtained for S1 and S3, respectively, compared to bulk Si.

The internal resistance $R_{\rm TEG}$ is found to be of the same order of magnitude as $R_{\rm IV}$. Differences are due to probe position and compression of the tops of the NWA with repeated measurements. $R_{\rm TEG}$ is approximately three orders of magnitude larger than $R_{\rm sample}$.

In order to evaluate the reasons for the performance improvement, the matrix formalism is used to simulate the experimental data by changing the electrical and thermal conductivities of a thin interfacial layer. This allows us to obtain the effective (internal) temperature drop $\Delta T_{\rm int}$ across the TEG without interface effects. The material parameters α and ρ used in the simulations are measured and given in Table II. The thermal conductivity of the bulk materials is taken from [23]. The values of the thermal conductivity of the NWA samples are chosen ten times lower than bulk based on available data on single wires [3], [4]. The resistivity ratio found experimentally for the Si bulk/Si NWA sample is used to estimate the resistivity of the SiGe NWA.

For the simulations, the electrical conductivity of the interfacial layer is first adapted to equal R_L at $P_{\rm out}^{\rm max}$. $R_{\rm TEG}$ changes with bias due to the nonlinear contact. This causes a varying (10%–0%) overestimation (respectively underestimation) of the simulated $P_{\rm out}$ below (respectively above) $P_{\rm OUT}^{\rm MAX}$. In the second step, the thermal conductivity of the interface layer is adapted to equal $P_{\rm OUT}^{\rm MAX}$.

From $T(x)$ and $V(x)$, $\Delta T_{\rm int}$ and $V_{\rm oc}$ for $j = 0$ are extracted. These values are given in Table II. The simulation parameters for 1-μm interfacial layers are given in Table III.

The simulated value for $V_{\rm oc}$ (Table II) is very close to the measured value (Table I). Comparing the simulated value of $\Delta T_{\rm int}$ to the measured value $\Delta T_{\rm ext}$ shows that the simulated interface temperature drop of 45% is similar to the 50% measured in Fig. 5. These results demonstrate a good agreement between experiment and simulation.

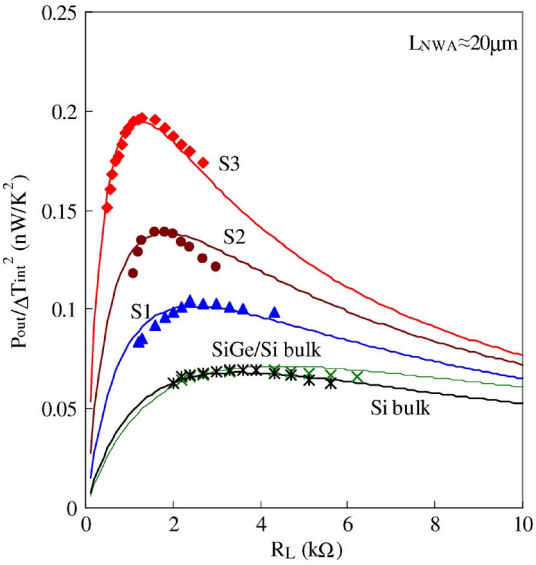

Fig. 6. Output power $P_{\rm out}$ normalized to ΔT^2 as a function of load resistance R_L. The input power is the same in all cases, and the temperature difference across the TE leg is given in Table I. S1: Si NWA; S2: $Si_{0.8}Ge_{0.2}$ NWA; and S3: Si NWA on the hot side and the SiGe layer on the cold side. The markers are measurement, and the full lines are the result of the simulation based on (5) for each TEG.

The simulations and measurements are shown in Fig. 6. To compare results, $P_{\rm out}$ normalized to $\Delta T_{\rm int}^2$ is plotted in Fig. 6 since the temperature differences maintained across the different TEGs for the same $P_{\rm heat}$ are different. This follows the relationship that $P_{\rm out}$ is proportional to ΔT^2 [24].

The value of $P_{\rm OUT}^{\rm MAX}$ is limited by both the temperature drop across the metal–semiconductor interfaces and the contact resistances. The values of $\Delta T_{\rm int}$ confirm that the NWA/SiGe-based materials have a lower thermal conductivity than bulk even for very thin NWA/SiGe layers, improving $P_{\rm out}$. $P_{\rm out}/\Delta T_{\rm int}^2$ shows an additional improvement due to the lower electrical contact resistance of the NWA-based devices.

The lower thermal conductivity, together with the reduced contact resistance in the NWA-based samples, leads to improved output power performance.

V. CONCLUSION

The measurements have shown that the output power of a Si-based TEG is substantially improved by the introduction of short Si or SiGe NWAs (20 μm) and thin SiGe layers (5 μm). The best performance is obtained for a composite material consisting of a Si NWA at the bottom and a SiGe layer at the top of the Si bulk. This structure outperforms the Si bulk sample by a factor of 20. The simulations, based on a novel matrix formalism, corroborate that the effective internal temperature drop increases for NWA-based TEGs.

The simulations, in close agreement with the measurements, have shown that the increased output power is due to the reduced thermal conductivity of the composite NWA/bulk/SiGe material and the reduced contact resistance for the NWA- and SiGe-based samples.

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Authors' photographs and biographies not available at the time of publication.