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Conduction Bottleneck in Silicon Nanochain Single Electron Transistors Operating at Room Temperature

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Single electron transistors are fabricated on single Si nanochains, synthesised by thermal evaporation of SiO solid sources. The nanochains consist of one-dimensional arrays of ~10 nm Si nanocrystals, separated by SiO_2 regions. At 300 K, strong Coulomb staircases are seen in the drain–source current–voltage (I_{ds}–V_{ds}) characteristics, and single-electron oscillations are seen in the drain–source current–gate voltage (I_{ds}–V_{gs}) characteristics. From 300–20 K, a large increase in the Coulomb blockade region is observed. The characteristics are explained using single-electron Monte Carlo simulation, where an inhomogeneous multiple tunnel junction represents a nanochain. Any reduction in capacitance at a nanocrystal well within the nanochain creates a conduction "bottleneck", suppressing current at low voltage and improving the Coulomb staircase. The single-electron charging energy at such an island can be very high, ~$20k_BT$ at 300 K. © 2012 The Japan Society of Applied Physics

1. Introduction

Single-electron devices in silicon, where charge on a nanoscale "island" is controlled at the one-electron level using the "Coulomb blockade" effect,[1–15] are highly promising systems for the development of low electron number, low power, transistor and memory large-scale integrated (LSI) circuits.[16,17] The single electron transistors have also been fabricated in materials other than Si.[18,19] Practical application of these devices requires room temperature operation and therefore a large island single-electron charging energy $E_c = e^2/2C \gg k_B T = 26\,\text{meV}$, where C is the total island capacitance and temperature $T = 300\,\text{K}$. In practice, this requires $C \sim 1\,\text{aF}$ or less and island dimensions $<10\,\text{nm}$, such that the island forms a quantum dot. Room-temperature single-electron transistors (SETs) with islands of this scale have been fabricated mainly using high-resolution electron beam (e-beam) lithography.[20,21] These include both single-island, double-tunnel junction[20,22,23] and many island, multiple tunnel junctions (MTJ) devices.[21] Recent measurements on SETs with ultra-small islands, with diameter down to ~2 nm, show room-temperature single-electron oscillations in the drain–source current–gate voltage (I_{ds}–V_{gs}) characteristics with very large peak–valley ratios, ~100 or greater.[23–25] However, a "Coulomb staircase"[1] in the drain–source current–voltage (I_{ds}–V_{ds}) characteristics can be less well resolved. The devices may be defined by complex high-resolution lithography[20–23] or alternatively, defined "naturally" by material growth techniques. Examples of the later approach include SETs fabricated using nanocrystalline Si thin films, where crystalline Si grains ~10–30 nm in diameter form charging islands.[18,24,26] These techniques raise the possibility of control over the island morphology at the nanoscale by controlling growth parameters.

Recently, we have observed strong Coulomb staircases at room temperature in the MTJ formed by a single Si nanochain.[27] The Si nanochains, prepared by thermal evaporation of SiO solid sources,[28,29] consist of one-dimensional arrays of ~10 nm diameter Si nanocrystals (SiNCs) separated by narrow SiO_2 regions. Here, the SiNCs form charging islands and the SiO_2 regions form tunnel barriers. Nanochain synthesis allows the preparation of very large "bulk" quantities of MTJs and Si quantum dots. In these MTJs, both islands and tunnel barriers are naturally-defined in entirety. Furthermore, in contrast with nanocrystalline Si thin films,[18,24,25] variations in SiNC size and separation within the same nanochain are better controlled (±16% variation).[27] Other investigations of these systems include measurement of electron tunneling in ensembles of Si nanochains using *in situ* scanning electron microscopy,[30] non-gaussian fluctuations in charge transport in Si nanochains,[31] electrical breakdown of individual nanochains,[32] and a theoretical prediction of negative differential conductance with large peak to valley ratio.[33] However, the detailed mechanism for single-electron effects in the nanochains, and the possibility of gate-control, is unclear.

In this paper, we report the I_{ds}–V_{ds} and I_{ds}–V_{gs} characteristics of room-temperature SETs fabricated using single Si nanochains. At 300 K, strong Coulomb staircases with varying current step height are seen in the I_{ds}–V_{ds} characteristics, and single-electron oscillations are seen in the I_{ds}–V_{gs} characteristics. The temperature dependence of the Coulomb staircase from 300–20 K shows a large increase in the width of the Coulomb blockade region. The new experimental data sets presented here that were not present in ref. 27 consist of a temperature dependence of the I_{ds}–V_{ds} curves, arrhenius curve and single electron oscillations. We investigate these characteristics using single-electron Monte Carlo simulations of an MTJ where the gate capacitance C_g at the islands is significant compared to the tunnel junction capacitance C. Here, the effective capacitance C_{eff} for islands within the MTJ is reduced due to the presence of the capacitive array on either side, strengthening the Coulomb staircase at 300 K. The corresponding single-electron charging energy can be very large, $E_c = e^2/2C_{eff} \sim 0.3\,\text{eV} \sim 11k_BT$ at 300 K. Furthermore, we find that the

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essential features in our data may be explained by inhomogeneity in the MTJ, where the total capacitance at an island well within the MTJ is reduced. The higher charging energy associated with such an island (up to $\sim 20 k_B T$ at 300 K) leads to a "bottleneck" in conduction, suppressing current at lower voltages and leading to larger current steps in the Coulomb staircase. The formation of the "conduction bottleneck" is the key finding of this paper and was not discussed in the ref. 27. Only experimental data for a device with eight junctions MTJ was taken from ref. 27 to discuss the formation of the conduction bottleneck in addition to new experimental data.

2. Device Fabrication

The Si nanochains were synthesised by thermal evaporation of high purity (99.99%) SiO powder solid source at 1400 °C, in a quartz tube furnace.[28,29] Ar gas carried the vapour through the tube, and nanochains were synthesised in a cooler part of the furnace, at ~900 °C. Depending on growth conditions 10–50% nanowires may be present with the nanochains. The nanochains were undoped and consisted of SiNCs separated by SiO_2 "necks". Figure 1(a) shows a scanning electron micrograph of a nanochain. X-ray diffraction and high-resolution transmission electron microscopy indicated that SiNCs in the nanochain were crystalline. Figure 1(b) shows a high resolution transmission electron micrograph of nanochains dispersed on a copper grid from isopropyl alcohol (IPA) solution. The image is slightly under-focused to emphasise diameter variations. The SiNC diameter in different nanochains varies from <10 to ~30 nm. The SiNC marked with arrow has a diameter ≈12 nm. A thin SiO_2 layer, ~1–3 nm thick, exists on the SiNCs outer surface. The widths of the necks vary from the diameter of the SiNCs to well below this value. The as-synthesised, sponge-like material was then dissolved in IPA (0.1 mg/3 ml) using ultrasonic tip agitation for 5 min, for spin-coating on suitable substrates.

Silicon nanochain SETs were fabricated using e-beam lithography to define contacts, using poly(methyl methacrylate) (PMMA) resist. Figure 1(c) shows a schematic diagram and Fig. 1(d) shows a scanning electron micrograph of a nanochain SET. Here, the Si substrate is used as a back-gate. The devices were defined on a ~100 nm thick SiO_2 layer, grown thermally on a doped silicon substrate. The surface of the SiO_2 was treated with hexamethyldisilizane (HMDS) vapour for 3 min to promote adhesion. The nanochain solution was then spun onto the SiO_2 surface at 5000 rpm for 30 s to deposit nanochains on SiO_2. Individual nanochains were then selected using scanning electron microscopy. Electrical contacts consisting of a 20 nm Ti/75 nm Al layer were then defined on individual nanochains using thermal evaporation. The source–drain contact separation defines the length of the nanochain segment, and the number of islands, in the device.

3. Experimental Results and Discussion

The nanochain SETs were electrically characterised in vacuum ($\sim 10^{-6}$ mBar) using a low temperature probe station, BCT-43MDC from Nagase, and an Agilent B1500A semiconductor device analyser. Figure 2(a) shows the I_{ds}–V_{ds} characteristics at 300 K from a device where the

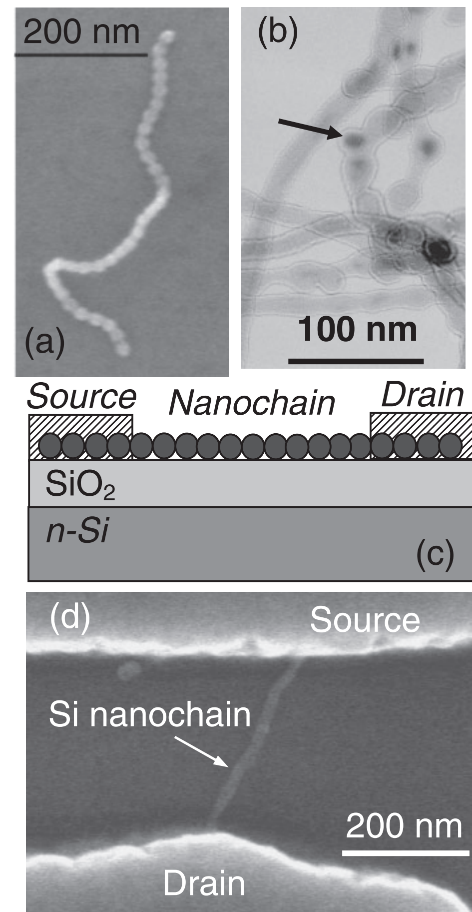

Fig. 1. (a) Scanning electron micrograph of a Si nanochain deposited on SiO_2. (b) Transmission electron micrograph of Si nanochains dispersed on a copper grid. (c) Schematic diagram of the silicon nanochain SET. (d) Scanning electron micrograph of a Si nanochain SET.

source–drain separation was ~150 nm, corresponding to a chain of 7 SiNCs at $V_{gs} = 0$. A Coulomb staircase characteristic is observed, with a low current "Coulomb gap" region at low voltage. The edges of the Coulomb gap are rounded due to thermally activated current. We extract threshold voltages for conduction $V_{+t1} = 0.4$ V and $V_{-t1} = -1.3$ V by plotting the absolute value of the current on a log scale, to determine the onset of current [Fig. 2(a) inset]. We also see current steps in the characteristics outside the Coulomb gap, e.g., at ~2 and ~3.6 V.

In our previous paper[27] temperature dependence of I_{ds}–V_{ds} characteristics was not studied. Figure 2(b) shows the temperature dependence of the I_{ds}–V_{ds} characteristics, as the temperature is varied from 300–20 K, in steps of 40 K at $V_{gs} = 0$. The Coulomb gap increases as the temperature is reduced, with a large increase in the magnitude of the threshold voltages on both sides. For positive V_{ds}, the threshold voltage increases in magnitude from $V_{+t1} = 0.4$ V at 300 K, to $V_{+t2} = 2$ V at 20 K [Figs. 2(a) and 2(b), insets]. For negative V_{ds}, the threshold voltage decreases from $V_{-t1} = -1.3$ V to $V_{-t2} = -2.6$ V. The Coulomb gap is seen to increase greatly, from ~1.7 V at 300 K to ~4.6 V at 20 K. This increase is much larger than can be explained by the reduction in the thermally activated current around V_{-t1} and V_{+t1}.

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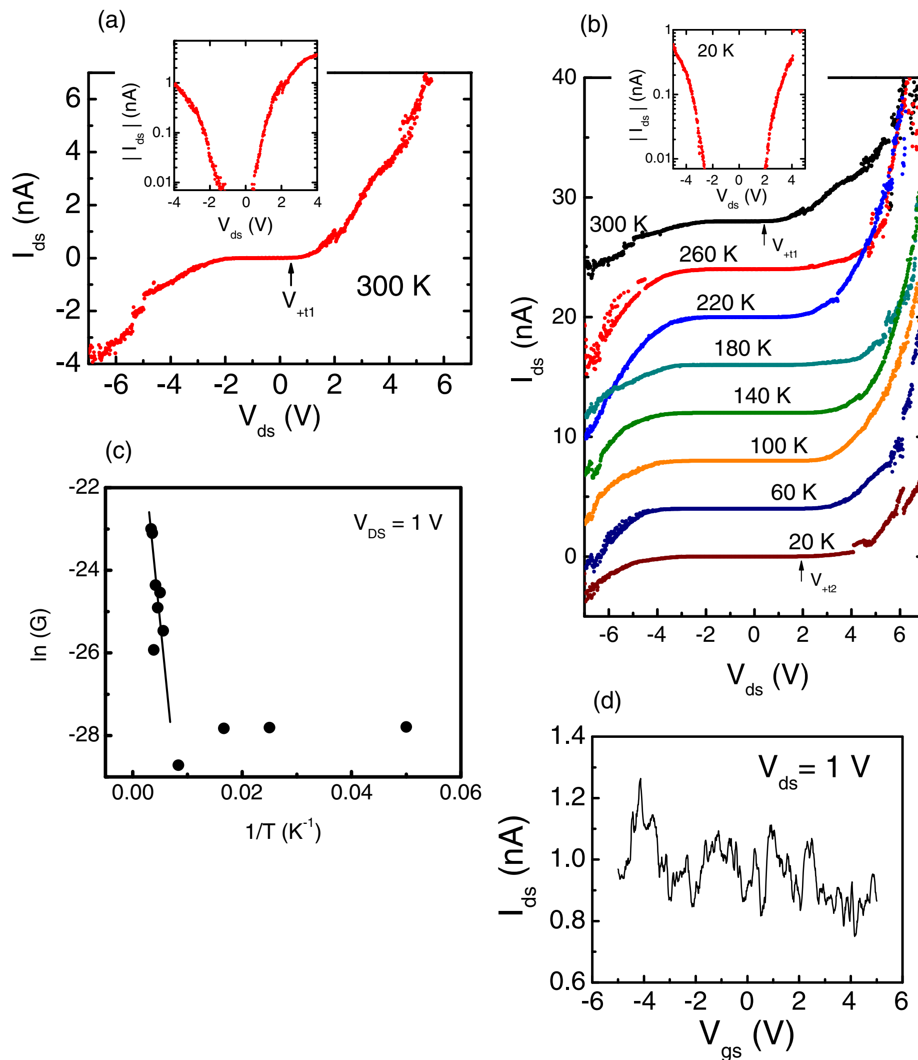

Fig. 2. (Color online) (a) I_{ds}–V_{ds} characteristics of a nanochain SET at 300 K. The inset shows the data on a log–linear $|I_{ds}|$–V_{ds} plot at $V_{gs} = 0$. (b) Temperature dependence of the I_{ds}–V_{ds} characteristics for the same device at $V_{gs} = 0$. The inset shows the data at 20 K on a log–linear $|I_{ds}|$–V_{ds} plot. (c) Arrhenius plot of the logarithm of conductance G as a function of inverse temperature $1/T$. (d) Current oscillations in the I_{ds}–V_{gs} characteristics of a second, similar nanochain device, at 300 K and $V_{ds} = 1$ V.

Figure 2(c) shows an Arrhenius plot of the logarithm of conductance $\ln G$ vs inverse temperature $1/T$, measured at $V_{ds} = 1$ V. V_{ds} is chosen to correspond to $> V_{+t1}$ for current at 300 K. For temperatures from 300 to ~140 K (corresponding to inverse temperature $1/T$ from 0.0033 to 0.0071 K^{-1}), the conductance decreases linearly as the thermally activated conductance falls, from 2.31 to 0.15 nS. This corresponds to an activation energy $E_A \sim 100$ meV, and may be attributed to the highest charging energy in the SiNCs along the nanochain.[34]

Single electron transistor oscillations were not discussed in our previous paper.[27] Therefore we measured single electron oscillations in Si nanochain devices. Figure 2(d) shows current oscillations in the I_{ds}–V_{gs} characteristics of a second, similar nanochain device at 300 K, at $V_{ds} = 1$ V. The different device was used because the first device was damaged during the measurements. The oscillations are however weak, and do not show a single clear period. Any variation in the SiNC to back-gate capacitance along the MTJ would prevent the observation of single-period oscillations. Furthermore, the presence of traps along the interface between the Si nanochain and the underlying, exposed SiO_2 surface would also degrade the oscillations. "Free energy" analysis[34] suggests that Coulomb oscillations in an MTJ are periodic only for small deviations in the gate capacitance C_g, with period $e/\langle C_g \rangle$, where $\langle C_g \rangle$ is the average over all islands. This is not the case in our devices, suggesting large variation in C_g.

Our electrical characteristics may be associated with the formation of an MTJ along the nanochain. Figure 3(a) shows the circuit diagram of a homogenous N island MTJ, with the same tunnel junction capacitance C and the island-gate capacitance C_g along the MTJ. Looking from an island k well within the MTJ [Fig. 3(b)] at zero V_{gs}, we may approximate the capacitive half-arrays on either side as semi-infinite, with capacitance C_h.[1] The "effective" capacitance seen from k is then $C_{eff} = C_g + 2C_h$. Approximating half-arrays C_h at islands $k-1$ and $k+1$, we also have $1/C_h = 1/(C_g + C_h) + 1/C$ [Fig. 3(c)] and rearranging this gives $C_h = (1/2)(\sqrt{C_g^2 + 4CC_g} - C_g)$. Substituting C_h into the expression for the effective capacitance gives us $C_{eff} = \sqrt{C_g^2 + 4CC_g}$.[1] We note that as $C_h < C$, $C_{eff} < C_t =$

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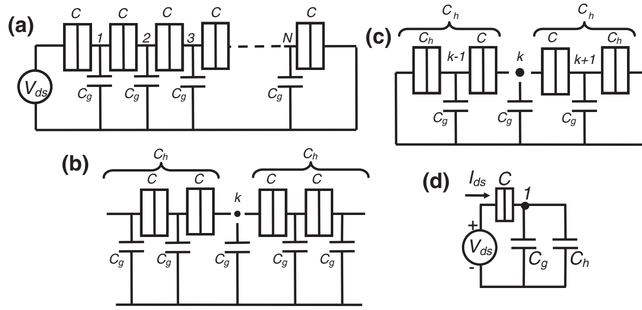

Fig. 3. (a) Multiple-tunnel junction model for an N island Si nanochain, with tunnel junction capacitance C and gate capacitance C_g. (b) Multiple-tunnel junction approximation using Two semi-infinite capacitive arrays C_h at islands k. (c) Multiple-tunnel junction approximation using capacitive arrays C_h at islands $k+1$ and $k-1$. (d) Multiple-tunnel junction approximation looking from island 1.

$C_g + 2C$, where C_t is the total capacitance connected to the island. This increases the charging energy $E_{c,k} = e^2/2C_{eff}$ at island k in comparison with a single-island, double tunnel junction, and a corresponding increase in the MTJ SET operating temperature.

We next consider the effect of C_g on the threshold voltage V_t. Looking from the first island, C_h lies in parallel with C_g [Fig. 3(d)]. V_{ds} then causes a voltage $V_1 = (C_g + C_h)V_{ds}/(C + C_g + C_h)$ across the first junction. At the threshold voltage V_t, eV_1 is equal to the charging energy $E_{c1} = e^2/[2(C + C_g + C_h)]$ and electrons are injected into the MTJ. This gives $V_t = e/[2(C_g + C_h)] = e/(C_g + C_{eff})$. If C_g is negligible, then the island sees a one-dimensional (1D) array of capacitances C towards the right, with very small C_{eff}. In consequence, $E_{c1} = eV_1$ only at relatively high V_{ds}, leading to a large value of V_t. However, as C_g increases, greater voltage drops across the first junction, lowering V_t. For example, for $C_g = C$, $C_h = 0.62C$ and $V_1 = 0.62V_{ds}$, i.e., the majority of applied voltage drops across the first junction.

We now consider the effect of an inhomogeneity in the MTJ. If the island k is poorly coupled to the gate, with a negligible value of C_g, then $C_{eff,k} \approx 2C_h$ at k. This increases $E_{c,k} = e^2/2C_{eff,k}$ relative to neighbouring islands and forms a conduction "bottleneck" along the MTJ. The increase in $E_{c,k}$ raises the SET operation temperature relative to a homogenous MTJ, and further still relative to a double tunnel junction. However, a large variation in capacitance along the MTJ would prevent the observation of a single period single-electron oscillation. A similar bottleneck would also form if C is reduced at the island.

We now use single-electron Monte Carlo simulations[35] of inhomogenous MTJs to explain qualitatively the essential features of our experimental data. We use an eight junction MTJ circuit, similar to the nanochain SET measured for Fig. 2. We also assume, for simplicity, equal tunnel junction capacitances C and gate capacitance C_g at all islands. We then remove C_g from one or more islands to form conduction "bottlenecks". Furthermore, as we observe a strong Coulomb staircase, asymmetry may also occur along the tunnel junctions. We include the effect of this by means of a random variation in the tunnel junction resistances R_n, reasonable given the variation in SiNC separation along the nanochain. There is also likely to be an associated variation in C, further increasing MTJ asymmetry and improving the Coulomb staircase. Small variations in the SiNC separation are likely to affect tunnel resistance more than tunnel capacitance. We neglect variation in C in our analysis for simplicity.

Figure 4(a) shows the simulated I_{ds}–V_{ds} characteristics of the eight junction MTJ SET, as one gate capacitance at a time, from the first to the seventh island, is removed. Here, we use $C = 0.12$ aF, and $C_g = 0.1$ aF, giving $C_{eff} = 0.24$ aF and $V_t = e/(C_g + C_{eff}) \approx 0.5$ V. Here, the corresponding value of E_c for a SiNC within the array is very large, $E_c = e^2/2C_{eff} \sim 0.33$ eV, $\sim 12k_BT$ at 300 K. The capacitance values are in the same range as those extracted for nanochain SETs in our previous work,[11] and correspond to the self capacitance of a sphere $\sim$6 nm (sphere is in air) to $\sim$1.5 nm (sphere embedded in SiO_2) in diameter. These values then give the diameter of the conducting core in a SiNC. The average tunnel junction resistance $R_{av} = 1$ GΩ, with ±40% variation in the resistances (0.6–1.4 GΩ). For all C_g present, the threshold voltage is small, $V_t \approx 0.3$ V and the current steps are similar in height. If C_g is removed at one of the islands then V_t increases, e.g., $V_t \approx 0.7$ V if C_g is removed at the central (fourth) island. Our variation in V_t spans the range 0.3–0.7 V, and the experimental value of $V_{+t1} = 0.4$ V at 300 K in Fig. 2(a) lies within this range. If C_g is removed at the fourth island, at this island $C_{eff,k} \approx 2C_h = 0.14$ aF, a reduction compared to $C_{eff} = 0.24$ aF. This increases $E_{c,k} = e^2/2C_{eff,k} = 0.57$ eV $\sim 22k_BT$ at 300 K. This large value explains the clarity of single-electron effects in an inhomogeneous MTJ even at 300 K.

The second current step in Fig. 4(a) becomes more prominent if a given C_g is removed, and the effect is strongest when C_g is removed at the central island (step at $V_{ds} \approx 1.8$ V), implying greater influence of the "bottleneck". As the central island is the most isolated from the contacts, the contribution of C_g to its charging energy is relatively large and removing C_g has the strongest effect. For $V_{ds} > 1.8$ V, the bottleneck charging energy is overcome and the current rises strongly. For $V_{ds} < 1.8$ V, the bottleneck suppresses I_{ds}, lowering the first step in current.

Figure 4(b) shows the temperature dependence of the simulated I_{ds}–V_{ds} characteristics where C_g is removed at the fourth island. As T reduces from 300–4.2 K, the thermally activated current below the second step falls ($V_{ds} < 1.8$ V). This leads to an increase in the observed threshold voltage, from $V_t = 0.7$ V at 300 K to $\sim$1.6 V at 4.2 K. The position of the second step does not change. This follows qualitatively the behaviour of the experimental data in Fig. 2(b), where the threshold voltage increases from $V_{+t1} = 0.4$ V at 300 K, to $V_{+t2} = 2$ V at 20 K.

Figure 4(c) shows the simulated I_{ds}–V_{ds} characteristics for the MTJ with C_g present at varying numbers of islands. Removing C_g at the first island increases V_t compared to an MTJ with all C_g present, from $V_t = 0.3$ to 0.7 V. As C_g is removed from increasing numbers of islands, V_t increases further, until $V_t > 3$ V for all C_g removed. This is due to the reduction in array capacitance looking from the first island into the array, leading to smaller voltage drops across the first tunnel junction and an increase in V_t. Furthermore, as

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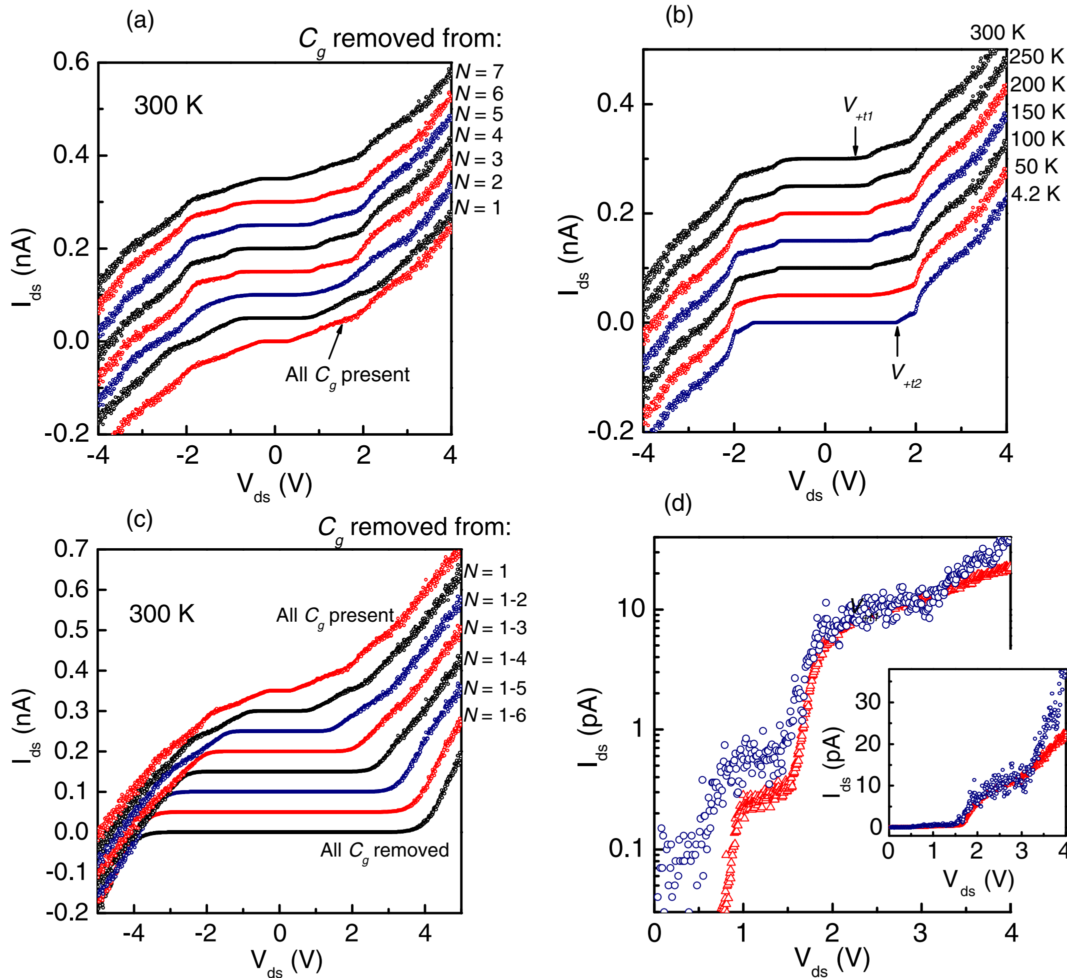

Fig. 4. (Color online) Single electron Monte Carlo simulations for an MTJ with $N = 8$. Curves offset from each other by 0.05 nA for clarity for (a)–(c). (a) Coulomb staircase I_{ds}–V_{ds} characteristics at 300 K, for single C_g removed at an island (b) Coulomb staircase I_{ds}–V_{ds} characteristics from 300–4.2 K, for C_g removed at the fourth island. (c) Coulomb staircase I_{ds}–V_{ds} characteristics at 300 K, for C_g removed at multiple islands. (d) Experimental (circles) and simulated (triangles) data at 300 K for a nanochain SET with eight islands. I_{ds} is plotted using a log (main figure) and linear (inset) scale.

we remove C_g from increasing numbers of islands, the steps in the Coulomb staircase become harder to observe.

In some of our devices, the effect of the bottleneck is very strong. Figure 4(d) shows experimental and simulation data from an eight junction MTJ, where the experimental data is from our earlier work.[27] Here, I_{ds} is plotted on log (main figure) and linear (inset) scales. The very strong second step at ~1.5 V can now be explained by a conduction bottleneck. Removing C_g at the fourth island and using $C = 0.12$ aF and $C_g = 0.12$ aF, the simulation predicts the low value of $V_t = 0.45$ V, a large current step at 1.5 V, and tends to give a rapid rise in current above ~3 V, similar to the experimental data. Here, $C_{eff} = 0.27$ aF, the average tunnel junction resistance $R_{av} = 6\,G\Omega$, and there is a random variation in R_n within 60% of R_{av} (maximum value: 9.4 GΩ, minimum value: 2.8 GΩ). Here, the corresponding value of E_c for a SiNC within the array is $E_c = e^2/2C_{eff} \sim 0.3$ eV, $\sim 11 k_B T$ at 300 K. For the fourth island, $C_{eff,k} \approx 2C_h = 0.15$ aF, a reduction compared to $C_{eff} = 0.27$ aF. This increases $E_{c,k} = e^2/2C_{eff,k} = 0.53\,\text{eV} \sim 20 k_B T$ at 300 K. Furthermore, as the removal of C_g from multiple islands simultaneously weakens the steps in the Coulomb staircase [Fig. 4(c)], the presence of strong steps in our data suggests only one, or at most a few islands, have reduced capacitance.

4. Conclusions

We have studied electrical characteristics of SETs fabricated using single Si nanochains at 300 K. Strong Coulomb staircases with varying current step height were observed in the I_{ds}–V_{ds} characteristics, and single-electron oscillations were observed in the I_{ds}–V_{gs} characteristics. Monte Carlo simulations were used to investigate the characteristics by considering a nanochain as an MTJ, where the gate capacitance C_g at the islands is significant compared to the tunnel junction capacitance C. Here, the effective capacitance C_{eff} for islands within the MTJ is reduced due to the presence of the capacitive array on either side, strengthening the Coulomb staircase at 300 K. $C_{eff} \sim 0.27$ aF for the experimental data in Fig. 4(d), giving a large value of $E_c = e^2/2C_{eff} \sim 0.3\,\text{eV} \sim 11 k_B T$ at 300 K. From 300–20 K, the Coulomb staircase shows a large increase in the Coulomb blockade width, much greater than can be explained by a reduction in the thermally activated current at the Coulomb blockade edge. Furthermore, in some devices, a given current step can be larger than others,

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improving the clarity of the Coulomb staircase at room temperature. We find that the essential features in our data may be explained by inhomogeneity in the MTJ, associated with a reduced total capacitance at an island well within the MTJ. The higher charging energy associated with such an island leads to a "bottleneck" in conduction, suppressing current at lower voltages and leading to a large current step in the Coulomb staircase. The single-electron charging energy at such an island can be very high, $\sim 20 k_B T$ at 300 K.

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