Fabrication of 2D silicon nano-mold based on sidewall transfer

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A method based on the sidewall transfer technique for fabricating two-dimensional (2D) nano-mold on a silicon substrate was developed. Instead of using expensive nanolithography, the authors fabricated 2D silicon nano-mold using standard ultraviolet lithography, conformal deposition of gold by radio frequency sputtering, argon sputter etching and deep reactive ion etching (DRIE). This technique enables the generation of very fine geometries with nanoscale dimensions without the electron-beam (e-beam) lithography equipment or other additional lithography techniques. Based on SF_6, O_2 and C_4F_8 plasmas, a vertical mold profile and a minimum scallop size of 30 nm were obtained by optimising DRIE parameters. For smooth mold surfaces, the authors report and demonstrate a new mechanism of removing 'grass' obtained during inductively coupled plasma etching. With this technique, very uniform 2D silicon nano-molds consisting of 200 nm wide, 200 nm high and 4.3 mm long bar arrays have been successfully fabricated.

1. Introduction: As overall device sizes scale down, their critical dimensions should also be scaled down to the nanoscale region. Nanofabrication methods can be usually divided into two groups: bottom-up and top-down methods. Bottom-up methods begin with atoms or molecules to build up nanostructures, in some cases through smart use of self-organisation [1, 2]. The method is mainly used for the formation of nanotubes and nanotunnels but not for network structures. Consequently, it is not suitable for more general nanofabrication. Top-down methods start with patterns made on a large scale and reduce their lateral dimensions before forming nanostructures. To fabricate a two-dimensional (2D) silicon nano-mold, many techniques have been developed, such as direct laser or focused beam writing [3–5], sacrificial layer surface-machining [6, 7], nano-imprint lithography [8, 9], chemical–mechanical polishing [10], thermomechanical deformation [11] and so on. However, these methods are only marginally useful for nanofabrication because of expensive equipment, complex processing, high fabrication cost or difficulty in controlling accurate linewidth and uniformity.

Among these techniques, electron-beam (e-beam) lithography is the most frequently used technique for nanoscale patterning, but it has very low throughput and the capital costs of the necessary equipment is too high for large-scale application of the technology. In addition, conventional e-beam lithography gives rise to secondary electron effects and proximity effects [12]. While e-beam methods would require considerable development to improve resolution further, other techniques using conventional processes to realise ultra-fine patterns have been pursued. In this research, nanoscale linewidths were easily, accurately and uniformly fabricated by using the sidewall transfer technique.

Sidewall transfer is a process to define line patterns by using a sidewall spacer as an etch mask [13–15]. In this technique, by conformally depositing a material that has a different etching property over a lithographically defined pattern layer and selectively removing the deposited material, the sidewall material is preserved and can serve as a nanoscale mask for further processing. The resolution of this method is not limited by the photolithography but by the thickness of the material deposited. In this respect, the sidewall transfer technique makes it possible to form very fine line patterns without the need of e-beam equipment or other additional lithography. From the economic point of view, it is competitive and has an obvious advantage in accuracy, uniformity and reproducibility, despite the drawback that it requires some additional process steps.

In sidewall transfer, many materials such as SiO_2, Si_3N_4 and so on have been used as mask materials, and deposited by thermal oxidation or chemical-vapour deposition (CVD), both of which need silicon or silicide mesa substrates. The formation of these mesas needs additional processing steps. When fabricating platinum silicide sidewalls, a special salicide process is also needed [15]. All of these make fabrication more complicated. Furthermore, thermal oxidation and CVD always cause high intrinsic stress between substrate and sidewalls because of their high deposition temperatures, which can result in sidewalls peeling off from the substrate. In this Letter, however, a method based on gold deposition as the sidewall material to fabricate a 2D silicon nano-mold over a full four-inch wafer is presented. Gold sputtering on photoresist mesas greatly simplified the fabrication process. In addition, the sputtering and sputter etching process were performed at low temperature, which yields low intrinsic stress. Meanwhile, compared to SiO_2 and Si_3N_4, gold has an excellent plasticity and ductility which release and lower the stress in the deposition and etching process by its deformation, which increases the adhesion between substrate and sidewalls. This method delivers nanostructures over a large area, and can be adapted to provide various geometries by conformal deposition and reactive ion etching (RIE) to meet specific needs by modifying the photolithographic mask design. Finally, a 2D silicon nano-mold consisting of nearly 200 nm wide, 200 nm high, 4.3 mm long bar arrays can be routinely produced.

To fabricate a robust nano-mold, it is necessary to obtain a vertical mold profile with small scallops and smooth sidewall surfaces. Consequently, we pay much attention to optimise the deep reactive ion etching (DRIE) parameters to minimise the scallops, and it is essential to suppress the forming of 'grass' on the silicon surface, which may otherwise result in severe roughness. Here, we suggest and demonstrate a new mechanism for removing 'grass' in an inductively coupled plasma (ICP) etcher system by using SF_6, O_2 and C_4F_8 plasmas.

The application of the nano-mold has been most widely demonstrated for its high potential in economically duplicating polymer nanofluidic chips, which can be applied to control nanofluidic transport, such as sample separation [16], ion purification [17], stretching of DNA and proteins [18, 19] and so on.

2. Method description: Fig. 1 illustrates the silicon nano-mold fabrication process based on sidewall transfer. Here, we briefly present the experimental steps for ease of understanding. For detailed experimental descriptions, readers should refer to the experimental section.

1. The photoresist is spin coated on the wafer, which has previously been treated with hexamethyldisiloxane (HMDS) as an adhesion

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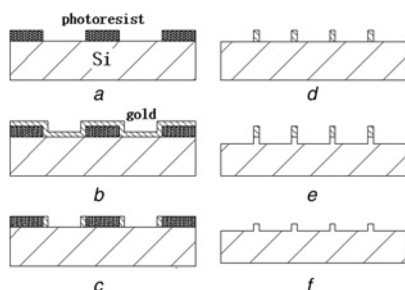

Figure 1 *Schematic diagram of the sidewall transfer process*
a Photoresist mesas
b Gold sputtering
c Argon sputtering etch
d Photoresist removing
e DRIE
f 2D silicon nano-mold

promoting layer. The wafer is then exposed to UV light with a mask containing a 2 μm wide, 4.3 mm long line grating pattern to transfer into photoresist mesas.
2. After the wafer is cleaned in oxygen plasma for 1 min to remove any residues, a layer of gold with a thickness of 200 nm is conformally deposited over these mesas by RF sputtering.
3. The gold is selectively removed from horizontal surfaces by argon sputter etching. The remaining vertical surfaces then act as the sidewalls, whose width is nearly 200 nm and height is 500 nm.
4. The photoresist mesas are removed completely in oxygen plasma. Then the remaining gold sidewalls act as a mask for the next step.
5. The wafer is etched to a depth of 200 nm by a DRIE process, using SF_6, O_2 and C_4F_8 plasmas. In case of clean substrates, oxygen plasma cleaning for 1 min is recommended.
6. After the gold sidewalls are carefully removed in aqua regia, a 2D silicon nano-mold consisting of 200 nm wide, 200 nm high, 4.3 mm long bar arrays is completed.

3. Experimental

3.1. Preparation and photolithography: Fabrication starts with a 100-mm, *n*-type <100> silicon wafer with a thickness of 0.5 mm. To clean the substrate, a baking step at 150°C for 30 min is first used to desorb H_2O. Adhesion promotion is then carried out, by applying a pretreatment with HMDS for 20 min from the gaseous phase on the heated substrate. A positive photoresist (Shipley AZ 701) is spin coated at a speed of 3500 rpm for 30 s on the wafer to a thickness of nearly 500 nm. Note that the coating operation should be performed directly after cooling down the substrate, to avoid re-adsorption of water vapour. Then the wafer is exposed to UV light using a conventional photolithography technique with a mask containing a 2 μm wide, 4.3 mm long line grating pattern. The grating pattern covers the whole 100-mm silicon wafer surface. After the wafer is developed for 20 s, this pattern is transferred into photoresist mesas.

A conventional contact mask aligner (SUSS MicroTec MA/BA6) is used for lithography. The thickness of photoresist and gold layer in step (b) are both measured using a contact surface profiler (Kosaka Laboratory Surfcorder ET 4000M).

3.2. Photoresist removal: A plasma unit with RF generator (Quorum/Emitech K1050X) is used for photoresist removal. The K1050X is a small reactor which consists of a solid-state RF generator and associated tuning circuits, a vacuum system with solenoid valves, a constant feed gas supply system and a reaction chamber system which includes two semicircular electrodes and a two-piece Pyrex chamber. The RF generator is a solid-state crystal controlled oscillator designed to provide up to 150 W of continuous wave 13.56 MHz power to the reaction chamber.

Conditions of the oxygen plasma cleaning run in this configuration are shown as follows: 50 W power, 0.6 mbar pressure and 10 min ashing duration. Note that it is important to sufficiently lower the power sufficiently. Since the energy of the ion bombarding the wafer is in proportion to the forward power, high power can give rise to re-sputtering of gold in bare silicon areas, and the sputtered gold will then form a micro-mask for the subsequent DRIE step.

3.3. Gold sputtering and argon sputter etching: Gold sputter deposition and argon sputter etching are both performed in a thin film deposition system (Kurt J. Lesker LAB18). This equipment serves also as a RF magnetron sputtering system that can be configured to suit a wide variety of process requirements. In the process of sputtering, the gold target acts as the negative electrode and the metal cylinder of the sputtering chamber as the positive electrode. Argon ions generated by efficient inductive coupling of RF power at 13.56 MHz then bombard the target in an electric field. After 3 min pre-sputtering with the shutter closed, the pressure stabilises in the sputtering chamber. Then the shutter plate is opened, and a layer of gold with a thickness of nearly 200 nm is deposited over the mesas by sputtering, shown in Fig. 1*b*.

During sputter etching, the shutter plate is used as the positive electrode and the wafer holder plate as the negative electrode. The distance between the two plates is set to be 36 mm. In this parallel-plate electric field, argon ions will vertically bombard the wafer, so that the gold is selectively removed, as shown in Fig. 1*c*. Owing to the differences in etching rate that follow from the ion directionality, the horizontal gold layers can be selectively removed from the mesas by careful control of the etch time. The vertical gold sidewalls are then left to act as the mask during the subsequent DRIE process.

The parameters of gold sputtering in our system are as follows: 150 W power, 3 mTorr pressure, 14.5 sccm argon, 25 min process duration. As measured by a Kosaka Laboratory Surfcorder ET 4000M surface profiler, the thickness of the gold layer is 217 nm.

The parameters of argon sputter etching in this configuration are as follows. The process is divided into two phases: (i) 100 W power, 11 mTorr pressure, 61.8 sccm argon, etched for 3 min to obtain stable RF-induced gaseous discharge and (ii) a decrease in pressure to 5 mTorr, continued for 33 min until the horizontal gold layers are completely removed.

3.4. Deep reactive ion etching: DRIE is carried out using an ICP etcher (ALCATEL AMS100SE ICP etcher) as shown in Fig. 2. The plasma source generates very high density plasmas by efficient inductive coupling of RF power at 13.56 MHz in a dielectric alumina cylinder. A good and homogeneous thermal contact between the wafer and the substrate holder is obtained by setting

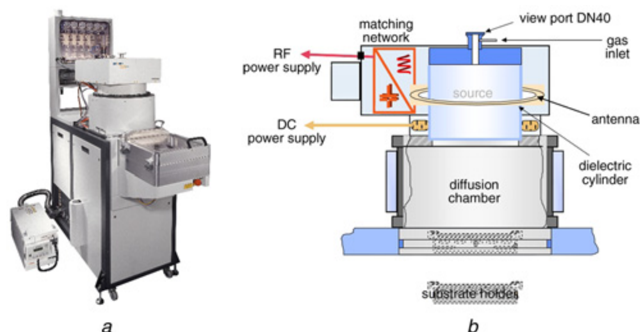

Figure 2 *Alcatel AMS100 ICP etcher system*
a Picture of Alcatel AMS100 ICP etcher system
b Schematic diagram of Alcatel AMS100 ICP etcher system

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of 10 mbar of helium pressure. The wafer is cooled down to 10°C by the helium back side flow, while the temperature of the diffusion chamber is reduced and controlled appropriately. The distance between the plasma source and the substrate holder is set to be 200 mm.

Research into the relation between DRIE parameters and scallops in our ICP etcher system was performed. For these experiments, 100 mm wafers coated with 0.5 µm-thick photoresist containing a 2 µm wide, 4.3 mm long line grating pattern were used, shown in Fig. 1*a*. The mask for DRIE is photoresist, which covers almost the whole wafer and leaves little silicon exposed. SF_6, O_2 and C_4F_8 gases were used as plasmas for etching and the effect of the main process parameters (including pressure, gas flow, substrate holder power and etching/passivation cycle duration) on the influence of the scallops and etch rate was assessed. This research will provide a framework for tuning the DRIE parameters to form our nano-mold structure using 100 mm wafers with gold sidewalls as a mask, as shown in Fig. 1*d*.

A mixture of SF_6 and O_2 was first passed into chamber for 3 s (the etching cycle), followed by C_4F_8 for 2 s (the passivation cycle). The experimental variables were gas flow, etching/passivation cycle duration, chamber pressure, source power and substrate holder power. All experimental samples were etched for 3 min. The optimum ICP process conditions run in this configuration are shown in Table 1.

Unfortunately, a major problem was the formation of so-called 'grass' on the silicon surface during a DRIE process with gold sidewalls as a mask using the conditions shown in Table 1 (as shown in Fig. 6*a*). The main reason for 'grass' formation is different silicon loading. The wafers used for scallop minimisation studies were covered by a photoresist mask with little silicon exposed ($<5\%$), as shown in Fig. 1*a*. However, when etching wafers with gold sidewalls act as a mask, most of the silicon was exposed ($>99\%$), as shown in Fig. 1*d*. The silicon loading in the latter case was so high that the plasma density in the average silicon area was greatly decreased, which resulted in the 'grass'.

During research into 'grass' removal, we inherited and optimised the conditions shown in Table 1 for small scallops. Meanwhile, based on a new mechanism of removing 'grass', we suppressed the 'grass' growth by tuning the substrate holder power of C_4F_8 which hardly affected scallop formation. For these experiments, we increased the O_2 flow to 14 sccm, decreased the pressure to 0.015 mbar and gradually increased the substrate holder power for C_4F_8 to 40 W to obtain small scallops and minimal 'grass' at the same time.

The etched structure properties, such as the etching rate, etch profile, scallops, 'grass' and so on, were measured by scanning electron microscopy (SEM; JEOL JSM-6360LV).

4. Results and discussion

4.1. Scallop minimisation: Fig. 3 shows the effects of the etching/passivation cycle and pressure on etch rate and scallop size, as measured from SEM micrographs. As shown in Fig. 3*a*, with the increase of etching/passivation cycle from 3 s/2 s to 7 s/3 s, the scallop size of microchannel sidewalls was increased significantly, due to the isotropic etching character of SF_6 during the etching cycles. At the same time, there was a corresponding change in the etch rate. When the etching cycle duration was held at 3 s, the etching effect of SF_6 was not noticeable, and lateral etching was

Table 1 Optimal ICP process conditions used for small scallops

Gas	Flow, sccm	Cycle duration, s	Pressure, mbar	Source power, W	Substrate holder power, W
SF_6/O_2	140/7	3	0.024	1500	40
C_4F_8	125	2	0.019	1500	0

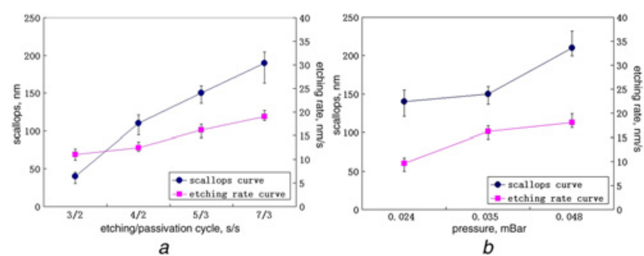

Figure 3 *Scallop size and etch rate were measured as a function*
a Etching/passivation cycle under 0.035 mbar pressure
b Pressure with 7s/3s etching/passivation cycle, other parameters: 140 sccm SF_6, 7 sccm O_2, 125 sccm C_4F_8, 40 W substrate holder power

relatively slight. As a result, the scallop size was the smallest, only 30 nm. When the etch cycle was increased to 4 s, the scallop size increased rapidly, and finally reached 210 nm at a maximum of 7 s. Obviously, the size of the scallops is proportional to the etching/passivation cycle duration, and better vertical sidewall surfaces with smaller scallops can be achieved by using short cycles. Fig. 4 shows the SEM micrographs of the microchannel cross-section pattern for various etching/passivation cycles, (*a*) 7 s/3 s and (*b*) 3 s/2 s, respectively.

As the pressure was increased from 0.024 to 0.048 mbar, the etch rate was increased from 9.4 to 17.6 nm/s, and the scallop size increased from 160 to 230 nm, as shown in Fig. 3*b*. At different plasma densities, the pressure is proportional to the concentration of the reactive species that are responsible for the chemical component of the etching mechanism. Increasing the pressure results in the production of more radical and surface reactions. Consequently, it will clearly lead to more intense etching in the vertical and horizontal directions, which increases the etching rate and the rate of scallop formation, respectively. Lower pressure helps to reduce scalloping.

Fig. 5 shows the effect of the substrate holder power and oxygen flow rate on etching rate and scallop size. As shown in Fig. 5*a*, when the substrate holder power was increased from 40 to 80 W,

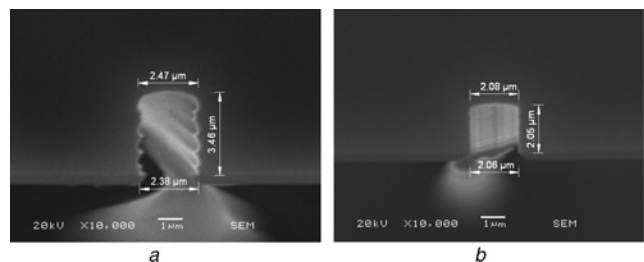

Figure 4 *SEM cross-section view of 2 µm wide microchannel*
a Etched in 7 s/3 s
b In 3 s/2 s etching/passivation cycle, other parameters: 140 sccm SF_6, 7 sccm O_2, 125 sccm C_4F_8, 0.035 mbar pressure, 40 W substrate holder power

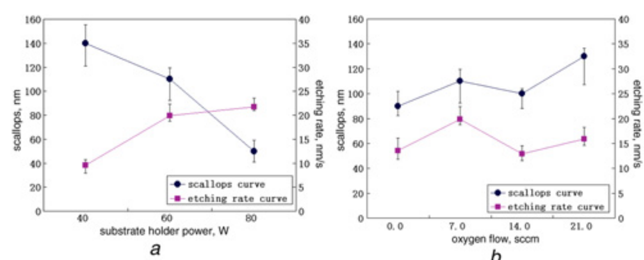

Figure 5 *Dependency of scallops and etch rate*
a Substrate holder power with 7 sccm O_2
b O_2 flow at 40 W substrate holder power. Other parameters: 140 sccm SF_6, 125 sccm C_4F_8, 0.024 mbar pressure, 5 s/3 s etching/passivation cycle

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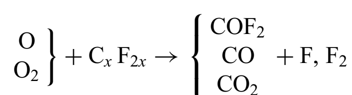
the etch rate was accelerated from 9.4 to 21.2 nm/s, but the scallop size decreased from 140 to 40 nm. Scalloping occurs when chemically reactive fluorine is absorbed on the sidewall surface in localised isotropic silicon etching cycles. With increasing of substrate holder power, the density of fluorine plasma available for lateral bombardment is reduced because of the effect of the stronger vertical electric field. As a result, the minimum of 40 nm scallop size was observed at high substrate holder power of 80 W. However, when used for wafers etching with gold sidewalls as a mask, substrate powers of 60 and 80 W caused serious damage to the sidewalls because of the high ion bombarding energy. To reduce this damage, a lower substrate power (40 W) was chosen.

Fig. 5*b* indicates a fluctuation in etch rate and scallop size with increasing the oxygen flow. Obviously, with an increase in flow, the etch rate reached a maximum at 5% O_2 content (7 sccm). When continuing addition of more O_2 to the SF_6 gas, the etch rate decreased. After the O_2 content exceeded 10% (14 sccm), the etch rate rose again. The maximum and minimum etch rates were 19.5 and 12.9 nm/s, and the scallop size reached its own maximum and minimum at the same oxygen flow. In addition, the scallop formation curve is in a great agreement with the etch rate curve, because the etch rate variation directly determines the depth of lateral erosion.

In SF_6 and C_4F_8 plasmas, the relationship of O_2 with the etch rate and scallop size is complicated, which could possibly be explained by the passivation mechanism of oxygen and C_4F_8. At low oxygen concentrations, further increments of O_2 can facilitate the conversion of SF_6 to F radicals. The result is an increase in the concentration of F radicals, leading to an increase in the silicon etch rate. At high O_2 concentrations, however, there is competition between the F and O radicals for reaction with silicon; the former resulting in etching, the latter acting to passivate the silicon surface by forming SiO_xF_y that protects the silicon against reaction with F radicals, thereby, causing a decrease in silicon etch rate with further increase in O_2 concentration [20, 21].

However, in our work, when the concentration exceeded 10% (14 sccm), excessive O_2 and O radicals reacted with C_xF_{2x} radicals that were converted from C_4F_8. This reaction will result in generation of more F_2 and F radicals and will accelerate the silicon etch, which spontaneously increases scallop sizes. The reaction equation is shown as follows [22]:



$$\left.\begin{matrix} O \\ O_2 \end{matrix}\right\} + C_x F_{2x} \rightarrow \left\{\begin{matrix} COF_2 \\ CO \\ CO_2 \end{matrix}\right. + F, F_2$$

Based on the relations between the main ICP parameters and the resulting scallops, the optimum conditions needed to achieve small scallops with photoresist as a mask are obtained, as shown in Table 1.

4.2. 'Grass' removal: In plasmas based on SF_6 and O_2 gases, SF_6 generates fluorine radicals that etch the silicon forming the volatile SiF_4, while O_2 gives rise to oxygen radicals that passivate the silicon surface with SiO_xF_y. At certain oxygen content, there is a competition balance between the etching and the passivation that results in a nearly vertical wall. At the same time, in the etching cycle some substances such as native oxide, dust, residues, and so on can act as micro-masks, and then spikes will appear because of the directional etching. Then in the passivation cycle, these spikes will be deposited with a thin layer of silicon oxyfluoride protecting the silicon inside from further etching. Depending on the etch rate, these spikes will become higher in time until 'grass' appears [23].

There is a similar mechanism in plasmas based on SF_6 and C_4F_8 (or CHF_3) gases [24]. In both processes, an inhibitor is added to fluorine-based plasmas to form a competition balance for directional etching, which is formed from an oxide-forming (O_2) or a fluorocarbon gas (C_4F_8 or CHF_3), and the passivation skin is separately by the SiO_xF_y or a fluorocarbon layer.

As stated above, the 'grass' will obviously appear in such plasmas when directional etching is performed to create a vertical wall. Although the 'grass' can be controlled by tuning pressure and substrate holder power, this method will also change the profile of a nano-mold. In our study, to simultaneously decrease and eventually remove the scallops and 'grass', we propose a new mechanism for optimising a DRIE process as follows. Using SF_6, O_2 and C_4F_8 plasmas for etching, there are three constant competitions in the DRIE process. As stated above in Table 1, the first is between SF_6 (that etches the silicon) and O_2 (that passivates) in the 3 s etching cycle. The purpose of adding a small amount of O_2 to the SF_6 is to minimise the scallops. At the same time, the SiO_xF_y passivation layer on the silicon surface can act as micro-mask for further etching. The second competition is between O_2 (forming the SiO_xF_y layer) and C_4F_8 (which is the source for the CF_x^+ ions that etch the SiO_xF_y layer in one direction. forming the volatile CO_xF_y). Without the SiO_xF_y passivation layer providing a skin on these spikes, 'grass' can be inhibited remarkably well. After CF_x^+ ions remove the SiO_xF_y layer completely, they continue to passivate the exposed silicon to form a fluorocarbon layer. Then the third competition between SF_6 and C_4F_8 appears, and the result of this final competition balance is the predominant factor deciding the eventual profile of the nano-mold structure.

Based on this mechanism, by gradually increasing the substrate holder power for C_4F_8, the optimum conditions of 40 W for both small scallops and minimal 'grass' with gold sidewalls are obtained, as shown in Table 2.

Fig. 6*b* shows SEM cross-section micrographs of the silicon nano-mold after etching for 5 min in SF_6, O_2 and C_4F_8 plasmas. In comparison with Fig. 6*a*, 'grass' is greatly eliminated and the problem of surface roughness is properly solved, and the situation of scallop minimisation is fairly satisfactory as well. The nano-mold is 150 nm in width and 3.5 μm in height, so the etch rate is nearly 700 nm/min on average. The profile is shown to be tapered; however, this aspect is useful for demolding in a process that involves polymer casting for nanochannel fabrication. By reducing the etch time to about 20 s, we can obtain a more robust 2D silicon nano-mold with the height of nearly 200 nm.

Based on the sidewall transfer technique, by combining of the conformal deposition of gold sputtering, argon sputter etching

Table 2 Optimal ICP process conditions used for both small scallops and low 'grass' formation with gold sidewalls as a mask

Gas	Flow, sccm	Cycle duration, s	Pressure, mbar	Source power, W	Substrate holder power, W
SF_6/O_2	140/14	3	0.015	1500	40
C_4F_8	120	2	0.01	1500	40

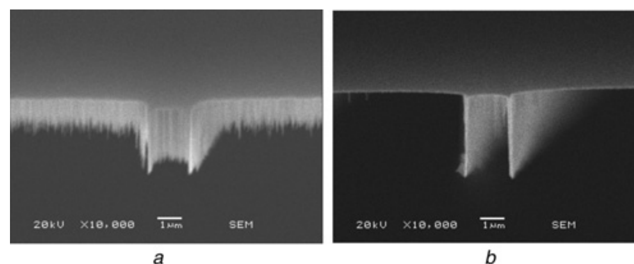


Figure 6 *SEM cross-section view of silicon nano-molds before and after the 'grass' removing step*
a Formation of 'grass' with conditions shown in Table 1
b Effect of 5 min etching in SF_6, O_2 and C_4F_8 plasmas with conditions shown in Table 2

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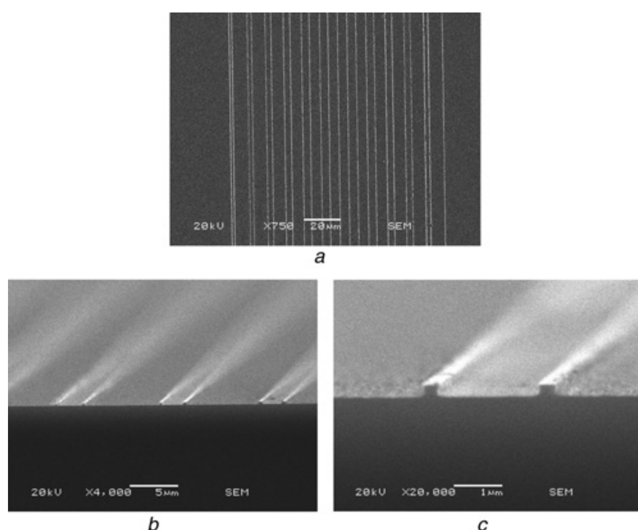

Figure 7 *SEM view of 2D silicon nano-mold with gold sidewalls removed for 20-s etching in SF_6, O_2 and C_4F_8 plasmas with ICP process conditions*
a Plan view of the fabricated line pattern
b Oblique view of cross-section of nanobar arrays with ICP process conditions shown in Table 2
c Enlarged view of two nanobars with nearly 200 nm in width and 200 nm in height

and DRIE, we have successfully fabricated a 2D silicon nano-mold using a conventional photolithography process, shown in Fig. 7. The width, height and length of the silicon nano-mold are nearly 200 nm, 200 nm and 4.3 mm, respectively.

5. Conclusions: In this Letter, a method based on sidewall transfer technique to fabricate a 2D silicon nano-mold over a full wafer is presented. Instead of using expensive nanolithography, we fabricated the nano-mold using standard UV lithography, conformal deposition of gold by RF sputtering, argon sputter etching and DRIE. With this technique, we have successfully fabricated very uniform 2D silicon nano-molds consisting of 200 nm wide, 200 nm high and 4.3 mm long bar arrays. The process generates nanostructures over the whole 100 mm wafer, and can be adapted to comprise various geometries to meet specific needs by modifying the photolithography mask design. Finally, this method shows great potential in fabricating 2D silicon nanostructures. In our future work, poly-dimethyl-siloxane (PDMS) will be cast on the silicon nano-mold for fabrication of 2D polymer nanochannels. By bonding PDMS nano-channel chip and other microchannel chips, we will further investigate the micro- and nanofluidic chips system.

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7 References

[1] Xia D.Y., Brueck S.R.J.: 'Fabrication of enclosed nanochannels using silica nanoparticles', *J. Vac. Sci. Technol. B*, 2005, **23**, pp. 2694–2699
[2] Zeng Y., Harrison D.J.: 'Self-assembled colloidal arrays as three-dimensional nanofluidic sieves for separation of biomolecules on microchips', *Anal. Chem.*, 2007, **79**, pp. 2289–2295
[3] Rill M.S., Plet C., Thiel M., ET AL.: 'Photonic metamaterials by direct laser writing and silver chemical vapour deposition', *Nat. Mater.*, 2008, **7**, pp. 543–546
[4] Mahabadi K.A., Rodriguez I., Haur S.C., van Kan J.A., Bettiol A.A., Watt F.: 'Fabrication of PMMA micro- and nanofluidic channels by proton beam writing: electrokinetic and morphological characterization', *J. Micromech. Microeng.*, 2006, **16**, pp. 1170–1180
[5] Shao P.G., van Kan J.A., Ansari K., Bettiol A.A., Watt F.: 'Poly (dimethyl siloxane) micro/nanostructure replication using proton beam written masters', *Nucl. Instrum. Meth. B*, 2007, **260**, pp. 479–482
[6] Cheng G.J., Pirzada D., Dutta P.: 'Design and fabrication of a hybrid nanofluidic channel', *J. Microlith. Microfab.*, 2005, **4**, article no. 013009
[7] Tas N.R., Berenschot J.W., Mela P., Jansen H.V., Elwenspoek M., van den Berg A.: '2D-confined nanochannels fabricated by conventional micromachining', *Nano Lett.*, 2002, **2**, pp. 1031–1032
[8] Yang B., Pang S.W.: 'Multiple level nanochannels fabricated using reversal UV nanoimprint', *J. Vac. Sci. Technol. B*, 2006, **24**, pp. 2984–2987
[9] Cao H., Yu Z.N., Wang J., ET AL.: 'Fabrication of 10 nm enclosed nanofluidic channels', *Appl. Phys. Lett.*, 2002, **81**, pp. 174–176
[10] Lee C., Yang E.H., Myung N.V., George T.: 'A nanochannel fabrication technique without nanolithography', *Nano Lett.*, 2003, **3**, pp. 1339–1340
[11] Sivanesan P., Okamoto K., English D., Lee C.S., DeVoe D.L.: 'Polymer nanochannels fabricated by thermomechanical deformation for single-molecule analysis', *Anal. Chem.*, 2005, **77**, pp. 2252–2258
[12] Cazaux J.: 'Secondary electron emission and charging mechanisms in Auger electron spectroscopy and related e-beam techniques', *J. Electron Spectrosc.*, 2010, **176**, pp. 58–79
[13] Choi Y.K., Zhu J., Grunes J., Bokor J., Somorjai G.A.: 'Fabrication of sub-10-nm silicon nanowire arrays by size reduction lithography', *J. Phys. Chem. B*, 2003, **107**, pp. 3340–3343
[14] Haneveld J., Berenschot E., Maury P., Jansen H.: 'Nano-ridge fabrication by local oxidation of silicon edges with silicon nitride as a mask', *J. Micromech. Microeng.*, 2006, **16**, pp. S24–S28
[15] Zhang Z., Hellstrom P.E., Lu J., Ostling M., Zhang S.L.: 'A novel self-aligned process for platinum silicide nanowires', *Microelectron Eng.*, 2006, **83**, pp. 2107–2111
[16] Lee S.B., Martin C.R.: 'Electromodulated molecular transport in gold-nanotube membranes', *J. Am. Chem. Soc.*, 2002, **124**, pp. 11850–11851
[17] Qiao R., Aluru N.R.: 'Surface-charge-induced asymmetric electrokinetic transport in confined silicon nanochannels', *Appl. Phys. Lett.*, 2005, **86**, article no. 143105
[18] Abad E., Merino S., Retolaza A., Juarros A.: 'Design and fabrication using nanoimprint lithography of a nanofluidic device for DNA stretching applications', *Microelectron Eng.*, 2008, **85**, pp. 818–821
[19] Guo L.J., Cheng X., Chou C.F.: 'Fabrication of size-controllable nanofluidic channels by nanoimprinting and its application for DNA stretching', *Nano Lett.*, 2004, **4**, pp. 69–73
[20] Zou H.: 'Anisotropic Si deep beam etching with profile control using SF_6/O_2 plasma', *Microsyst. Technol.*, 2004, **10**, pp. 603–607
[21] Knizikevicius R.: 'Simulation of anisotropic etching of silicon in $SF_6 + O_2$ plasma', *Sensor Actuat. A Phys.*, 2006, **132**, pp. 726–729
[22] Flamm D.L., Donnelly V.M.: 'The design of plasma etchants', *Plasma Chem. Plasma Process.*, 1981, **1**, pp. 317–363
[23] Jansen H., Boer M.D., Legtenberg R., Elwenspoek M.: 'The black silicon method 1', *J. Micromech. Microeng.*, 1995, **5**, pp. 115–120
[24] Laermer F., Schilp A.: 'Method for anisotropic plasma etching of substrates'. US Patent 5 501 893, 26 March 1996

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