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1/*f* Noise and trap density in n-channel strained-Si/SiGe modulation doped field effect transistors

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ABSTRACT

The low frequency (1/*f*) noise characteristics of Schottky-gated strained-Si n-channel modulation doped field effect transistors have been investigated as a function of Ge concentration for different virtual substrates. The gate voltage dependence of the 1/*f* noise agrees well with the McWhorter carrier number fluctuations model. The trap density (extracted using a Ge dependent potential barrier height and tunnelling constant) is low in devices on thick virtual substrates ($N_t = (2–6) \times 10^{16}\ \mathrm{cm}^{-3}\ \mathrm{eV}^{-1}$), and does not degrade with the increase of the Ge concentration from 30% to 40%. This trap density is the same for thin Helax virtual substrates (He^+ ions implanted thin substrate) but increases two orders of magnitude for thin low-temperature grown substrates.

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1. Introduction

High electron mobility transistors (HEMT) can deliver high speed and power performance [1]. These structures are traditionally fabricated in III–V materials. A similar approach can be taken for more commonly available IV–IV elements such as Si in combination with SiGe. Schottky-gated n-channel modulation doped Si/SiGe transistors – MODFETs – have a strained-Si (s-Si) channel surrounded by relaxed SiGe layers [2]. One of these layers is the virtual substrate (VS), which is a relaxed $Si_{1-x}Ge_x$ layer on top of a traditional Si substrate. The Ge concentration, *x*, in the VS is graded to allow relaxation of the layer, while preventing dislocation propagation in the growth direction. The strain in the s-Si channel causes a conduction band offset between the s-Si and surrounding SiGe, forming a quantum well channel. The strain also causes an increase in carrier mobility due to the reduction of the effective mass and intervalley scattering. Similarly, s-Si channels can be used for the fabrication of MOSFETs with strain in the channel underneath the gate oxide giving increased speed performance [3]. Electrical noise in FETs gives an indication of the material quality and is important for RF applications. The low frequency noise and trap density in s-Si MOSFETs is mainly determined by the oxide quality on these devices, similar to Si MOSFETs. In s-Si MOSFETs, the trap density can increase with increasing Ge concentration in the virtual substrate (0–40% Ge) on which the strained channel is defined [4]. This degradation is attributed to Ge diffusion during non-optimised high-temperature fabrication steps that reduces the oxide quality. In Ref. [5] a MOS-gated Si/SiGe MODFET with deposited oxides was investigated. The noise in these devices is mainly determined by the oxide–semiconductor interface quality.

Since SiGe is a poor thermal conductor and the traditional VS is 3–5 μm thick, Si/SiGe MODFETs suffer from self-heating at high drain bias. In order to control the self-heating effect and reduce the fabrication costs, thin substrates are used. Thin SiGe VSs have been shown to reduce the self-heating effect [6]. Ref. [6] presented RF noise in this material and some 1/*f* noise results, the latter, however, without further analysis. In Ref. [7] the low frequency noise was studied on s-Si n- and p-type MOSFETs on thin and thick substrates. The thin substrate was grown via a low-temperature growth process. The Ge concentration was different for both substrate types and therefore noise dependence on Ge concentration and substrate growth technique was convoluted. The thick substrate showed unexpectedly higher noise levels than the thin substrate. The extracted trap density in [7] was the lowest reported for s-Si n-channel MOS-gated FETs.

In this work, we investigate Schottky-gated Si/SiGe MODFETs using two Ge concentrations, 30% and 40%. This allows investigation of the trap density as a function of Ge concentration only, thus

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without the influence of gate oxides. Additionally structures with thin and thick VSs were studied.

2. Device description

The MODFET device layers were grown by Molecular Beam Epitaxy (MBE) on Low Energy Plasma Enhanced Chemical Vapour Deposition (LEPECVD) grown VSs on p-doped Si substrates.

In this work four different VSs are considered. Two device layer structures were grown on 5 μm thick standard VSs, where the Ge concentration was graded linearly from Si to $Si_{1-x}Ge_x$ with $x = 0.3$, respectively, 0.4 (thick VS).

Two different methods were used to produce thin VSs in this work. One is the Helax process [8], in which He^+ ions are implanted into a thin constant composition MBE grown SiGe layer. Upon annealing, the relaxation process is induced by the defects introduced by the implant process. This VS was 200 nm thick with composition $x = 0.3$. The other method was based on low-temperature LEPECVD growth of a thin constant composition SiGe layer [9]. The high growth rate at low-temperatures combined with the focused high-density plasma on the surface leads to relaxation and confinement of dislocations. The LEPECVD grown VS was 500 nm thick with composition $x = 0.4$.

Fig. 1 shows the device layer structures. There is only small difference between the layers thicknesses for the different devices. Both 30% MODFETs had a 12 nm thick channel; the 40% MODFETs had a 9 nm thick channel. Fig. 1 also shows the schematic conduction band diagram for the Schottky-gated structures. The tensile strain in the thin Si channel is due to the relaxed surrounding SiGe layers. It causes the energy band offsets in valence and conduction bands ($\Delta E_c \approx 0.6 \times x$ eV, with x the Ge concentration) and leads to a quantum well channel for electrons. The δ-doping in the SiGe supply layers causes depletion mode operation of the MODFETs.

Devices were processed as described in [6] with a maximum fabrication temperature of 600 °C, in order to avoid diffusion of Ge. The mushroom gate material was Ti/Pt/Au with the gate length and width of the measured devices $L_g = 150$ nm and $W = 50$ μm, respectively. The Schottky-gated structures were not self-aligned and the source–drain distance in all measured devices was 2 μm, with the gate in the middle between the source and drain. The contact resistance and access resistance of the devices were measured on TLM structures. These values are important in order to separate the noise generated by the contacts and "long" access regions from that generated by the carriers in the "short" channel. The values of the TLM measurements: contact resistance R_c and access resistance R_{acc}, are given in Table 1. The difference in R_{acc} between the different devices is due to small variations in layer structure and the substrate preparation process that led to different carrier concentrations in the s-Si quantum well. The value of R_c is much lower than that of R_{acc}. Therefore, the noise related to the channel series resistance will be mainly due to the access regions. The gate voltage dependent channel resistance R_{ch}, given by: $R_{ch}(V_{GS}-V_{th}) = \left.\frac{dV_{DS}}{dI}\right|_{V_{GS}} - R_c - R_{acc}$, is lower for the thin 30% virtual substrate than for the thick substrate at $V_{GS} - V_{th} \approx 0.55$ V. Also given in Table 1 are some of the MODFET performance parameters: the carrier mobility, μ, determined by Van der Pauw measurements, the maximum transconductance $g_{m_{max}}$ and the sub-threshold slope S, both at $V_{DS} = 50$ mV.

3. Low-frequency noise

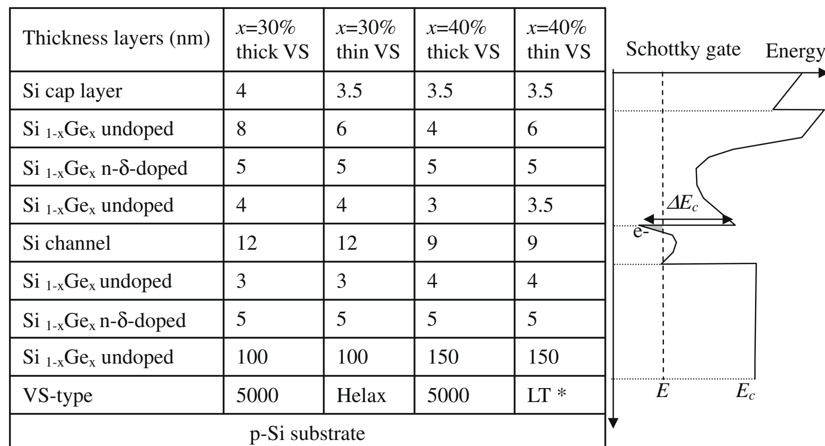
The low-frequency noise was measured using an electro-statically shielded probe station with 10-μm diameter tungsten probes under controlled pressure, in a frequency range from 1 Hz to 50 kHz at 300 K with the FETs in common source mode at source–drain bias $V_{DS} = 50$ mV in the linear region for all gate voltages, V_{GS}. The voltage fluctuations S_V from the load resistor R_L connected in series with the drain were analyzed by a SR770 FFT Spectrum Analyzer.

The spectral noise density of the short circuit drain current fluctuations, S_I, was calculated using: $S_I = S_V[(R_L + R_{SD})/(R_L R_{SD})]^2$, where R_{SD} is the drain-to-source differential resistance. All MODFETs showed $1/f^{\gamma}$ noise with $\gamma \approx 1$ below 1 kHz. At higher frequencies the contribution of the generation recombination (GR) noise was found for the majority of devices. An example of the normalised spectral noise density for two 30% devices at the same gate voltage overdrive $V_{GS} - V_{th} \approx 0.1$ V is given in Fig. 2. The traps responsible for the GR noise might reside in the Si channel or at some well defined distance from the channel. For example, traps may be located at delta-doped/un-doped interfaces at a distance of approximately 10 tunnelling lengths from the channel.

Fig. 3 gives the synopsis of the measurement results at $f = 10$ Hz. Other MODFETs on the same die with the same gate length but slightly different access regions (1 and 1.5 μm) were also measured and showed similar characteristics.

The noise contribution of channel and contacts can be separated using a fit to the experimental data based on the following equation:

$$\frac{S_I}{I^2} = \frac{S_{Rch}}{R_{ch}^2} \times \frac{R_{ch}^2}{(R_{ch} + R_c + R_{acc})^2} + \frac{S_{Rc}}{R_c^2} \times \frac{R_c^2}{(R_{ch} + R_c + R_{acc})^2} \quad (1)$$



Thickness layers (nm)	x=30% thick VS	x=30% thin VS	x=40% thick VS	x=40% thin VS
Si cap layer	4	3.5	3.5	3.5
Si $_{1-x}$Ge$_x$ undoped	8	6	4	6
Si $_{1-x}$Ge$_x$ n-δ-doped	5	5	5	5
Si $_{1-x}$Ge$_x$ undoped	4	4	3	3.5
Si channel	12	12	9	9
Si $_{1-x}$Ge$_x$ undoped	3	3	4	4
Si $_{1-x}$Ge$_x$ n-δ-doped	5	5	5	5
Si $_{1-x}$Ge$_x$ undoped	100	100	150	150
VS-type	5000	Helax	5000	LT *
p-Si substrate				

Fig. 1. Left: the layer structures for the four different Schottky-gated MODFETs. Right: the schematic conduction band diagram. Grey area is the channel region filled with free electrons. ΔE_c is the conduction band offset between s-Si channel and surrounding SiGe layers. LT* is the low-temperature LEPECVD grown thin VS.

Table 1
The contact resistance R_c, FET access resistance R_{acc} and channel resistance R_{ch} at $V_{GS}-V_{th}\approx 0.55$ V. The carrier mobility, μ, the maximum transconductance $g_{m_{max}}$ and the sub-threshold slope S, both at V_{DS} = 50 mV.

	x = 30%		x = 40%	
	Thick VS	Thin VS	Thick VS	Thin VS
R_{acc} (Ω)	56.4	54.8	59.4	43.6
R_c (Ω)	5.2	5.9	3.0	9.0
R_{ch} (Ω)	26.5	16.8	34.0	34.4
μ (cm^{2}V^{-1}s^{-1})	1405	1627	1254	1303
$g_{m_{max}}$(S)	2.9×10^{-4}	2.8×10^{-4}	2.7×10^{-4}	2.3×10^{-4}
S (mV/dec)	104	104	90	140

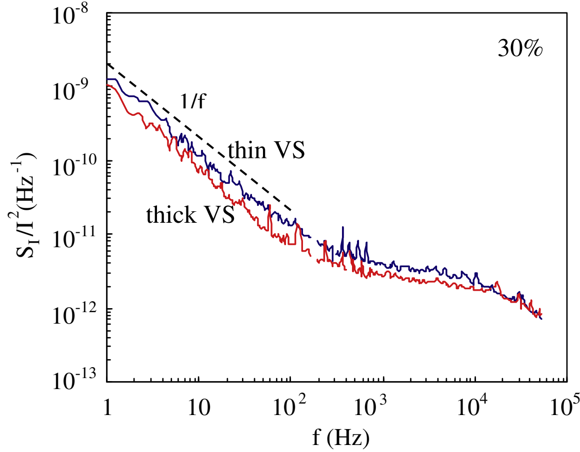


Fig. 2. The normalised spectral noise density as a function of frequency for two 30% devices at the same gate voltage overdrive $V_{GS}-V_{th}\approx 0.1$ V. The dashed line is the theoretical $1/f$ line.

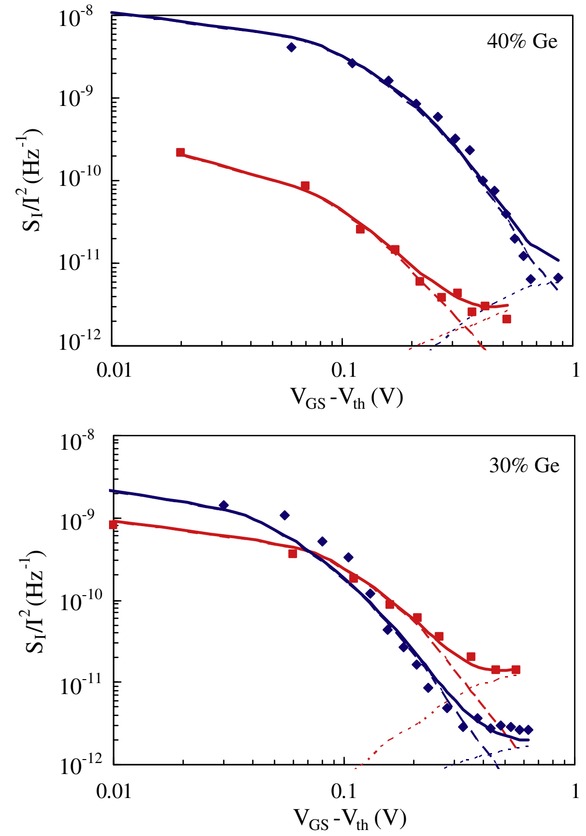


Fig. 3. The normalised spectral current noise density as a function of gate voltage overdrive, $V_{GS}-V_{th}$. Top graph for x = 0.4 and bottom graph for x = 0.3. Diamonds and squares are the measured data, diamonds for thin VS and squares for thick VS. The lines are the fit to the data by Eq. (1). Bold line: total fitted noise, dashed line: channel noise contribution, dotted line: contact noise contribution.

where $\frac{S_{Rc}}{R_c^2}$ is the spectral noise density of the contact resistance, independent of gate voltage overdrive, $\frac{S_{Rch}}{R_{ch}^2}$ is the spectral noise density of the channel resistance fluctuations. Based on the McWhorter model of the 1/f noise in MOSFETs $\frac{S_{Rch}}{R_{ch}^2}\propto\frac{1}{n^2}$ where n is the electron concentration in the channel [10]:

$$n=\frac{C_g\eta kT}{q^2}\ln\left\{1+\exp\left(\frac{q(V_{GS}-V_{th})}{\eta kT}\right)\right\}, \quad (2)$$

In Eq. (2), C_g is the gate capacitance given for HEMT structures by $C_g=\frac{\varepsilon_0\varepsilon(x)}{t_{ins}+\Delta d}$ with x the Ge concentration, $\Delta d\approx 9$ nm the correction factor following [11], $\varepsilon(x)$ is the dielectric constant of relaxed SiGe – calculated based on linear interpolation between the value for Si and Ge, and t_{ins} is the total thickness of Si/SiGe layers on top of the s-Si quantum well channel. The assumption is that the delta doped layer is depleted of mobile carriers due to electron transfer to the quantum well. η is the quality factor used to improve the fit in weak inversion ($3\leqslant\eta\leqslant4$). Eq. (2) describes the gate voltage dependence of the carrier concentration both below and above threshold.

The measured normalised current noise S_I/I^2 is fitted to Eq. (1) and the result is given in Fig. 3. The dashed line is the contribution of the channel noise, given by the first term of the right hand side of Eq. (1). The dotted line is the contribution of the access noise, given by the second term of the right hand side of Eq. (1). The bold line is the sum of the dashed and dotted line and thus gives the fit to the measured data. Fig. 3 shows that the fits to the data are in good agreement. The noise contribution of the access resistance in the thick VS samples overwhelms the channel noise at large gate voltage overdrive. This is possibly due to aging of the surface of the access region or the older fabrication process used for these structures.

In order to estimate the Hooge parameter [12], α_H for the gated part of the structure and the trap density, N_t only the channel noise has to be taken into account. The Hooge parameter α_H can be extracted from $\frac{S_{Rch}}{R_{ch}^2}=\frac{\alpha_H}{f\,n}$ with f the frequency (f = 10 Hz) and n given by Eq. (2). Thus the Hooge parameter varies as $(V_{GS}-V_{th})^{-1}$ in strong inversion. For the thick VS devices and the thin VS Helax devices, the Hooge parameter was found to be $\alpha_H=10^{-4}$–10^{-3} for $V_{GS}-V_{th}$ = 0.2 V. For the thin 40% VS device, the Hooge parameter was an order of magnitude larger ($\alpha_H\approx10^{-2}$).

Since the spectral noise density follows a $(V_{GS}-V_{th})^{-2}$ slope, the trap density, N_t can be assumed to be homogeneously distributed in energy and can be derived from [13]:

$$\frac{S_{Rch}}{R_{ch}^2}=\frac{\lambda(x)\times k\times T\times N_t}{f\times W\times L_g\times n^2} \quad (3)$$

with k the Boltzmann constant, T the temperature in K, f the frequency, W and L_g, respectively, the gate width and length, n given by Eq. (2) and $\lambda(x)=\frac{h}{4\pi\sqrt{2m_e(x)\Delta E_c(x)}}$ the tunnelling length in $Si_{1-x}Ge_x$. h is Planck's constant, $m_e(x)$ is the Ge concentration dependent electron effective mass and $\Delta E_c\approx0.6\times x$ (eV) is the potential barrier for electrons between the s-Si quantum well channel and the surrounding relaxed SiGe layers. The Ge dependent tunnelling lengths are $\lambda(0.4)=4.4\times10^{-8}$ cm and $\lambda(0.3)=4.9\times10^{-8}$ cm. Eq. (3) is typically used to derive the trap density in oxide-gated FETs. The value of λ for tunnelling into the oxide is approximately 10^{-8} cm. In MODFETs, however, no oxide is present and carrier tunnelling is into the surrounding relaxed SiGe layers. The Ge dependent tunnelling length is found to be four times larger than into oxide as a consequence of

Table 2
The trap density as a function of Ge concentration in the virtual substrate for n-channel s-Si MODFETs and MOSFETs.

Ge%	$N_t(E_{fn})$ (cm^{-3} eV^{-1}) s-Si Schottky-gated MODFET on thick VS (this work)	$N_t(E_{fn})$ (cm^{-3} eV^{-1}) s-Si Schottky-gated MODFET on thin VS (this work)	$N_t(E_{fn})$ (cm^{-3} eV^{-1}) Other work on s-Si MOSFETs (except [5] – MOSMODFET)
0			2×10^{17} [4], 3–12 $\times 10^{16}$ [7], 10^{17} [15]
15			2×10^{17} [4]
20			2×10^{18} [4], 9×10^{17} [14], 3–12 $\times 10^{16}$ [7]
25			2×10^{18} [4]
30	6×10^{16}	4×10^{16}	2.3×10^{18} [4], 1.4×10^{19} [5]
40	2×10^{16}	1×10^{18}	

the lower barrier height presented by the SiGe layers. The trap density N_t extracted from Eq. (3) and the Ge dependent tunnelling length is given in Table 2 and compared to values found in other work.

It is found that the trap density of the thick VS samples is very low, comparable to the lowest values reported in Si technology. The trap density of the 30% and 40% thick VS device are of the same order of magnitude. Indicative that with the lack of oxides on SiGe layers, there is no noise degradation with increased Ge concentration. The trap density of the thin Helax VS devices is also of the same order of magnitude as the thick VS devices, indicating that the He^+ implantation process gives good quality SiGe VS. On the other hand, the trap density in the thin LEPECVD grown 40% VS increases almost 2 orders of magnitude, indicative of a poorer quality virtual substrate.

4. Conclusions

The trap density in Schottky-gated s-Si MODFETs on traditional thick virtual substrates is found to be lower than for their oxide gated equivalents. In contrast to oxide gated s-Si MOSFETs, where the trap density increases with Ge concentration, the trap density in Schottky-gated MODFETs does not degrade with Ge concentration but is determined by the MBE grown material quality. In Schottky-gated MODFETs, the trap density is sensitive to the virtual substrate preparation. Thin LEPECVD virtual substrates show increased trap densities. For the Helax virtual substrate, however, no increase in trap density is seen and thus this technology is promising for s-Si devices on thin virtual substrates.

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