Power-Extraction Circuits for Piezoelectric Energy Harvesters in Miniature and Low-Power Applications

James Dicken, Paul D. Mitcheson, *Senior Member, IEEE*, Ivan Stoianov, and Eric M. Yeatman, *Senior Member, IEEE*

***Abstract*—When a piezoelectric energy harvester is connected to a simple load circuit, the damping force which the piezoelectric element is able to generate is often below the optimal value to maximize electrical power generation. Circuits that aim to increase the power output of a piezoelectric energy harvester do so by modifying the voltage onto which the piezoelectric current source drives its charge. This paper presents a systematic analysis and comparison of all the principal types of power extraction circuit that allow this damping force to be increased, under both ideal and realistic constraints. Particular emphasis is placed on low-amplitude operation. A circuit called single-supply prebiasing is shown to harvest more power than previous approaches. Most of the analyzed circuits able to increase the power output do so by synchronously inverting or charging the piezoelectric capacitance through an inductor. For inductor Q factors greater than around only 2, the single-supply prebiasing circuit has the highest power density of the analyzed circuits. The absence of diodes in conduction paths, achievable with a minimum number of synchronous rectifiers, means that the input excitation amplitude is not required to overcome a minimum value before power can be extracted, making it particularly suitable for microscale applications or those with a wide variation in amplitude.**

***Index Terms*—Energy conversion, energy harvesting, piezoelectric, transducers, vibration-to-electric energy conversion.**

I. Introduction

INERTIAL energy harvesters turn the mechanical motion of a proof mass into electrical energy in order to power a load circuit. There are three main transduction methods for converting the mechanical work into electrical energy: electromagnetic, electrostatic, and piezoelectric. The electromagnetic approach, as commonly used in conventional energy generation schemes, has been implemented at miniature and microscales for energy harvesting devices by utilizing finely wound or printed coils and permanent magnets. These devices have been successful particularly at the centimeter scale and above [1], [2]. The electrostatic force has been implemented using moving-plate capacitors primed with an external source such as a battery [3], or primed with an electret [4], [5]. Piezoelectric devices include centrally loaded beams [6], and cantilevers [7].

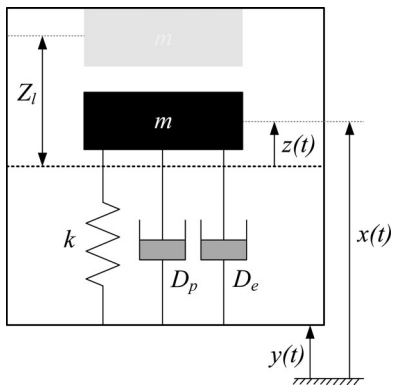

Fig. 1. Inertial energy harvester with parasitic damping and displacement-constrained travel.

For the inertial energy harvester device shown in Fig. 1 to operate optimally (i.e., with maximum possible power density), the damping force presented by the transducer must be optimized [8]. As an example, when operating the generator at resonance, the electrical damping force D_e should be made equal to the parasitic (mechanical) damping force D_p, or to a level which just limits the travel range of the proof mass to $\pm Z_l$ (the maximum displacement amplitude in which the mass may travel before hitting the end stops), whichever is the greater. Under many operating conditions and transducer designs, the required damping forces cannot readily be reached using conventional load circuits (resistors or bridge rectifiers) connected to piezoelectric transducers. This is primarily because of the modest electromechanical coupling coefficients achievable [9], [10].

If the amplitude Y_o of the external displacement is small compared to the internal travel range of the mass Z_l, then the system can operate with a high Q before the end stop limits are reached. In such cases, if the parasitic damping is low, high Q operation will maximize power output, and this will require low electrical damping; consequently, a high piezoelectric coupling coefficient is not required. However, these conditions are generally found only for high-frequency applications, and it is increasingly recognized that most practical applications of energy harvesters provide vibration at modest frequencies, in the range 1–100 Hz. Low-amplitude displacement operation also presents a practical

Manuscript received September 16, 2011; revised December 24, 2011; and February 8, 2012; accepted March 12, 2012. Date of current version June 20, 2012. This work was supported in part by the Engineering and Physical Sciences Research Council (EPSRC) under Grant EP/G070180/1 [Next Generation Energy-Harvesting Electronics: Holistic Approach (website: www.holistic.ecs.soton.ac.uk)] and by the EPSRC Project EP/E003192/1 [Delivering sustainable water systems by optimizing existing infrastructure via improved knowledge, understanding and technology (project NEPTUNE)]. Recommended for publication by Associate Editor Prof. T.-J. P. Liang.

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Digital Object Identifier 10.1109/TPEL.2012.2192291

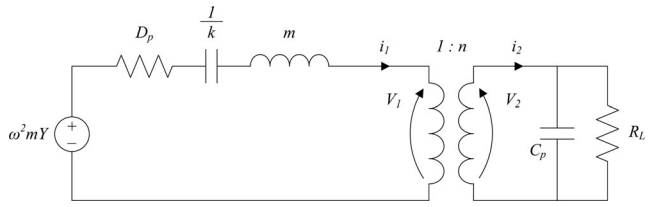

Fig. 2. Microgenerator with piezoelectric transduction.

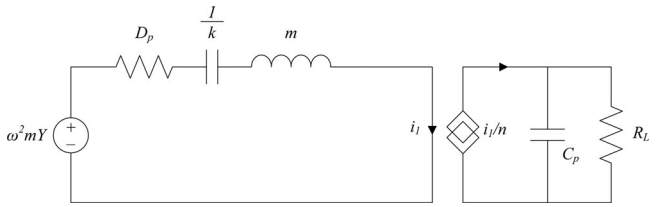

Fig. 3. Microgenerator equivalent circuit with low electromechanical coupling.

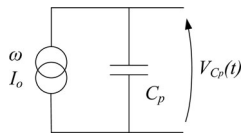

Fig. 4. Simplified piezoelectric model. The open-circuit amplitude of $V_{C_p}(t)$ is V_{po}.

limitation in some circuits in that the open-circuit voltage must be large enough to overcome the diode on-state voltage drops.

Whatever electrical damping is realized results from providing real power to the electrical load connected to the transducer. If a simple resistive or rectifying load is used, the maximum damping for a piezoelectric device is small, as stated earlier. However, various load circuits have been proposed and demonstrated which can overcome this limit. All essentially function by placing additional charge on the piezoelectric element in a synchronous fashion, which acts to increase the force the transducer presents to the mechanical system. In this paper, we review and compare these circuits in terms of the power densities that can be achieved under both ideal and realistic constraints, and identify which provide the best performance under specific conditions. We also discuss a circuit that has the potential to perform best over all operating conditions called single-supply prebiasing, the purpose of which is to avoid the need for the open-circuit voltage to overcome diode drops by using a minimal number of synchronous rectifiers. This allows effective operation of an energy harvester even for low-amplitude input vibrations. A general review of energy harvesting power conditioning circuits is given in [11].

All of the circuits are analyzed here within the same analytical framework to allow fair comparisons to be made between them. Where circuits have previously been investigated by others, the analysis is briefly repeated here, but with particular attention to such factors as the effect of diode drops for circuits with low piezoelectric output voltages. All of the derived closed-form solutions have been verified against *PSpice* time-domain simulations and the results agree within a few percent.

II. Modeling

The force presented by the piezoelectric transducer to the mechanical system is influenced by the impedance and operation of the electrical circuit that is connected to it. The transducer interface circuit can, therefore, be designed to allow modification of the damping force, and different types of circuit are capable of modifying the electrical damping by different amounts. A simple equivalent circuit model of a mass–spring–damper microgenerator damped by a piezoelectric element with a purely resistive load is shown in Fig. 2 [12].

In Fig. 2, the circuit on the primary side of the transformer represents the mechanical system (voltages correspond to forces and currents correspond to velocities [13]). The transformer represents the piezoelectric transduction mechanism and the secondary side circuit represents the electrical load and properties of the piezoelectric transducer, including its in-built capacitance C_p. In this case, an external load resistor is attached to the transducer. Due to the relatively low coupling coefficient of most piezoelectric materials, the transformer is a step-up device with a high turns ratio. This has the effect that the combined impedance of C_p and R_L, when referred to the primary side, is very low, so that V_1 is low and effectively a small mechanical force is presented by the load. Thus, the current in the primary side, corresponding to proof mass relative velocity $\dot{z}(t)$, is largely unaffected by connections made on the secondary side. The transformer can, therefore, be replaced with a current-controlled current source, and Fig. 2 redrawn as the circuit shown in Fig. 3.

Therefore, a piezoelectric energy harvester with a level of electromechanical coupling low enough that any level of damping from the electrical side makes negligible difference to the velocity of the proof mass can be simplified to the circuit of Fig. 4.

The task of the interface circuit is, therefore, to extract the maximum power from a sinusoidal current source with an inherent shunt capacitance. Where sophisticated circuits are able to overcome the low damping limitation described earlier, the approximation that I_o is unaffected by the electrical load will begin to break down. However, we will neglect this limitation in the analysis that follows, for purposes of simplicity and clarity. For a wide range of useful applications, the output power can be improved substantially by modified circuits before the change to I_o becomes significant. Furthermore, even where I_o is significantly reduced by the enhanced damping, the relative performance of the various circuits—all referenced to I_o—will be unaffected. A more detailed analysis of the full electromechanical coupling is provided in [14].

III. Analysis Methodology

Before discussing the candidate interface circuits, we must first place some bounds on the analysis that is to follow. The

TABLE I
COMPONENT PARAMETERS FOR HARVESTER CONFIGURATIONS

Config.	Vol.	R_s	L	C_p	$V_{D_{on}}$
1	1 cm^3	0.47 Ω	470 μH	65 nF	0.5 V
2	3 cm^3	0.141 Ω	1.41 mH	585 nF	0.4 V
3	10 cm^3	47 mΩ	4.7 mH	6.5 μF	0.3 V

circuits analyzed have many degrees of freedom, including diode on-state voltage drop V_D, inductor Q factor (dependent on the series resistance, R_s), the on-state drain-to-source resistance of the MOSFETs $R_{\mathrm{DS_{on}}}$, the size of the piezoelectric element, and the mechanical excitation amplitude and frequency of the harvester. Typically the power generated in the piezoelectric can be increased and the losses in the circuit reduced by allocating additional volume to each constituent part of the harvester system. As there is generally a constraint on total harvester volume, optimally choosing all of the component values within the volume constraint is a complex task. Fully optimizing the system in a holistic way across all of these variables for each candidate circuit is beyond the scope of this paper; however, sensible component values must be chosen to allow fair comparisons between the circuits to be made.

The power consumed by control circuitry has also not been considered. This control usually involves maxima/minima detection, gate drives and some simple timing, and so its power consumption is similar across the range of architectures studied. This will affect the relative performance of circuits with and without such a requirement, particularly at very low output power levels, although not the comparison of the circuits' performance in terms of the Q factor of their inductive current paths.

In the case that diode voltage drops are either negligible or ignored, it is found that the power output of each circuit can be normalized to a factor of ${I_o}^2/\omega C_p$ and written solely as a function of the Q factor of the current paths containing inductors. This allows a comparison between the performance of all circuits to be made which holds regardless of excitation characteristics and the volume of piezoelectric material used. However, when diode drops are taken into account, such normalization is not possible. For these comparisons, component values were taken from the best available off-the-shelf products at the time of writing for three chosen sizes of energy harvester. The configurations of harvester and component parameters used are summarized in Table I. The on-state resistance of any switches is assumed negligible compared to the series resistances of inductors, and the parasitic capacitance is negligible compared to C_p, which is realistic for existing off-the-shelf parts.

The inductors were chosen from a range of products available to maximize the Q factor of the current paths in each given volume, and the diodes are Schottky diodes.

Of the various circuits analyzed, some have the capability to push energy into a storage element such as a capacitor in order to provide a stable dc voltage for a load, while others provide a time-varying voltage. This important difference in functionality is taken into account when final comparisons of the circuits are made. The circuits will now be analyzed.

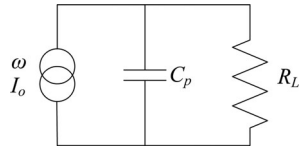

Fig. 5. Piezoelectric energy harvester connected to a purely resistive load.

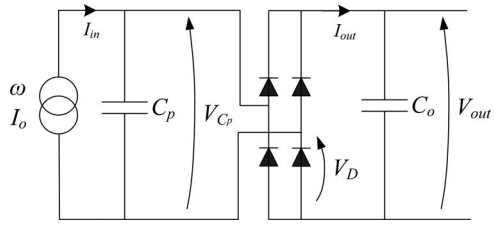

Fig. 6. Full-bridge rectifier with output smoothing capacitor.

IV. PURELY RESISTIVE LOAD

The simplest load that can extract real power from the piezoelectric transducer is a resistive load as shown in Fig. 5.

Under excitation by a sinusoidal current source with a magnitude I_o, a resistive load of magnitude R_L will dissipate a power P_{R_L}, given by

$$P_{R_L} = \frac{1}{2}\left(\frac{{I_o}^2 R_L}{1 + {R_L}^2 \omega^2 {C_p}^2}\right). \tag{1}$$

At the optimal load resistance of $1/\omega C_p$, the circuit has a maximum power output of

$$P_{\mathrm{ORL}} = \frac{1}{4}\left(\frac{{I_o}^2}{\omega C_p}\right). \tag{2}$$

This value of P_{ORL} will be used as a base case for comparison with the other circuits.

V. TUNED-OUT SHUNT CAPACITANCE

An obvious approach to extract the maximum power from the current source in Fig. 4 is to add a shunt inductor to tune out the piezoelectric capacitance. However, this option is not realistically achievable because of the very large inductor values required. For example, in an energy harvesting application with a typical vibration frequency of 100 Hz, and a piezoelectric capacitance of 100 nF, the required resonant inductor would be about 25 H. Consequently, this option cannot be exploited in practice, and is not considered further here.

VI. RECTIFIED DC LOAD

A more useful output circuit for piezoelectric microgenerators is a standard bridge rectifier with a smoothing capacitor (see Fig. 6). The circuit's application in energy harvesting was originally analyzed in [15] where the diodes were assumed to be ideal. Here, we analyze the circuit as having diodes with a fixed on-state voltage drop V_D. This circuit provides useful additional functionality over the circuit in Fig. 5 as almost all electronic loads require a dc input. The output capacitance C_o will typically be much larger than the piezoelectric capacitance C_p, and

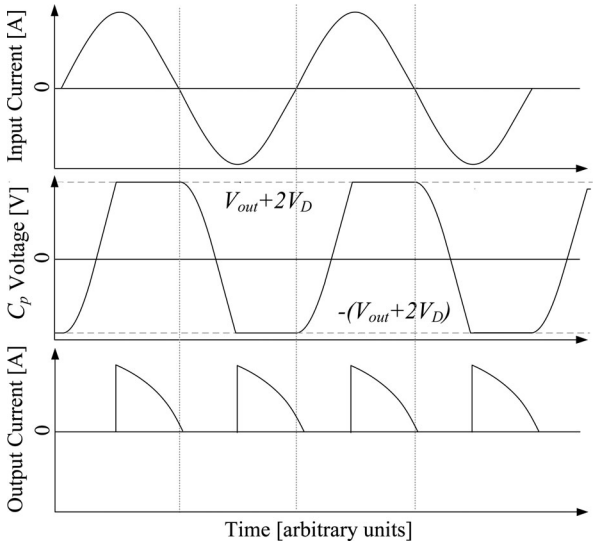

Fig. 7. Input current, piezoelectric voltage, and output current in the presence of a bridge rectifier with a fixed output voltage $V_{\rm out}$.

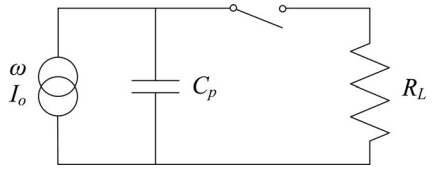

Fig. 8. Synchronous switched extraction circuit.

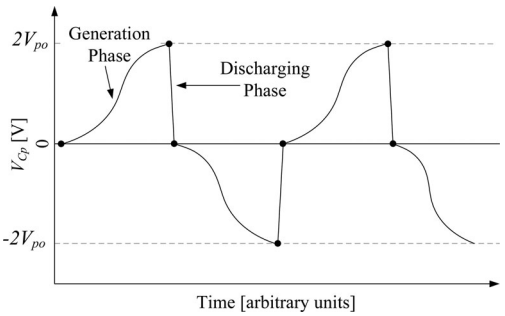

Fig. 9. Voltage waveform on the piezoelectric capacitance C_p for the circuit of Fig. 8. The discharge phase is shown as near-instantaneous; in practice this is subject to an *RC* time constant if the load is purely resistive.

so its voltage can be approximated as constant over a cycle. The current waveform $I_{\rm out}$ will be discontinuous, and only nonzero when the magnitude of the voltage on the piezoelectric capacitance V_{C_p} exceeds $V_{\rm out}+2V_D$. The voltage waveform on the piezoelectric capacitance in relation to the piezoelectric current source is shown in Fig. 7.

It is useful to introduce a quantity V_{po} which is the open-circuit voltage magnitude of the piezoelectric capacitance as shown in Fig. 4. This is given by

$$V_{po} = \frac{I_o}{\omega C_p}. \tag{3}$$

By finding the angle at which conduction into the output stage begins, the power output of the circuit as a function of the output voltage $V_{\rm out}$ can be determined:

$$P_{\rm out} = \frac{2}{\pi} I_o V_{\rm out} \left[1 - \frac{V_{\rm out}+2V_D}{V_{po}}\right]. \tag{4}$$

For which the optimal output voltage is

$$V_{\rm out_{opt}} = \frac{1}{2}(V_{po} - 2V_D). \tag{5}$$

The maximum power is then found by substituting (5) into (4), as follows:

$$P_{\max} = \frac{(I_o - 2V_D\omega C_p)^2}{2\pi\omega C_p} = \frac{1}{2\pi}\left(1 - \frac{2V_D}{V_{po}}\right)^2 \left(\frac{{I_o}^2}{\omega C_p}\right). \tag{6}$$

Unless the diodes are replaced with synchronous rectifiers, the circuit only produces power if the change in voltage due to the current source is high enough to cause current to flow to the output stage, that is $V_{po} > V_{\rm out}+2V_D$. Therefore, to extract power from the circuit at all if $V_{\rm out} \to 0$ we require that:

$$V_{po} > 2V_D. \tag{7}$$

In the ideal case that the diode drop is negligible, the power output simplifies to $P_{\max} = {I_o}^2/2\pi\omega C_p$, which is less than the optimal resistive load case ($P_{\rm ORL}$) by

$$\frac{P_{\rm RECTDC}}{P_{\rm ORL}} = \frac{2}{\pi} \approx 0.64. \tag{8}$$

Clearly, when the diode drops are included, this ratio is even lower. Thus, while this circuit is more useful than the optimal resistive load, there is a tradeoff in that less power can be converted.

VII. Synchronous Switched Extraction

A third circuit, originally proposed by Shenck [16], and reviewed in more detail in [17], is shown in Fig. 8. Instead of a direct connection, the resistive load is connected via a switch that closes when the voltage on the capacitor is maximal in either polarity (i.e., at the zero crossings of the current source). At that instant, all the energy on the capacitor is transferred to the load, and the process is repeated in the negative half-cycle as shown in Fig. 9. Note that in this circuit the switch must be capable of conducting and blocking in both directions and, therefore, cannot be a single MOSFET. However, the effect could be achieved with a pair of series MOSFETs with suitable gate drives. We assume from now on that all switches have this capability, and hence model them as perfect switches.

A sinusoidal current source of amplitude I_o and frequency ω produces a charge per half-cycle $Q_{\frac{1}{2}} = 2I_o/\omega$. This charge, placed on C_p, has an energy:

$$E = \frac{1}{2}\frac{Q^2}{C_p} = \frac{2}{C_p}\left(\frac{I_o}{\omega}\right)^2. \tag{9}$$

Therefore, the power dissipated in a resistive load R_L is

$$P_{\max} = 2f\left(\frac{2{I_o}^2}{\omega^2 C_p}\right) = \frac{2}{\pi}\left(\frac{{I_o}^2}{\omega C_p}\right). \tag{10}$$

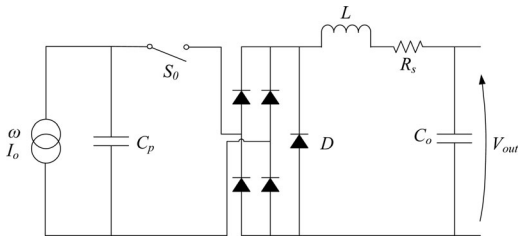

Fig. 10. Circuit for synchronous switched extraction with dc output.

Compared to the base-case optimal resistive load circuit of Fig. 5 this represents an improvement in power generation, for a modest increase in complexity, by a simple ratio of

$$\frac{P_{\mathrm{SSE}}}{P_{\mathrm{ORL}}} = \frac{8}{\pi} \approx 2.55. \tag{11}$$

VIII. Synchronous Switched Extraction With DC Output and Efficient Energy Transfer

As we have seen from the circuit in Fig. 8, there is an advantage of a factor of 2.55 over the optimal resistive load case when extracting energy from the circuit at zero crossings of the current source. As previously discussed, a dc output is required to power a typical electronic load. A new synchronous switched circuit can, therefore, be proposed (see Fig. 10) with a rectifier and smoothing capacitor, which aims to achieve the same energy gain of 2.55 and provide a dc output. The output stage in this case is the output filter of a buck switch-mode power supply, which allows energy to be transferred efficiently from C_p to the output capacitor C_o, which again behaves as a constant-voltage source.

A. Optimal Energy Transfer

In any circuit that transfers energy between a capacitor and a voltage source through an inductor, such as the $C_p \rightarrow S_0 \rightarrow L \rightarrow C_o$ current path of Fig. 10 (with C_o being modeled as a voltage source), there can be one or two parts to the energy transfer process. The first part is the transfer of energy through the path between the capacitor, inductor, and voltage source, and the second part is when the capacitor is fully discharged and the inductor current then freewheels (in this case though D). If the value of the voltage source (given the initial voltage on the capacitor) is carefully chosen, all the energy will have been removed from the capacitor at the same point as the inductor current falls to zero, meaning the freewheeling stage does not occur. If the current path resistance is zero, then the initial voltage on the capacitor, $V_{C_p}(0)$, must be exactly twice the value of the voltage source in order for it to fully discharge. If the voltage on the capacitor is higher than this, then freewheeling will occur. If it is lower then a voltage will remain on the capacitor (approximately $2V_{\mathrm{out}} - V_{C_p}(0)$) when the current has dropped to zero.

It can be shown that in the presence of losses, maximum energy is delivered to the voltage source if the voltages are such that the circuit operates at the limit of the onset of freewheeling, and this is the strategy chosen for the circuits analyzed here.

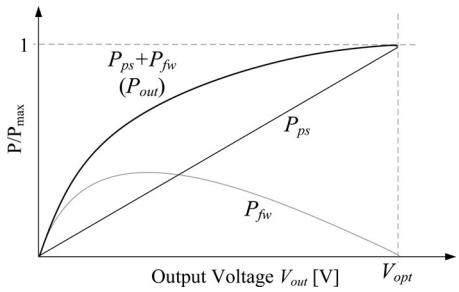

Fig. 11. Contributions to power output from freewheeling and direct conduction, and their sum, as a function of output voltage, for the circuit of Fig. 10. At $V_{\mathrm{out}} = V_{\mathrm{opt}}$ the contribution from freewheeling is zero.

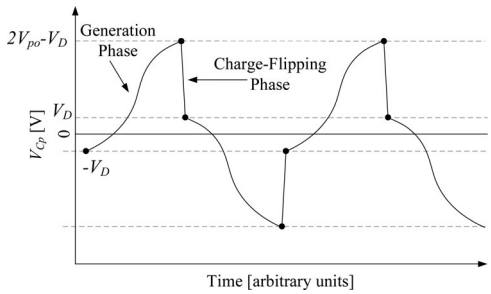

Fig. 12. Voltage waveform on the piezoelectric capacitance.

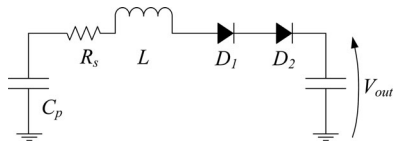

Fig. 13. Resonant current path for charge extraction.

Fig. 11 shows the results of a simulation of the normalized output power versus V_{out}, and the contributions to this power from freewheeling and direct conduction.

B. Detailed Analysis of Synchronous Switched Extraction

The circuit of Fig. 10 will now be analyzed. At the start of the cycle (shown in Fig. 12), the current source drives charge into the capacitor with switch S_0 open. As in the previous synchronous extraction case, S_0 is closed at the point when the voltage on C_p is at its maximum. This causes current to flow through the full-bridge rectifier and inductor to the output capacitor. If the circuit is operating on the limit of freewheeling occurring, the voltage on C_p will be clamped at V_D at the end of the extraction process. It is worth noting that were D not present, the voltage after energy extraction would instead be $2V_D$.

The inductor is modeled as having inductance L with series resistance R_s, and the capacitors are assumed to be free of leakage. It is also again assumed that the output voltage is constant and is, thus, modeled as a voltage source. The main current path is a series *RLC* circuit with two diodes as shown in Fig. 13.

The Q factor of the current path is unaffected by the diodes, which are assumed to have a constant on-state voltage drop,

giving

$$Q = \frac{1}{R_s}\sqrt{\frac{L}{C_p}}. \tag{12}$$

The damped resonant frequency of the path is

$$\omega_n = \sqrt{\frac{1}{LC_p} - \frac{{R_s}^2}{4L^2}}. \tag{13}$$

Given that D clamps C_p at V_D at the end of the charge-flipping phase, the voltage at the end of the piezoelectric generation phase is $2V_{po} - V_D$. The period for which the switch should be closed is half a cycle of the damped natural frequency ω_n (i.e., π/ω_n), the end of which coincides with a zero value of inductor current. The fraction of voltage conserved on the capacitor of an *RLC* oscillator with Q factor Q after one half-cycle of operation is

$$\gamma \approx e^{-\frac{\pi}{2Q}}. \tag{14}$$

Therefore, the final voltage on the piezoelectric capacitance C_p will be

$$V_{\text{final}} = (V_{\text{out}} + 2V_D) - \gamma\left[(2V_{po} - V_D) - (V_{\text{out}} + 2V_D)\right]. \tag{15}$$

As explained in Section VIII-A, in order to remove as much energy as possible from the piezoelectric capacitance, we require that in a resonant half-cycle, enough energy is removed from C_p to reduce the voltage to exactly V_D. This implies that (15) puts an upper bound on the value of V_{out} of

$$V_{\text{out}} \leq \frac{(2V_{po} - 3V_D)\gamma - V_D}{1+\gamma}. \tag{16}$$

If V_{out} is greater than this value, then it is impossible to extract all of the energy stored in C_p through the action of the resonant circuit. Assuming V_{out} is set exactly as per the limit of the inequality in (16), then the energy output from the circuit per half-cycle is

$$E_{\frac{1}{2}} = V_{\text{out}} C_p (2V_{po} - 2V_D). \tag{17}$$

By approximating γ as close to 1 and hence taking a truncated series expansion $\gamma = 1 - \pi/2Q$, and with V_{out} set to the maximum value permitted by (16), this expression multiplied by $2f$ gives the power output from the circuit:

$$P_{\text{out}} \approx \frac{2}{\pi}\left(\frac{{I_o}^2}{\omega C_p}\right)\left[\left(1 - \frac{\pi}{4Q}\right) - 3\frac{V_D}{V_{po}}\left(1 - \frac{\pi}{6Q}\right) + 2\left(\frac{V_D}{V_{po}}\right)^2\left(1 - \frac{\pi}{8Q}\right)\right]. \tag{18}$$

This expression indicates clearly the loss of power from two factors—the finite Q of the inductor and the diode voltage drop. If both factors are neglected, the output power is the same as the synchronous switched extraction into a resistive load of Fig. 8. Without neglecting losses, to obtain any power in the circuit of Fig. 10 we require that $V_{po} > V_D$.

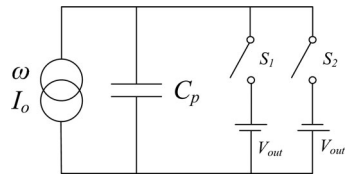

Fig. 14. Piezoelectric fixed voltage control.

IX. Piezoelectric Fixed Voltage Control

The circuits analyzed so far achieve different performance in terms of power output ultimately because the piezoelectric current source pushes charge into different average voltages. To maximize the energy generated, the circuit must, therefore, maximize this voltage. We can now see that it is intuitively reasonable that the rectifier circuit should perform the poorest, the directly connected resistor is better and the synchronous circuits perform the best. The rectifier circuit clamps the peak voltage on the piezoelectric capacitance so that the current source never operates into the maximum voltage, while the synchronous circuits maintain all of the charge on the piezoelectric capacitance until the voltage peaks.

Expanding this concept, various circuits have been developed that increase the output voltage into which the generated charge is supplied by adding charge to the device at suitable points in the motion cycle. All these circuits require synchronous switching of some type, and thus have some monitoring and control overhead. A simple example is shown in Fig. 14, which was originally introduced for applications in structural damping [18], where the inefficiencies due to a lack of inductors in current paths are not a concern. In this circuit, the generator is connected to one of the two output voltage sources continuously, by either S_1 or S_2, except for two very short periods per cycle when the current source has a zero crossing. At that moment, the polarity of V_{out} is near-instantaneously switched using S_1 and S_2 so that the current source is always charging a supply.

Since the charge produced by the generator during each half-cycle is $2I_o/\omega$, the energy supplied per cycle is $4V_{\text{out}}I_o/\omega$. However, each polarity reversal at the current zero crossings (corresponding to a displacement maximum) drains $2C_pV_{\text{out}}$ of charge from the supply, reducing the net energy gain per cycle by $4C_p{V_{\text{out}}}^2$. The value of V_{out} that optimizes the net power is $I_o/2\omega C_p$, giving a net average power of

$$P_{\max} = \frac{1}{\pi}\left(\frac{{I_o}^2}{\omega C_p}\right). \tag{19}$$

This is worse than the optimal resistive load by a factor of $2/\pi$.

Some improvement can be made by dividing the polarity reversal into two stages (see Fig. 15): discharge through an additional switch S_o, followed by charging to the opposite polarity. This reduces the lost energy by half, and doubles the net power and the optimal V_{out}. However, at $4/\pi$ times better than the optimal resistive load case, the output power is still low compared to the synchronous switched output circuits discussed earlier. To gain a power advantage over these previous synchronous circuits, it is necessary to apply the extra charge to the piezoelectric

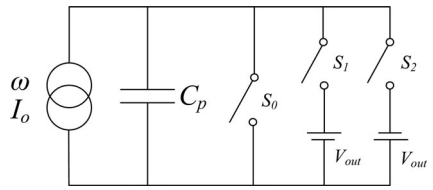

Fig. 15. Piezoelectric fixed voltage control (with charge canceling).

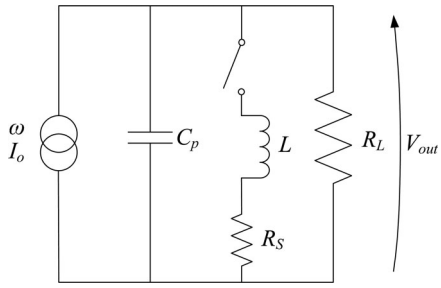

Fig. 16. SSHI with resistive load.

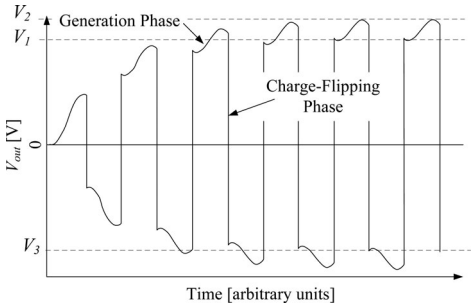

Fig. 17. Voltage waveform of SSHI showing build-up to the steady state.

device in as lossless a manner as possible, which is the purpose of the class of circuits described as follows.

X. Parallel SSHI With Resistive Load

The synchronous, switched harvesting with inductor (SSHI) technique reported by Guyomar *et al*. in [19] introduced the key advance of using a switched inductor to flip the charge on the capacitor twice per cycle. Since the extra charge does not have to be drawn from an external supply, the losses can be minimal—limited primarily by the finite Q of the path containing the inductor.

Fig. 16 shows an SSHI circuit with a resistive load, with the inductor losses occurring in R_s. The output voltage $V_{\rm out}$ is shown in Fig. 17. Gradually the energy stored in the capacitor C_p builds, increasing the voltage, until the power output increases to a point where the system reaches the steady state.

There are two phases of operation.

1) The generation phase, during which the current source charges C_p and the load resistor removes some charge. The voltage on C_p goes from $V_1 \rightarrow V_2$.
2) The charge-flipping phase, where the charge stored on C_p is flipped in magnitude through the inductor, and the voltage on C_p goes from $V_2 \rightarrow V_3$. This phase occurs over a very short time period.

After the system is started from rest the output magnitude gradually rises until the steady state is reached at $V_3 = -V_1$ as shown in Fig. 17.

A. Generation Phase $V_1 \Rightarrow V_2$

During the charging phase some energy is dissipated by the load R_L. The total charge passing through the load is

$$q_{R_L} = I_{R_L} t \approx \frac{V_1}{R_L}\frac{\pi}{\omega}. \tag{20}$$

The net charge supplied to C_p is then $2I_o/\omega - q_{R_L}$, and the change in voltage is simply this divided by C_p, giving

$$V_2 = V_1\left(1 - \frac{\pi}{\omega R_L C_p}\right) + 2V_{po}. \tag{21}$$

B. Charge-Flipping Phase $V_2 \Rightarrow V_3$

The charge-flipping phase will be much shorter than the generation phase so that the energy dissipated by the load resistor R_L during that time can be neglected. The switch is closed for a time π/ω_n [where ω_n is given in (13)], i.e., until the current in the inductor returns to zero. Using the definition of γ in (14) the voltage after flipping from a voltage V_2 is a function of the Q factor of the *RLC* circuit as follows:

$$V_3 = -V_2\gamma. \tag{22}$$

C. Steady State

Solving (21) and (22) for the case where $V_3 = -V_1$ yields an expression for the steady-state voltage $V_{1_{\rm ss}}$:

$$V_{1_{\rm ss}} = \frac{2V_{po}}{1/\gamma - 1 + \pi/\omega R_L C_p}. \tag{23}$$

Approximating the output power as ${V_{1_{\rm ss}}}^2/R_L$, the optimal load can be derived as follows:

$$R_{L_{\rm opt}} = \frac{\pi}{\omega C_p\,(1/\gamma - 1)}. \tag{24}$$

Using the approximation $\gamma \approx 1 - \pi/2Q$, the output power is

$$P_{\max} = \frac{\gamma}{\pi\,(1-\gamma)}\left(\frac{{I_o}^2}{\omega C_p}\right) \approx \frac{2Q}{\pi^2}\left(\frac{{I_o}^2}{\omega C_p}\right). \tag{25}$$

Compared to the optimal resistive load this is an improvement of

$$\frac{P_{P\_\rm SSHI\_RL}}{P_{\rm ORL}} = \frac{1}{\pi}\frac{\gamma}{1-\gamma} \approx \frac{8Q}{\pi^2}. \tag{26}$$

Thus even a modest Q provides a significant power gain. What is now needed is a method which realizes the benefits of this circuit but which also gives a dc output.

XI. Parallel SSHI With DC Output

Fortunately, the parallel SSHI circuit can be straightforwardly adapted for a constant dc output with the addition of rectification as shown in Fig. 18. This circuit was originally presented in [20], was analyzed in more detail in [21], and is analyzed here for consistency with our analytical framework. The rectifier and

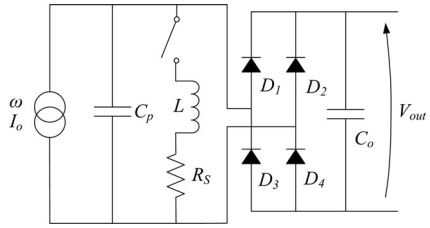

Fig. 18. Parallel SSHI with dc output.

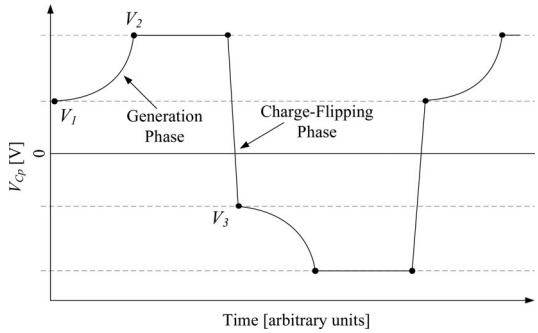

Fig. 19. Voltage waveform on the piezoelectric capacitance C_p for the circuit of Fig. 18.

output capacitor clamp the output voltage of the piezoelectric element to $\pm(V_{\rm out}+2V_D)$. As in the previous circuit, the switch is closed briefly at the zero crossings of the piezoelectric current to reverse the polarity on C_p. The voltage waveform on C_p is shown in Fig. 19.

As can be seen, the piezoelectric voltage is clamped at a maximum of V_2. After charge flipping this gives $V_3=-\gamma V_2$, which in steady state equals $-V_1$ so that $V_1=\gamma V_2$. To bring the voltage back to the clamped level in order to deliver charge to the output, some charge must be placed on C_p to compensate for the inefficiency in the flipping process. Thus

$$V_2-\gamma V_2=\frac{1}{C_p}\int_0^{\tau} I_o\sin(\omega t)dt \tag{27}$$

where τ is the time to reach the clamped voltage. From (27) we can obtain

$$\cos(\omega\tau)=1-\frac{V_2}{V_{po}}(1-\gamma). \tag{28}$$

The energy supplied to the output per half-cycle is

$$\begin{aligned}E_{\frac{1}{2}}&=I_oV_{\rm out}\int_{\tau}^{\pi/\omega}\sin(\omega t)dt\\&=C_pV_{po}V_{\rm out}\left[2-\frac{(1-\gamma)(V_{\rm out}+2V_D)}{V_{po}}\right].\end{aligned} \tag{29}$$

This energy is maximized for an output voltage of

$$V_{\rm out}=\frac{V_{po}}{1-\gamma}-V_D \tag{30}$$

for which the output power is given by

$$P_{\max}\approx\left[1-\frac{\pi}{2Q}\frac{V_D}{V_{po}}\right]^2\left(\frac{2Q}{\pi^2}\right)\left(\frac{{I_o}^2}{\omega C_p}\right). \tag{31}$$

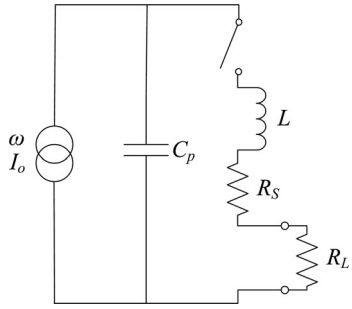

Fig. 20. Series SSHI with resistive load.

This equation shows a key advantage of the circuit, which is that the open-circuit output voltage V_{po} does not need to exceed the diode drop voltages, the minimum instead being V_D times $\pi/2Q$. If V_{po} is substantially greater than this minimum, so that the first factor in (31) can be neglected, then the output power is $8Q/\pi^2$ times higher than in the optimal resistive load case. For the high-Q case, where the diode drop can be neglected and $\gamma\approx 1-\pi/2Q$, the optimum output voltage $V_{\rm out}\approx(2Q/\pi)V_{po}$. Since a sinusoidal current source of amplitude I_o supplies an average current (when rectified) of $2I_o/\pi$, this implies an average power from the source of

$$P_{\rm source}\approx V_{\rm out}(2I_o/\pi)\approx\frac{4Q}{\pi^2}\left(\frac{{I_o}^2}{\omega C_p}\right). \tag{32}$$

Since the power supplied to the output is half this level, clearly the optimized circuit is 50% efficient, as would be expected from an impedance-matched source-load pair.

XII. Series SSHI With Resistive Load

An alternative implementation of the synchronous switched harvester is to place the switching inductor in series with the load, as shown in Fig. 20. This circuit was reported in [22], and analyzed again in [23] in the context of structural damping.

Again, the switch is briefly closed at the maxima of displacement to reverse the polarity of the voltage on C_p, but in this case power is only extracted into the load during this charge-flipping phase. The waveform on C_p will be the same as in Fig. 17, with a transient period until a steady state is reached. The loss of voltage due to dissipation in the charge reversal equals the voltage increase provided by the source, as was the case in the previous charge-flipping circuits.

For this circuit, during the generation phase current is only supplied to C_p, not to the load, so that (using the previous notation) $V_2(1-\gamma')=2V_{po}$. Here, γ' is the efficiency of the *RLC* circuit as before, but where the Q of the charge-flipping circuit now includes the load resistance R_L, i.e., $\gamma'=e^{\pi/2Q'}$ and

$$Q'=\frac{1}{R_s+R_L}\sqrt{\frac{L}{C_p}}. \tag{33}$$

The energy dissipated in the two resistors is therefore

$$E_{\rm loss}=\frac{1}{2}C_p{V_2}^2-\frac{1}{2}C_p{V_1}^2=\frac{1}{2}C_p(2V_{po})^2\frac{1+\gamma'}{1-\gamma'} \tag{34}$$

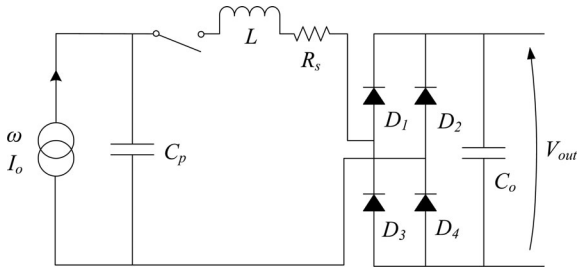

Fig. 21. Series SSHI with rectified dc load.

$$\approx \frac{8Q'}{\pi} C_p {V_{po}}^2. \tag{35}$$

This energy will divide between the two resistors in proportion to their magnitude since both conduct the same current, so the load energy per half-cycle is

$$E_{\frac{1}{2}} \approx \left(\frac{R_L}{R_L + R_s}\right)\left(\frac{8Q'}{\pi}\right) C_p {V_{po}}^2. \tag{36}$$

It is straightforward to show that this is maximized for $R_L = R_s$, for which $Q' = Q/2$, giving a maximum power of

$$P_{\max} = \frac{\omega}{\pi} E_{\frac{1}{2}} = \frac{2Q}{\pi^2}\left(\frac{{I_o}^2}{\omega C_p}\right) \tag{37}$$

which is the same as in the parallel SSHI case of Fig. 16.

XIII. Series SSHI With DC Output

The series SSHI circuit can also be adapted for a fixed dc output by adding rectification, as shown in Fig. 21. In this circuit, proposed by Lefeuvre *et al*. [24], the charge flipping and energy extraction again occur simultaneously. Another variation presented in [25] and [26] uses a transformer instead of an inductor to decrease the effective on-state voltage drop of the diodes. It is also possible to modify the output voltage by the addition of an additional flyback output stage as described in [27]. This allows the first capacitor to remain at the optimal voltage for operation of the SSHI technique, while giving a chosen output voltage, and this does not modify the upper limit on output power for this circuit. A further study of the switching duty cycle required to maintain an optimal voltage on the storage capacitor is presented in [28].

When the switch is closed, charge flows through either D_1 and D_4 or D_2 and D_3, and the output capacitor C_o, being in series with these, has charge added to it at a voltage $V_{\rm out}$. We assume C_o is large enough so that $V_{\rm out}$ does not vary during charge flipping.

The waveform on C_p for this circuit (see Fig. 22) has the same form as in the previous cases. We define V_1 as the voltage at the beginning of the generation phase, with $V_1 + 2V_{po}$ the voltage just before charge flipping. At this point the voltage across the inductor is the difference between $V_1 + 2V_{po}$ and $V_{\rm out} + 2V_D$ and it is this voltage whose polarity is reversed, with an efficiency γ, so that the voltage V_2 after flipping is

$$V_2 = (V_{\rm out} + 2V_D) - \gamma\left((V_1 + 2V_{po}) - (V_{\rm out} + 2V_D)\right). \tag{38}$$

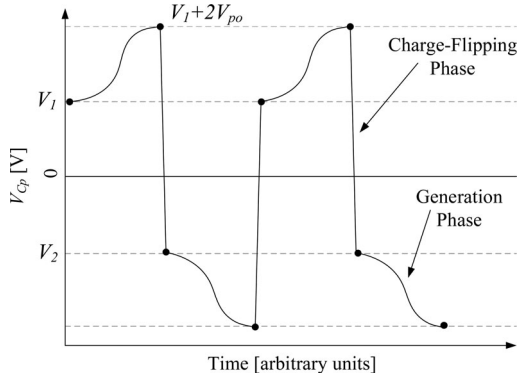

Fig. 22. Steady-state operating cycle of series SSHI circuit.

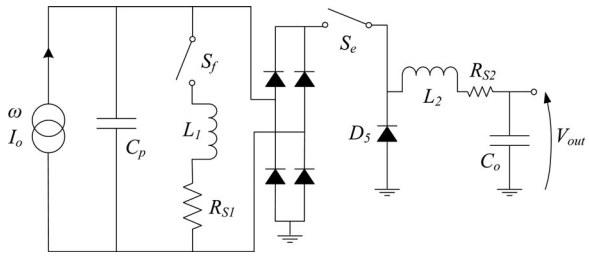

Fig. 23. Parallel SSHI circuit with synchronous extraction.

The steady-state value of V_1 is found by setting $V_2 = -V_1$:

$$V_{1_{\rm SS}} = \frac{2V_{po}}{1-\gamma} - (V_{\rm out} + 2V_D)\left(\frac{1+\gamma}{1-\gamma}\right). \tag{39}$$

While it appears from (39) that $V_{1_{\rm SS}}$ can be negative, the need for $V_1 + 2V_{po}$ to be greater than $V_{\rm out} + 2V_D$ introduces the simple requirement that the open-circuit piezoelectric voltage V_{po} must be greater than $2V_D$ for the circuit to function. This requirement can be a significant limitation for energy harvesting applications where the motion amplitude is low.

The energy added to the output capacitor on each half-cycle of motion is given by the voltage change on C_p during flipping times C_p (to give the charge transferred), times $V_{\rm out}$. Using the high-Q approximation $\gamma \approx 1 - \pi/2Q$, this gives

$$E_{\frac{1}{2}} \approx \frac{8Q}{\pi} C_p V_{\rm out}\left[V_{po} - (V_{\rm out} + 2V_D)\right]. \tag{40}$$

From this we can find the optimum output voltage as simply

$$V_{{\rm out}_{\rm opt}} = \frac{V_{po}}{2} - V_D. \tag{41}$$

The output power is then $(\omega/\pi)E_{\frac{1}{2}}$, i.e.

$$P_{\max} \approx \left[1 - \left(\frac{V_D}{V_{po}}\right)^2\right]\frac{2Q}{\pi^2}\left(\frac{{I_o}^2}{\omega C_p}\right). \tag{42}$$

This gives the same value as the parallel SSHI circuits if $V_{po} \gg V_D$. A variation of this circuit is proposed in [29] with only one diode in the conduction path, so V_D is halved compared to the series SSHI case.

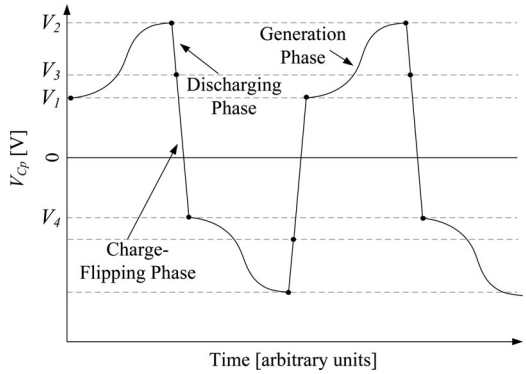

Fig. 24. Steady-state operating cycle of parallel SSHI with synchronous extraction circuit.

XIV. Parallel SSHI With Synchronous Extraction

The previous circuit combined the advantages of charge flipping for increased damping, synchronous charge extraction and a dc output. However, a disadvantage is that in order for it to operate, V_{po} must be greater than $2V_D$. We now propose a circuit, called parallel SSHI with synchronous extraction (see Fig. 23), which aims to retain all the advantages of the previous circuit and at the same time overcome the minimum requirement on V_{po}. This circuit introduces additional complexity in that there are now two control variables: the output voltage, V_{out} and the proportion of the stored energy on C_p to extract during each half-cycle.

We define V_1 as the voltage on C_p just after charge flipping has occurred, and V_2 as the voltage after generation has taken place, as shown in Fig. 24, with $V_2 = V_1 + 2V_{po}$. We now let α_e be the control parameter representing the proportion of the voltage on the capacitor C_p left after extraction through S_e (taking values between 0 and 1), and V_3 is the voltage on C_p after the discharge takes place, such that $V_3 = \alpha_e V_2$. Let α_f be the proportion of the voltage magnitude left after the charge flipping takes place, so the magnitude of the voltage after the flipping $V_4 = -\alpha_f V_3$. In steady-state operation $V_4 = -V_1$. Solving these expressions at $V_1 = -V_4$, we find that the steady-state condition of V_1 is

$$V_{1_{\text{ss}}} = 2V_{po}\frac{\alpha_e\alpha_f}{1-\alpha_e\alpha_f}. \tag{43}$$

A. Charge-Flipping Stage

The circuit has two Q factors: Q_f (of the flipping circuit) and Q_e (of the extraction circuit). The value of α_f in (43) is based only on the Q factor of the inductor of the flipping path Q_f, such that $\alpha_f = e^{-\frac{\pi}{2Q_f}} = \gamma$. The damped resonant frequency of this path is

$$\omega_{n_f} = \sqrt{\frac{1}{L_1 C_p} - \frac{{R_{s1}}^2}{4{L_1}^2}}. \tag{44}$$

Therefore S_f should be closed for a time π/ω_{n_f}.

B. Optimal Discharging Voltage Ratio α_e

The proportion of voltage left after discharging α_e is a control parameter, set by the discharge switch opening when the capacitor C_p voltage (starting from V_2) has fallen to that proportion of its initial value (i.e., V_3). When this happens there will be a current in the inductor, which will freewheel into the output power supply V_{out}. To find the optimal amount of energy to extract in each cycle, we can ignore the efficiency of the output stage since the energy extracted is not affected. The change in energy per half-cycle on the capacitor during discharging is

$$E_{\frac{1}{2}} = \frac{1}{2}C_p{V_2}^2 - \frac{1}{2}C_p{V_3}^2 = (1-{\alpha_e}^2)\frac{1}{2}C_p{V_2}^2. \tag{45}$$

Substituting V_2 for its steady-state value found from (43), and differentiating with respect to α_e we find that this expression is maximized when $\alpha_e = \alpha_f$.

C. Freewheel Energy Recovery

The differential equation describing the voltages along the freewheel loop is

$$L\frac{di(t)}{dt} + R_s i(t) + V_D + V_{\text{out}} = 0. \tag{46}$$

Solving this we find an expression for the inductor current with respect to time $i(t)$

$$i(t) = \left(i(0) + \frac{V_D + V_{\text{out}}}{R_s}\right)e^{-\frac{R_s}{L}t} - \frac{V_D + V_{\text{out}}}{R_s}. \tag{47}$$

The energy transferred to the power supply while the current is positive (it cannot go negative) is given by the integral:

$$E_{fw} = V_{\text{out}}\int_0^{t|_{i=0}} i_{fw}(t)dt = \frac{L_2 V_{\text{out}}}{{R_s}^2}i_{fw_o}R_s + \frac{LV_{\text{out}}}{{R_s}^2}(V_{\text{out}} + V_D)\ln\left(\frac{V_{\text{out}} + V_D}{i_{fw_o}R_s + V_{\text{out}} + V_D}\right) \tag{48}$$

where i_{fw_o} is the current at the start of freewheeling.

D. Maximizing Power Output

The energy from the capacitor C_p into the power supply during the discharge conduction (nonfreewheeling) stage is

$$E_{\text{out}} = V_{\text{out}}\int_0^{t_{S_e}} i_{\text{discharge}}dt = 2V_{po}\frac{(1-\alpha_e)C_p V_{\text{out}}}{1-\alpha_e\alpha_f}. \tag{49}$$

Substituting $\alpha_e = \alpha_f$ for maximum power extraction, and replacing V_2 with the steady-state value from (43), this gives a power output of

$$P_{\text{out}} = I_o V_{\text{out}}\left(\frac{2}{\pi}\right)\frac{\alpha_f - 1}{{\alpha_f}^2 - 1} + \frac{\omega}{2\pi}E_{fw}. \tag{50}$$

The final voltage on the piezoelectric capacitance after discharging is

$$V_{\text{final}} = (V_{\text{out}} + 2V_D) - \gamma\left(V_2 - (V_{\text{out}} + 2V_D)\right). \tag{51}$$

The power output of this circuit is maximized when V_{out} is set to a value such that $V_{\text{final}} = \alpha_e V_2$ without freewheeling

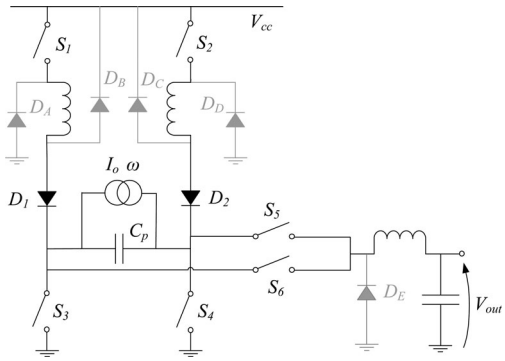

Fig. 25. Prebiasing circuit diagram, showing optional circuit components for nonoptimal output voltage operation in gray.

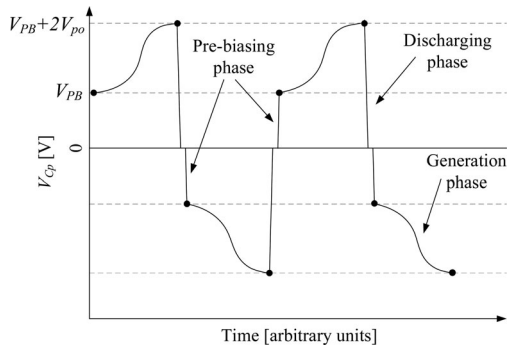

Fig. 26. Voltage waveform of the piezoelectric capacitance and operational cycle for the circuit of Fig. 25.

occurring, i.e., the switch S_e is closed for exactly one half-cycle. Substituting V_2 for the steady-state value found using (43), and solving for $V_{\rm out}$ gives

$$V_{\rm out_{opt}} = 4V_{po}\frac{\gamma}{(1-\gamma^2)(1+\gamma)} - 2V_D. \tag{52}$$

Substituting this into (49) gives a maximum power output of

$$P_{\rm max} = \frac{8}{\pi}\frac{\gamma}{(1+\gamma)^2(1-\gamma^2)}\left(\frac{{I_o}^2}{\omega C_p}\right) - \frac{4}{\pi}\frac{V_D I_o}{1+\gamma}. \tag{53}$$

Using the expansion $\gamma \approx 1 - \pi/2Q$ this expression simplifies to

$$P_{\rm max} \approx \left[1 - \frac{\pi V_D}{QV_{po}}\right]\frac{2Q}{\pi^2}\left(\frac{{I_o}^2}{\omega C_p}\right) \tag{54}$$

i.e., the same as for the previous circuit.

XV. Prebiasing

The prebiasing circuit (see Fig. 25), first proposed in [30], is a generalization of a number of the techniques analyzed so far, where the setting of the piezoelectric voltage and energy extraction occur as two independent phases. Previously the circuit was analyzed as a function of the overall efficiency that could be achieved in charging and discharging the piezoelectric capacitance. Here, a detailed analysis is performed for the first time in terms of the component values and hence Q factor.

The circuit is comprised of a modified H-bridge, which allows charging of the piezoelectric capacitance in either direction, and a synchronous buck output stage, which allows the extraction of an arbitrary amount of energy from C_p. Freewheeling paths exist to return energy to the power supply for operating modes where the switches must open when there is current in inductors. The voltage on the piezoelectric capacitance during operation is shown in Fig. 26. The exact voltage placed on the piezoelectric capacitance can be controlled, as can the exact amount of energy removed each cycle by the discharge circuit.

There are two possible modes of operation for this circuit.

1) *Optimal voltage control*: the power supply V_{cc} and output $V_{\rm out}$ voltages are set according to the optimal operating condition—i.e., energy transfer occurs without freewheeling occurring. Therefore, the diodes $D_{[A-E]}$ are not used to conduct freewheeling currents, although can be retained to deal with any freewheeling current that results from timing inaccuracy. Prebias voltages can be in the range $\approx 0 - 2V_{cc}$.
2) *Custom output voltage:* a nonoptimal regime that allows an arbitrary output voltage to be set by allowing energy transfer through freewheeling paths. Diodes $D_{[A-E]}$ are, therefore, required to conduct freewheeling currents. Prebias voltage is limited to V_{cc} because of the clamping of D_B and D_C.

For consistency with the analysis of the previous circuits, we will only consider the optimal operating regime, i.e., that which we term optimal voltage control.

The circuit operates in three phases. First, the prebias is applied by closing either S_1 and S_4, or S_2 and S_3 until $V(C_p) = V_{\rm PB}$. Then, the switches are opened and the piezoelectric capacitance floats, gaining more charge from the current source I_o, when motion occurs, until it is at a voltage $V_{\rm PB} + 2V_{po}$. Then, the entire charge is removed by the closing of S_5 and S_3 or S_6 and S_4, after which $V(C_p) = 0$. The process then repeats in the negative half-cycle.

A. Discharging Phase

Using the previous notation, the voltage on C_p after discharging is

$$V_2 = V_{\rm out} - \gamma(V_{\rm PB} + 2V_{po} - V_{\rm out}). \tag{55}$$

As previously discussed, this final voltage must be zero, with no freewheeling occurring, and so we set $V_{\rm out}$ to

$$V_{\rm opt} = \frac{(V_{\rm PB} + 2V_{po})\gamma}{1+\gamma}. \tag{56}$$

By substituting (56) into the power delivered to the power supply, which is derived from (17) as $V_{\rm out}C_p(V_{\rm PB} + 2V_{po})$, the energy into the output per half-cycle is

$$E_{\frac{1}{2}} = C_p(V_{\rm PB} + 2V_{po})^2\frac{\gamma}{1+\gamma}. \tag{57}$$

So, the discharge efficiency η_d can be written as follows:

$$\eta_d = 2\frac{\gamma}{(1+\gamma)}. \tag{58}$$

B. Charging Phase

If the piezoelectric capacitance starts at 0 V (having been perfectly discharged) then the prebias voltage after half a resonant cycle (lasting π/ω_n) is

$$V_{\rm PB} = (V_{cc} - V_D)(\gamma + 1). \tag{59}$$

Since $V_{\rm PB}$ is a control parameter, the required V_{cc} to achieve a given $V_{\rm PB}$ is

$$V_{cc} = \frac{V_{\rm PB}}{\gamma + 1} + V_D. \tag{60}$$

The energy expended by a power supply at V_{cc} charging a capacitor to a voltage of $V_{\rm PB}$ in a half resonant cycle is

$$E_{ps} = V_{cc} V_{\rm PB} C_p = V_{\rm PB} C_p \left(\frac{V_{\rm PB}}{\gamma + 1} + V_D \right). \tag{61}$$

Therefore, we can write the charge efficiency η_c as follows:

$$\eta_c = \frac{\frac{1}{2} C_p {V_{\rm PB}}^2}{E_{ps}} \approx \frac{1}{1 + \frac{\pi}{4Q} + \frac{2V_D}{V_{\rm PB}}}. \tag{62}$$

From (61) and (57), the per-cycle energy output is

$$E_{\frac{1}{2}} = C_p (V_{\rm PB} + 2V_{po})^2 \frac{\gamma}{1+\gamma} - C_p V_{\rm PB} \left(\frac{V_{\rm PB}}{\gamma + 1} + V_D \right). \tag{63}$$

From this expression, we find the optimal prebias voltage to be

$$V_{\rm PB_{opt}} = \frac{2\gamma V_{po} - \frac{1}{2} V_D (1+\gamma)}{1-\gamma}. \tag{64}$$

Therefore, the maximum power output from this circuit is

$$P_{\max} = \frac{\omega C_p}{\pi} \left[\frac{\gamma}{1-\gamma^2} 4 {V_{po}}^2 \left(1 - \frac{1+\gamma}{2} \frac{V_D}{V_{po}} \right) - \frac{{V_D}^2}{4} \frac{1+\gamma}{1-\gamma} \right]. \tag{65}$$

If V_D is set to 0 this becomes

$$P_{\max}|_{V_D = 0} = \frac{4}{\pi} \frac{\gamma}{1-\gamma^2} \left(\frac{{I_o}^2}{\omega C_p} \right) \approx \frac{4Q}{\pi^2} \left(1 - \frac{\pi}{4Q} \right) \left(\frac{{I_o}^2}{\omega C_p} \right). \tag{66}$$

Compared to the optimal resistive load this is a significant gain of

$$\frac{P_{\rm PB}}{P_{\rm ORL}} = \frac{16}{\pi} \frac{\gamma}{1-\gamma^2} \approx \frac{16Q}{\pi^2} \left(1 - \frac{\pi}{4Q} \right). \tag{67}$$

This increased power output is offset by the considerable complexity of the circuit due to the high number of components required.

XVI. Single-Supply Prebiasing

For a given Q factor, the previously analyzed prebiasing circuit exhibits the highest power output of those presented so far. However, the circuit requires three inductors and six switches, making a high Q factor harder to realize in that circuit than one with fewer inductors. We, therefore, now analyze an embodiment of the prebiasing method presented in [31], called single-supply prebiasing (see Fig. 27), which reduces the component count to four switches and one inductor. In addition, the existence of diode drops in the previously proposed circuits causes a reduction in efficiency when the generated voltage on the piezoelectric element is low. These diodes are either for rectification or to provide freewheeling paths. While in theory the diodes in any of the previously analyzed circuits could be implemented using synchronous rectifiers, the single-supply prebiasing circuit is particularly suitable for synchronous rectification due to the low component count, and the fact that the switches are always operated in synchronous pairs.

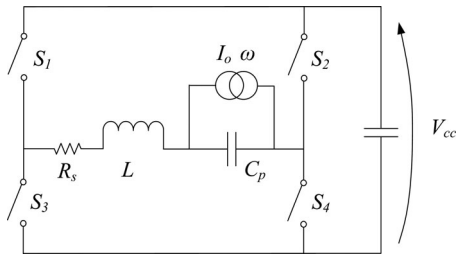

Fig. 27. Single-supply prebiasing circuit.

The circuit performs the same function as that presented in [32] except that it is implemented in a more efficient way, using a single voltage source, and requiring no diodes. The circuit of [33] is functionally similar, except that like the SSHI circuits all the energy is flipped through the output stage, and the circuit uses diodes instead of switches in the conduction paths, increasing the loss.

This circuit has a single voltage source from which the precharge is taken and into which the generated energy is returned. There exists a value of this voltage source that eliminates freewheeling currents entirely for both precharging and extraction, while allowing the piezoelectric capacitance to return to 0 V at the end of each half-cycle.

The basic principle of operation for a half-cycle of motion of the piezoelectric element is as follows: S_1 and S_4 are closed for exactly one half-period of the resonant cycle of the inductor L and the piezoelectric capacitance C_p, allowing the voltage on C_p to rise. The proof mass then moves, thus increasing the voltage in the same polarity. At the voltage maximum, the same switch pair is then closed again to discharge the piezoelectric to 0 V. The other pair of switches (S_2 and S_3) is used for the other half-cycle.

The operational cycle is similar to the prebiasing circuit of Fig. 26 in terms of the effect on the piezoelectric element, except that the same current path is used in charging and discharging with the advantage that fewer components are required. Since there are no freewheel paths, the switches must open only when the current in the inductor is zero, after a time π/ω_n. The voltage after charging $V_{\rm PB}$ is given as a function of the loss coefficient γ and the power supply voltage:

$$V_{\rm PB} = V_{cc}(\gamma + 1). \tag{68}$$

The voltage remaining after discharging $V_{\rm rem}$ is given by

$$V_{\rm rem} = V_{cc} - (V_{\rm PB} + 2V_{po} - V_{cc})\gamma. \tag{69}$$

The principle of operation of the circuit for maximum efficiency is that for a given harvester amplitude V_{po}, there exists a value of V_{cc} such that the voltage on C_p after discharging is exactly

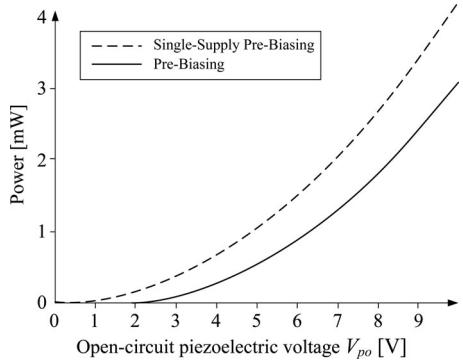

Fig. 28. Comparison between the prebiasing techniques in terms of output power for $C_p = 100$ nF, $L = 100$ μH, $V_D = 0.7$ V, $f = 100$ Hz, $Q = 10$.

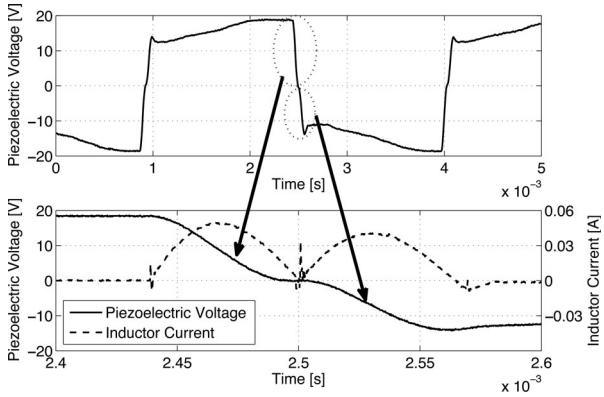

Fig. 29. Experimentally measured waveforms showing piezoelectric voltage over two cycles (top), and an expanded view of this voltage and of the inductor current during a transition (bottom).

0 and the switches, therefore, open under zero current, with no freewheeling path in operation. Solving $V_{\rm rem} = 0$ for V_{cc}:

$$V_{cc} = 2V_{po}\frac{\gamma}{1-\gamma^2}. \tag{70}$$

From this, in charging C_p an energy $C_p{V_{cc}}^2(\gamma+1)$ is borrowed from the power supply, and in discharging $V_{cc}C_p(V_{cc}(\gamma+1)+2V_{po})$ is returned. The power from the circuit is, therefore, the difference between these, multiplied by $2f$, with V_{cc} substituted with the value found in (70):

$$\begin{aligned} P_{\rm out} &= 8fC_p{V_{po}}^2\frac{\gamma}{1-\gamma^2} \\ &= \frac{4}{\pi}\frac{\gamma}{1-\gamma^2}\left(\frac{{I_o}^2}{\omega C_p}\right) \approx \frac{4Q}{\pi^2}\left(\frac{{I_o}^2}{\omega C_p}\right). \end{aligned} \tag{71}$$

This circuit, therefore, has the same limiting power output as the prebiasing circuit, but it can be seen that whereas the prebiasing circuit cannot produce net power below $2V_{po} = V_D$, the single-supply circuit both operates and produces more power over the entire range, with the two expressions converging at sufficiently high values of V_{po}. Fig. 28 shows the performance of the proposed circuit compared to the prebiasing circuit over a low-voltage operating range.

A. Experimental Results

In order to validate the theoretical results, the circuit was constructed on breadboard and connected to a Kingsgate KPSG-100 piezoelectric loudspeaker. The piezoelectric voltage and current waveforms are shown in Fig. 29. The top part shows the piezoelectric waveform for just over one cycle, and the bottom part shows a detailed view of the piezoelectric current and voltage for one discharge/charge cycle.

As can be seen, the resonant discharge pulse causes the piezoelectric voltage to return to zero. Once this has occurred, the charging pulse then prebiases the piezo ready for the next half-cycle of motion. The discharge pulse has a greater current magnitude than the charge pulse due to the mechanical to electrical energy conversion process.

The power output predicted by (71), given the measured component values ($C_p = 48.4$ nF, $L = 7.486$ mH, total $R_s = 317\ \Omega$, $\omega = 1998$ rd/s), is 10.33 mW. The actual net power as measured by a Yokogawa WT210 power analyzer was 10.1 mW, a deviation of about 2.3%. The small error is attributed to difficulty in measuring the exact series resistance of the piezoelectric element, and un-accounted-for parasitic capacitance of the inductor.

TABLE II
SUMMARY OF POWER OUTPUT OF CIRCUITS WITH RESISTIVE LOAD

Circuit	$\frac{P_{max}}{P_{ref}}$	$\frac{P_{max}}{P_{orl}}$ @$Q = 10, V_D = 0$
ORL	$1/4$	I
Sync Extraction	$2/\pi$	2.55
P SSHI R.L.	$\frac{1}{\pi(1/\gamma-1)}$	7.5
S SSHI R.L.	$\frac{1}{\pi}\frac{1+\gamma}{1-\gamma}$	16.24

XVII. COMPARISONS

In the previous sections, closed-form solutions for the optimized power output of each proposed circuit topology have been derived in terms of a common factor that now enables clear comparison between the circuits. Table II shows the relative performance of the circuits that operate into a resistive load, normalized to the simple optimal resistive load case of Fig. 5. Table III compares the circuits with a dc load against the optimal resistive load and bridge rectifier, assuming a zero on-state device voltage drop. For convenience we define:

$$P_{\rm ref} = \left(\frac{{I_o}^2}{\omega C_p}\right). \tag{72}$$

The comparison was performed in terms of an inductor Q factor independent of the volume of the device. The series SSHI technique is clearly superior in this comparison, outperforming the optimal resistive load by a factor of 16.24 for $Q = 10$. Fig. 30 shows the power gain over the rectified dc load circuit of Fig. 6 if the diode on-state voltage drops are neglected, and the inductor Q factor is equal to 10. From this it is clear that there are two distinct classes of circuit, those that do not depend on Q, and those that have a linear dependence. The first class have a constant power output that depends only on the excitation condition ${I_o}^2/\omega C_p$. The second class of circuits has

TABLE III
SUMMARY OF NONVOLUME-CONSTRAINED POWER OUTPUT FOR CIRCUITS WITH DC LOAD FOR $V_D = 0$

Circuit	$\frac{P_{max}}{P_{ref}}$	$\frac{P_{max}}{P_{ORL}}$	$\frac{P_{max}}{P_{RECTDC}}$
Rectified DC Load	$1/2\pi$	$2/\pi \approx 0.64$	1
S.S.E. DC	$\frac{4}{\pi}\frac{\gamma}{1+\gamma}$	2.34	4
Fixed-V Control	$1/2\pi$	$2/\pi \approx 0.64$	1
Fixed-V Control CC	$1/\pi$	$4/\pi \approx 1.27$	2
Parallel SSHI DC	$\frac{1}{\pi(1-\gamma)}$	8.76	$4Q/\pi$
Series SSHI DC	$\frac{1}{2\pi}\frac{1+\gamma}{1-\gamma}$	8.12	$4Q/\pi$
Parallel SSHI S.E.	$\frac{8}{\pi}\frac{\gamma}{(1-\gamma)(1+\gamma)^3}$	9.39	$4Q/\pi$
Pre-Biasing	$\frac{4}{\pi}\frac{\gamma}{1-\gamma^2}$	16.14	$8Q/\pi$
S-S Pre-Biasing	$\frac{4}{\pi}\frac{\gamma}{1-\gamma^2}$	16.14	$8Q/\pi$

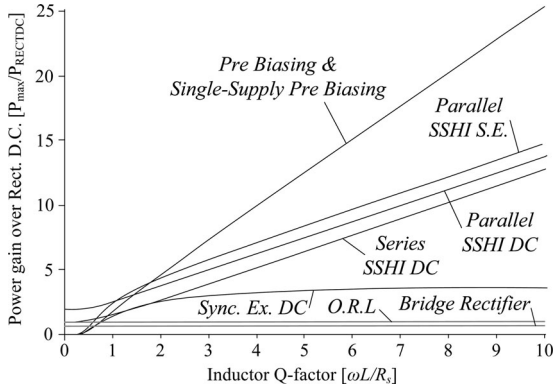

Fig. 30. Comparison of circuit power output against Q for $V_D = 0$.

a linear dependence on Q, and for these the power gain over a simple bridge rectifier tends to $4Q/\pi$ for moderate values of Q (around 10 or more). The prebiasing circuits too have a linear dependence, and have a higher power gain over the rectifier of $8Q/\pi$. When the piezoelectric fixed voltage control circuit (which performed worse than the optimal resistive load) was fitted with a charge-canceling switch that operated before the main charging path, the power output was doubled. This similarly is the cause of the increased power output of the prebiasing circuit, which can achieve the same bias voltage as the SSHI with synchronous extraction but only half the energy has to travel through the inductive paths as the entire charge is never flipped. A further comparison for those circuits with a dc output can be performed in terms of the voltage that must be supported if the circuit is operated at its optimal voltage so that freewheeling currents do not occur. Table IV shows these voltages as a function of the excitation voltage V_{po} for each circuit, sorted in order of maximum value of any of the voltages the circuit is required to support. In the case of low input excitation, a low output voltage (particularly where this is less than 1 V) may mean that the harvester requires further dc/dc power converter stages before a load can be connected.

In order to perform a fair comparison between the circuits with a fixed volume, the Q factor of the inductor must be reduced by a factor of 3 in the prebiasing circuit, as it has three inductors which must share the fixed volume. Fig. 31 shows a comparison of the power output against the piezoelectric open-

TABLE IV
SUMMARY OF NONVOLUME-CONSTRAINED OPTIMAL POWER SUPPLY VOLTAGES FOR $Q = 10$, $V_D = 0.5$

Circuit	Voltage normalised to V_{po}
Rectified DC Load	$V_{out} = 0.48$
Series SSHI DC	$V_{out} = 0.5$
S.S.E. DC	$V_{out} = 0.9$
Single-Supply Pre-Biasing	$V_{cc} = 6.3$
Parallel SSHI S.E.	$V_{1_{ss}} = 5.4$, $V_{out} = 6.8$
Parallel SSHI DC	$V_{out} = 6.9$
Pre-Biasing	$V_{PB} = 11.8$, $V_{out} = 81$, $V_{cc} = 6.4$

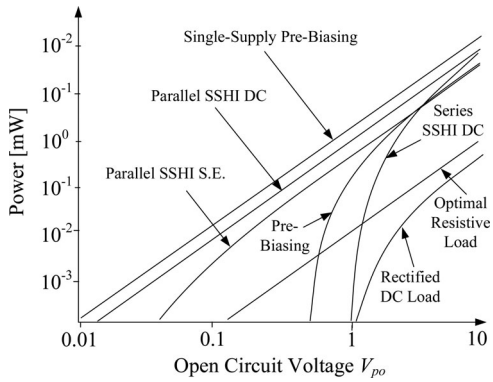

Fig. 31. Comparison of circuits with dc output for harvester config. 1.

circuit voltage V_{po} for the devices with a dc output (plus the optimal resistive load for reference). It can be seen that of these the single-supply prebiasing circuit of Fig. 27 performs best over the entire range.

It should be noted that the better performing circuits at low values of V_{po} all require overhead power for the associated control circuitry, which means their gross output power must be greater than the minimum required for this function. If the control can be achieved within 1 μW, then taking as an example the SSPB circuit operating at 100 Hz, with an inductor Q of 10 and a C_{po} of 100 nF, the total power can only exceed 1 μW for V_{po} above about 0.16 V.

XVIII. CONCLUSION

In this paper, all the principal circuit choices for interfacing to piezoelectric energy harvesters have been analyzed and compared in a unified analytical framework. The circuits have different levels of functionality, in that some are only able to dissipate energy in a resistive load and some are able to store the generated energy in a battery or capacitor and are hence significantly more useful in the majority of applications. Under many realistic operating conditions for energy harvesting devices, the damping force achievable from the piezoelectric element due to extraction of electrical energy is below that required for the harvester to operate at maximum power density, and in such cases, the challenge from a power processing perspective is to extract the maximum power possible from a current source with a shunt capacitance which is inherent in the piezoelectric element. The circuits analyzed in this paper which can extract more energy from the piezoelectric than can be extracted using

a simple bridge rectifier do so because they actively modify the voltage on the piezoelectric capacitance, meaning the charge from the current source is forced into a higher voltage, corresponding to increased work being done and correspondingly, an increase in the electrical damping and output power.

Accurate expressions for the power output of each circuit were obtained which include nonidealities in the components, particularly diode on-state voltage drops and series resistance in inductors. It was shown that, if diode drops are neglected, the output power from each circuit can be normalized to $I_o{}^2/\omega C_p$, which allows the performance of each circuit to be compared purely as a function of the Q factor of any paths containing an inductor. The circuits that flip the polarity of the charge on the piezoelectric element at the extremities of device motion, termed SSH, behave with approximately the same performance—the power gain over a simple passive bridge rectifier arrangement tends to $4Q/\pi$ for moderate values of Q (around 10 or more).

A circuit technique termed prebiasing separately precharges and discharges the piezoelectric capacitance and has a power gain over the simple bridge rectifier case of $8Q/\pi$. While the prebiasing and single-supply prebiasing variants have the same theoretical power, the single-supply prebiasing circuit requires two fewer switches and two fewer inductors (see Fig. 27). In theory any of the diodes in these circuits could be implemented with synchronous, bidirectionally blocking switches, although as seen in Table III, the prebiasing circuit retains advantages in terms of higher performance and lower complexity.

ACKNOWLEDGMENT

The authors would like to thank A. Elliott for his helpful contribution to the experimental results.

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