Physica E 45 (2012) 201–206

Contents lists available at SciVerse ScienceDirect

Physica E

journal homepage: www.elsevier.com/locate/physe

Effect of incorporation of zinc sulfide nanoparticles on carrier transport in silicon nanowires

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HIGHLIGHTS

- Silicon nanowires have been decorated with zinc sulfide nanoparticles.
- Detailed electrical characteristics were studied at low temperatures of 77 K–300 K.
- Increased dc conduction was obtained when zinc sulfide nanoparticles were incorporated in p^+-silicon nanowires.
- Decreased dc conduction was obtained when nanoparticles were incorporated in n-silicon nanowires.

ARTICLE INFO

Article history:
Received 13 June 2012
Received in revised form
14 August 2012
Accepted 16 August 2012
Available online 27 August 2012

Keywords:
Si NWs
ZnS NPs
Electrical characteristics
Schottky emission
SCLC effect

ABSTRACT

We investigate the transport properties of silicon nanowires coated with zinc sulfide nanoparticles. Silicon nanowires were prepared by metal assisted electro-less chemical etching technique. The diameter of nanowires varies from 30 to 300 nm and length was ~30 μm. Zinc sulfide nanoparticles having diameter ~30 nm were synthesized by co-precipitation method. The nanoparticles were then deposited between the nanowire arrays and most of the nanoparticles stick to the surfaces of the nanowires. The *JV* characteristics of the devices were investigated from 77 to 300 K. The *JV* characteristics were nonlinear and asymmetric. The decrease in current density in n-silicon nanowires while increase in current density in p^+-silicon nanowires were observed when zinc sulfide nanoparticles were coated on them. The decrease in the current density due to the presence of nanoparticles on the walls of the n-silicon nanowires is attributed to enhancement of trapped charge carriers at zinc sulfide nanoparticles and nanowire interface. However increased hole current was observed due to the formation of acceptor like states on the surfaces of p^+-silicon nanowires when nanoparticles were coated on them. The detailed carriers transport mechanisms were studied in both types of silicon nanowires. With back to back Schottky diode, Schottky emission mechanism was observed in p^+-silicon nanowires while unusual space charge limited current with and without traps was observed in n-silicon nanowires.

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1. Introduction

In the last few decades of advanced microelectronics, silicon nanowires (Si NWs) among all one dimensional nanostructures have attracted great interest as functional components in modern nano-electronic devices [1–5]. However over the successful fabrication of Si NWs on the large scale it is quite interesting to make the surface modifications for different applications in electrical devices [6–7]. Progressively nowadays, Si based nanostructures decorated with II-VI semiconductors are being widely used to enhance the electrical characteristics for variety of applications [8–11]. Most of the II-VI semiconductor nanoparticles (NPs) e.g. CdS, CdSe, CdTe, PbSe, and PbS, contain toxic elements such as Cd, Pb, and Se. However among these II-VI semiconductor NPs, ZnS is nontoxic. Its non-toxicity, low cost, high refractive index, wide band gap, and abundance availability makes it suitable for photovoltaic and optoelectronic applications [12–14]. Variety of techniques e.g. hydrothermal, chemical, micro emulsion, chemical vapor deposition, etc. are available to synthesize II-VI NPS [15]. Here we used chemical route to synthesize ZnS NPs due to its simplicity.

In this work we investigate the electrical properties of ZnS NPs coated n and p^+ type Si NWs. ZnS NPs with an average diameter ~30 nm were incorporated with the ~30 μm vertical Si NWs. SEM images revealed that ZnS NPs stick to the Si NWs surface.

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http://dx.doi.org/10.1016/j.physe.2012.08.007

2. Experimental details

The Si NWs were prepared by metal assisted electro-less chemical etching technique [16–21]. The resistivity of used p^+-Si and n-Si substrates was 0.0085–0.0115 Ω cm and 1–10 Ω cm respectively. Initially (1 0 0) oriented p^+-Si and n-Si wafers were cleaned with isopropanol and de-ionized water. The wafers were then immersed in a solution of 0.06 M silver nitrate and 5.6 M HF for 5 min to form dendrites of Ag on silicon surface. Later the wafers were placed in mixed solution of 0.6 M H_2O_2 and HF for 1 h at room temperature. The length of NWs depends on the etching time. Longer etching times will result in large length of NWs and vice versa. After 1 h of etching the wafers were washed repeatedly with water. Ag was then removed using HNO_3. Fig. 1(a) and (b) shows the top and cross sectional view of the prepared Si NWs respectively. The length of NWs ~30 μm and diameter is 30–300 nm.

To synthesize ZnS NPs, 0.1 M zinc chloride ($ZnCl_2$) was dissolved in 25 mL of ethylene glycol (EG) and heated to 100 °C (solution 1). Then 0.2 M of thiourea [$SC(NH_2)_2$] as a S^{2-} source was dissolved in 25 mL of EG (solution2). Ethylene glycol (EG) was used as a solvent and capping agent due to its extensive use for the synthesis of nano sized transition metal and semiconductor NPs [13]. Under vigorous magnetic stirring, solution 2 was poured drop wise into solution 1. Here the metal ions Zn^{2+} reacted with sulfur of thiourea. The mixed solution was heated to 200 °C for 25 min. At this stage the solution started to become milky white, indicating the formation of ZnS NPs. Stirring was continued up to 1 h to complete formation of NPs. The average size of NPs decorated with NWs is estimated of about 30 nm.

Later 50 μL of ZnS NPs solution were poured on the Si NWs. The ZnS NPs stick to surfaces of the NWs as shown in Fig. 1c (inset). Minute quantity might have settled down on the substrate at the bottom of the NWs. The samples were then dried in air. Fig. 1(c) shows the EDX pattern of the Si NWs coated with ZnS NPs. Clear indication of presence of ZnS NPs can be seen from the graph.

Finally the top and the bottom metal contacts were made using different metals. 50 nm Cr followed by 300 nm Au was sputtered on p^+-Si NWs devices while Cr of 50 nm followed by Al of 300 nm was thermally evaporated on n-Si NWs devices. Cr was used for a purpose of good sticking of metal contact with our devices. Fig. 1(d) shows the schematic diagram of the completed device. The JV characteristics of the Si NWs and ZnS NPs coated Si NWs were investigated from 77 to 300 K using an Agilent 4155B semiconductor parameter analyzer.

3. Results and discussions

The JV characteristics were measured using the Agilent 4155B semiconductor parameter in the temperature range 77–300 K. Fig. 2(a) and (b) shows the JV characteristics of p^+-Si NWs and p^+-Si NWs coated with ZnS NPs in the temperature range 77–300 K. The current density J was calculated using the top metal electrode area which is slightly exaggerated than the actual area of conducting region in these multiple nanowire diodes. The JV characteristics are nonlinear and asymmetric. Current density is temperature dependent in all cases. Fig. 2(c) identifies that the decorated p^+-Si NWs with ZnS NPs have larger current density as compared to that of p^+-Si NWs. The presence of ZnS NPs greatly changes the surface states of Si NWs. The increased current density in case of decorated NWs is based on the accumulation of hole carriers because there is a contribution of hole carriers of ZnS itself exhibiting p-type behavior [22]. Furthermore the creation of acceptor like states at p^+-Si NW/ZnS NPs interface causes the enhancement in hole current concentration and hence the increased conductivity. The increase in hole current at p^+-Si with ZnS NPs has been observed by Hazdra et al. [23]. In addition to the enhancement in conduction, for device application, it is very important to understand the transport properties of Si nanostructures. JV characteristics of our devices are consistent with metal–semiconductor–metal (M–S–M) junctions with two back to back Schottky barriers exhibiting clear rectifying behavior.

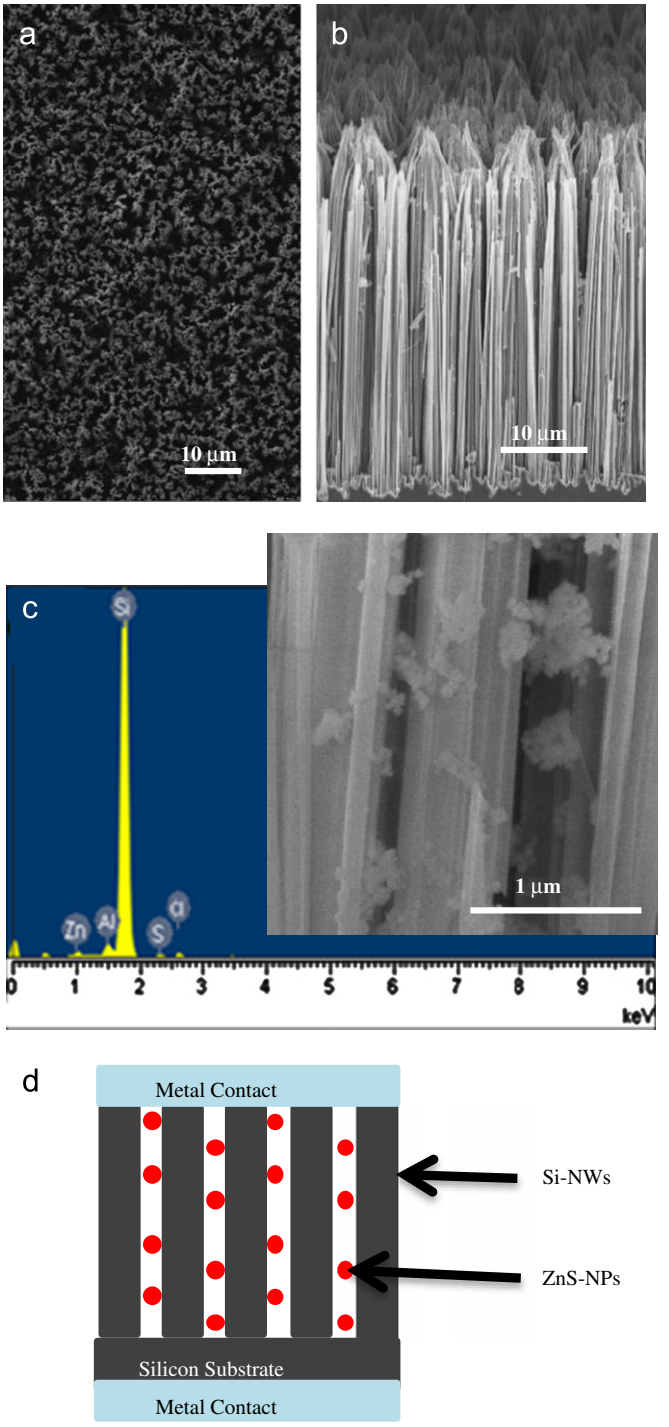

Fig. 1. (a) Planer SEM image of Si NWs, (b) cross-sectional SEM image of NWs, (c) EDX spectrum of ZnS decorated system (The inset shows SEM image of decorated structure of NWs with ZnS NPs, similar images were seen for both p^+- and n-Si NWs decorated with ZnS NPs) and (d) Schematic diagram of decorated structure of NWs with NPs.

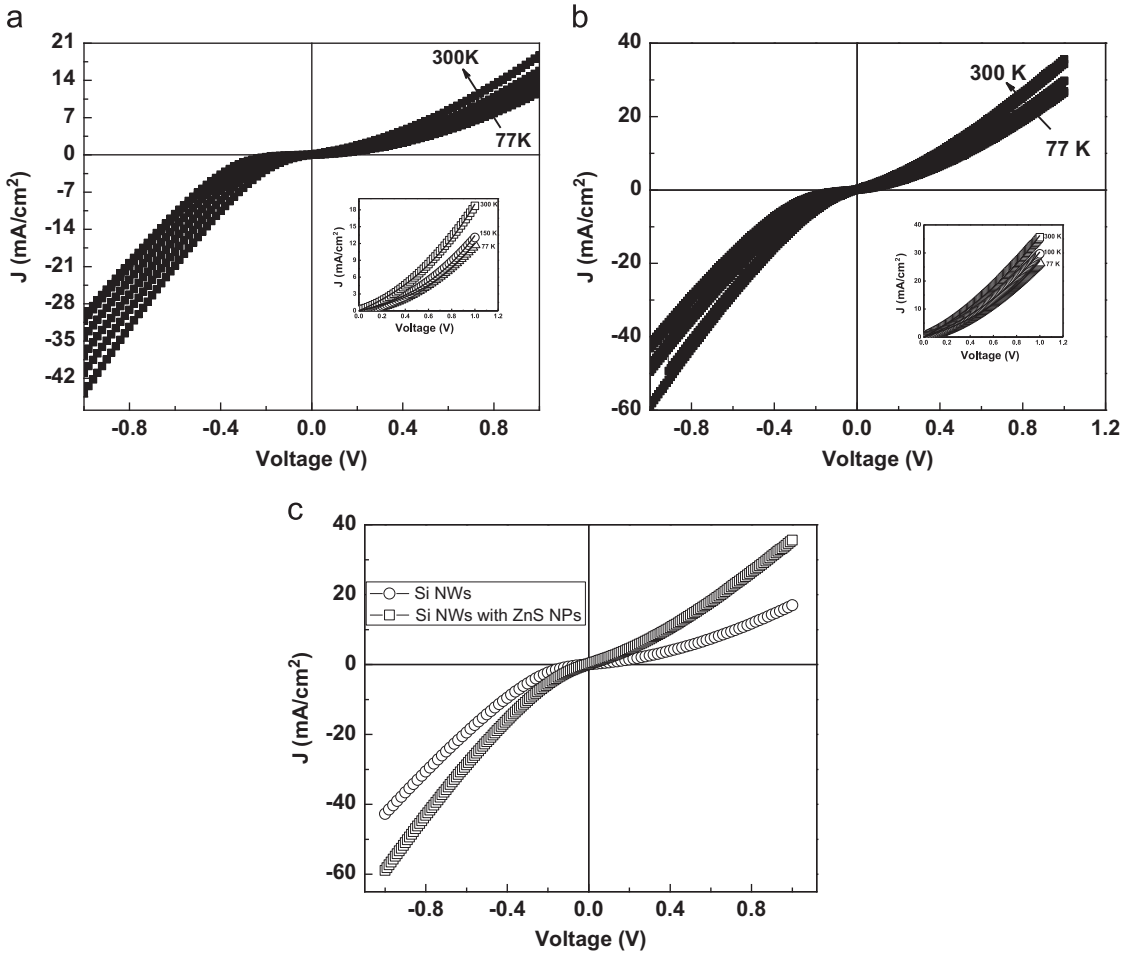

Fig. 2. *JV* characteristics of (a) p^+-Si NWs (b) p^+-Si NWs/ZnS NPs in the temperature range 77 K–300 K (Insets in fig. (a & b) shows the non-linear curve fitting of Schottky emission equation on selected temperatures data) and (c) Comparison of *JV* characteristics of decorated and without decorated structures at 300 K.

The forward bias *JV* characteristics obey thermionic emission model and the current can be expressed as [24]:

$$J = J_s\left[\exp\left(\frac{qV}{nkT}\right) - 1\right] \tag{1}$$

where J_s is the saturation current density expressed as follows:

$$J_s = A^*T^2\exp\left(-\frac{q\varphi_b}{kT}\right) \tag{2}$$

where q is electron charge, n is ideality factor, k is Boltzmann constant, T is measurement temperature, A^* is Richardson constant (120 A/cm^2/K^2) and φ_b is the Schottky barrier height of diode.

The non-linear curve fitting on selected temperatures based on Eq. (1) is shown in inset of Fig. 2(a) and (b). The Schottky barrier height φ_b can be calculated using Eq. (2):

$$\varphi_b = \frac{kT}{q}\ln\left(\frac{A^*T^2}{J_s}\right) \tag{3}$$

The saturation current density J_s and ideality factor n was calculated using the non-linear curve fitting of Eq. (1).

The calculated ideality factors and barrier heights are plotted at different temperatures and are shown in Fig. 3(a) and (b) respectively. It is clear that ideality factor decreases with increase of temperature while the barrier height increases with increase of temperature. The ideality factor for Si NWs coated with ZnS NPs is larger than those of Si NWs. Huge deviation of ideality factor is because of the presence of large number of trapping states which are commonly observed in the heterostructures of two different materials with large lattice mismatch [8] as is the case for Si and ZnS. Schottky barrier height was calculated using Eqs. (1)–(3) based on hugely deviated ideality factor to provide qualitative behavior of Schottky barrier height with temperature for our Si NW devices.

We also analyzed the *JV* characteristics of *n*-Si NWs devices. Fig. 4(a) shows the *JV* characteristics of *n*-Si NWs from 77 to 300 K. The *JV* characteristics are nonlinear and asymmetric. Here current density is ~80 mA/cm^2 at 1 V. Similarly for p^+-Si NWs, current is ~20 mA/cm^2 at 1 V (Fig. 2(a). It seems opposite to what is expected from the difference of their doping concentrations. However, this may be due to the fact that different metal electrodes were used for both type of Si NW devices. In case of p^+ Si NWs, the contact was made using sputtered Au whereas evaporated Al was used for *n*-Si NWs. However in this study we do not compare p^+-Si NWs with *n*-Si NWs. We only compare the effect of incorporation of ZnS nanoparticles for each case separately.

To study the transport mechanism of this device, double logarithmic ($\ln I$ versus $\ln V$) graph is plotted in the forward bias as shown in Fig. 4(b). This figure shows the power law ($J \propto V^m$) behavior of current density with different values of m. The current transport mechanisms are differentiated on the basis of this power law. As observed in Fig. 4(b), the double logarithmic graph of the device shows three distinct linear regions. The first region is the ohmic region having a slope of about one and it obeys ohm's law. At higher voltages square power law $J \propto V^2$ is obtained as a second region (II). These results of second region show that the

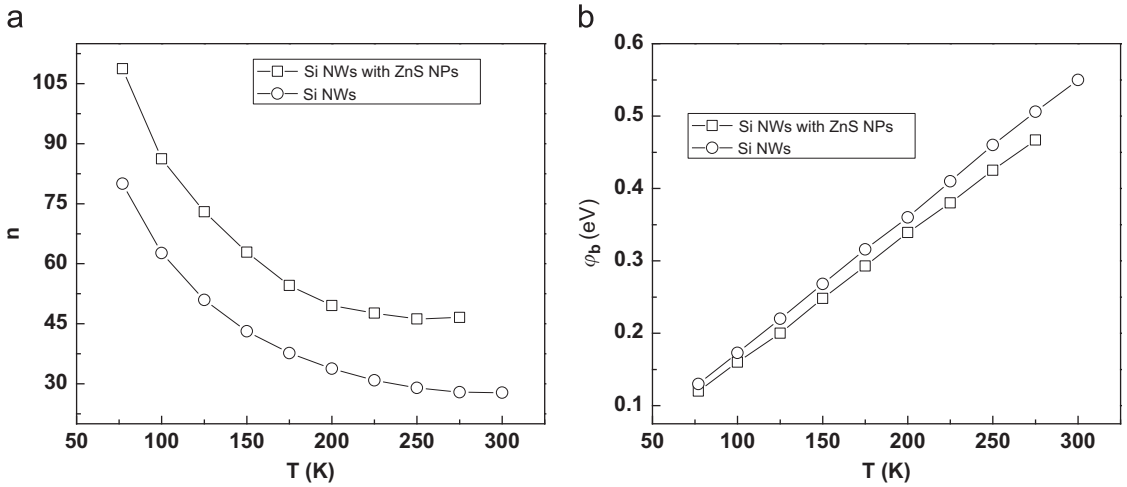

Fig. 3. Temperature dependence of (a) Ideality factor (n) and (b) Barrier height φ_b calculated from fitting of Schottky emission equation of p^+-Si NWs decorated with and without ZnS NPs.

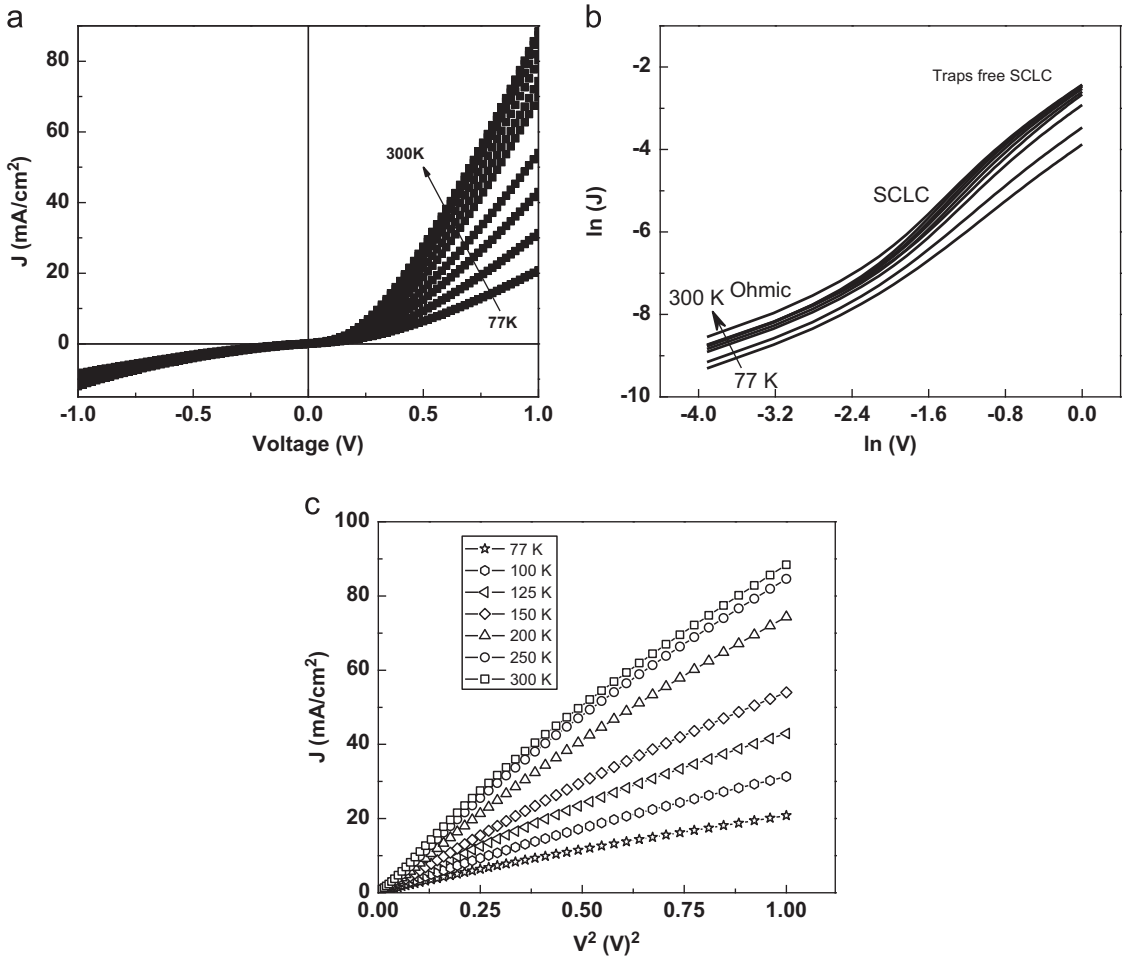

Fig. 4. *JV* characteristics of (a) n-Si NWs in the temperature range 77 K–300 K, (b) double logarithmic graph of n-Si NWs showing three regions and (c) J–V^2 variation at selected temperatures.

transport mechanism is space charge limited current (SCLC) dominated by a discrete trapping level in region II. This observation of space charge regime is normally observed in the case when the doping level of semiconductors is relatively low. We can see the comparison of doping concentration of this n-Si and previous highly doped p^+-Si. In this case of SCLC the injected carriers at contacts are high as compared with internal carrier concentration therefore these injected carriers cannot be completely screened by doping carriers. Thus it is the fundamental reason behind this happening of space charge region because of low screening of more injected carriers and this situation is more exacerbated in NWs when there is very little material available for the screening of injected carriers. Furthermore the charge trapping states in NWs [25] and due to high surface to volume ratio in NWs the

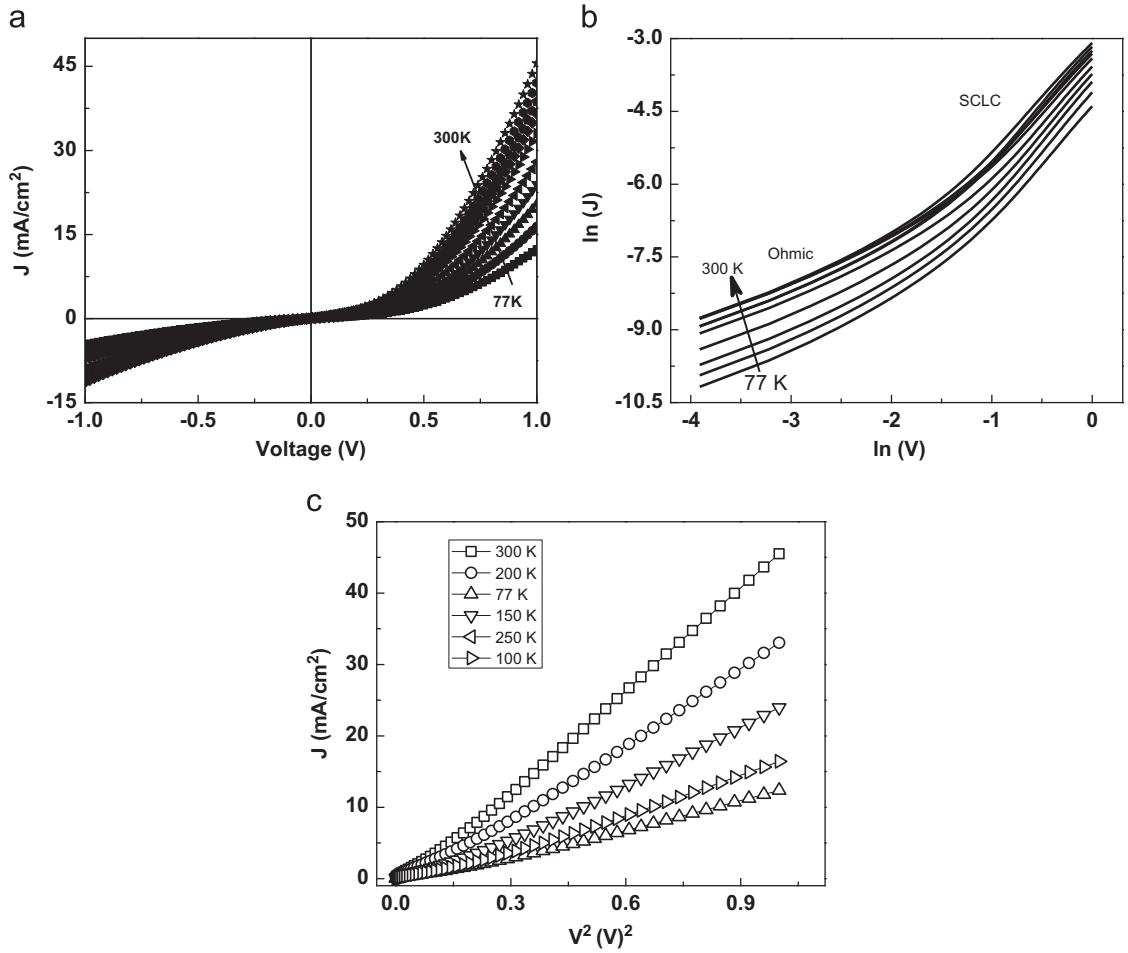

Fig. 5. *JV* characteristics of (a) *n*-Si NWs decorated with ZnS NPs in the temperature range 77 K–300 K, (b) double logarithmic graph of *n*-Si NWs decorated with ZnS NPs showing two regions and (c) $J-V^2$ linear variation at selected temperatures showing the presence of SCLC.

carriers depletion [26] at surface states causes this unusual space charge limited conduction. Further the third region has slope $m\sim 2$ which is assumed to be the part of space charge limited conduction without free traps or completely filled traps. It is to point out that slope of curves changes for the temperature above 150 K as shown in Fig. 4 (c) of power square law where the linear behavior start tends to change at the above mentioned temperature. This phenomena of trap free SCLC shows that the traps are completely filled or get enough energy to get out of trapping states and contribute to conduction due to higher temperature effect and at a voltage region of above 0.8 V. Similar phenomena was seen in literature [27].

Fig. 5(a) shows the *JV* characteristics of ZnS NPs decorated *n*-Si NWs from 77 to 300 K. These *JV* characteristics are also nonlinear and asymmetric. Double logarithmic graph of *JV* characteristics of this device showing two distinct regions is shown in Fig. 5(b). In this case again first region corresponds to ohmic region having slope of approximately one, while the second region corresponds to the space charge region obeying the square power law $J\propto V^2$. The linear behavior of current density against square of voltage as shown in Fig. 5(c) proves the presence of SCLC. Now in this case SCLC effect prolongs over the high temperatures and voltage as compared with the bared *n*-Si NWs and this is attributed to the addition of ZnS traps.

Fig. 6 identifies that the decorated *n*-Si NWs have smaller current density values at 300 K as compared to bared *n*-Si NWs. The behavior is opposite to that observed for p^+-Si NWs case discussed above. The deposited NPs stick to the walls of the NWs as can be seen from the SEM image (Fig. 1c). ZnS is wide band gap

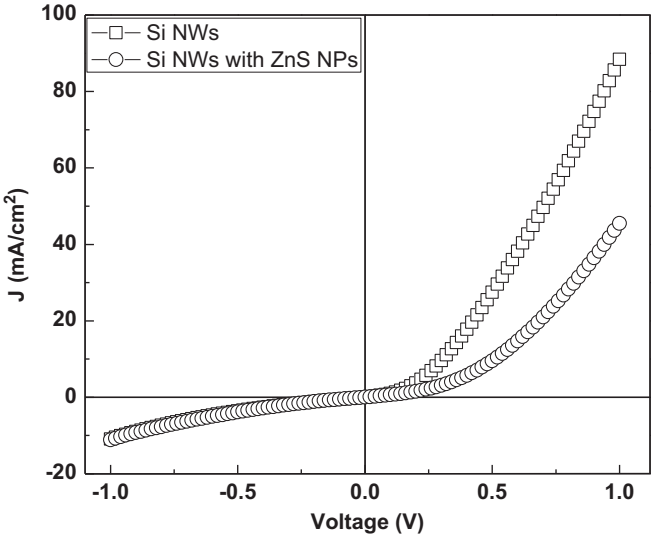

Fig. 6. Comparison of *JV* characteristics of decorated and without decorated structures at 300 K.

material with lot of trap states [11]. The presence of ZnS NPs on walls of the *n*-NWs enhances the trapping of electrons and increases the resistance of the *n*-Si NWs. Therefore we see decrease in the current density for NWs decorated with NPs. Such defects

states has been reported by Hazdra et al. [23] where they investigated *n*-silicon surfaces contaminated by ZnS over layers.

4. Conclusion

The effect of ZnS NPs on the transport properties of p^+-Si and *n*-Si nanowires was studied. The ZnS NPs prepared by co-precipitation method and the Si NWs prepared by metal assisted electro-less chemical etching technique were used to form a hybrid nanostructure. The *JV* characteristics of Si NWs and ZnS NPs coated Si NWs were measured from 77 to 300 K. The Schottky effect was observed as the transport phenomena in decorated and without decorated p^+-Si NWs while the unusual SCLC with and without traps was observed in decorated and without decorated *n*-Si NWs. The presence of ZnS NPS on the walls of the *n*-Si nanowires reduces the electron current due to trapping of electrons at the *n*-NW/NP interface. On the other hand presence of ZnS NPs on p^+-Si nanowires increased the hole current due to the formation of acceptor like states.

Acknowledgments

We acknowledge the financial support of the Higher Education Commission (HEC), Pakistan, through (5000) Indigenous Ph.D. scholarship scheme and the International Research Support Initiative Program (IRSIP).

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