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Single-electron and quantum confinement limits in length-scaled silicon nanowires

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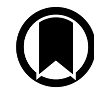

Abstract

Quantum-effects will play an important role in both future CMOS and 'beyond CMOS' technologies. By comparing single-electron transistors formed in un-patterned, uniform-width silicon nanowire (SiNW) devices with core widths from ~5–40 nm, and gated lengths of 1 μm and ~50 nm, we show conditions under which these effects become significant. Coulomb blockade drain–source current–voltage characteristics, and single-electron current oscillations with gate voltage have been observed at room temperature. Detailed electrical characteristics have been measured from 8–300 K. We show that while shortening the nanowire gate length to 50 nm reduces the likelihood of quantum dots to only a few, it increases their influence on the electrical characteristics. This highlights explicitly both the significance of quantum effects for understanding the electrical performance of nominally 'classical' SiNW devices and also their potential for new quantum effect 'beyond CMOS' devices.

Keywords: silicon nanowires, single electron effects, quantum dots, room temperature single electron transistor

(Some figures may appear in colour only in the online journal)

1. Introduction

By reducing device dimensions and developing new device structures, CMOS technology has delivered dramatic and continuous improvements in the speed, complexity and packing density of integrated circuits over a period of 40 years. These have required improvements in fabrication processes, lithography and materials. With several manufacturers having adopted or preparing for 14 nm node devices and minimum feature sizes <10 nm being planned, increasingly challenging barriers are being encountered in both device physics and technology [1]. At the scaling limit for planar MOSFET devices, a transition to non-planar Fin-FET [2] devices for the 14 and 10 nm device nodes is occurring [3, 4].

While both silicon and non-silicon alternatives are being considered, such as III–V and III–V-silicon devices [5], hetero-junction tunnel field effect transistors [6, 7], graphene [8] and $MoSi_2$ [9], there are likely to be significant manufacturing problems with the addition of non-silicon technologies. However, in addition to the major technological challenges posed by any successor 'beyond CMOS' technology at these scales (<10 nm), quantum effects are increasingly likely to influence the behaviour of all these devices adversely, even those which are not specifically quantum-dot (QD) devices. For example, the operation of a Fin-FET, with a fin only ~4 nm wide, has been shown to be fundamentally limited by quantum confinement [4]. Fortunately silicon itself offers distinct attractions for quantum devices [10].

In addition to these technologies, at dimension <10 nm single-electron (SE) devices [11–13] look increasingly attractive. Unlike 'classical' FETs, these devices inherently show performance improvements with reduction in size, but may require new approaches both for operation within circuits, and for lithographic and fabrication technologies at the sub-5 nm scale [14]. As highly scaled Si nanowires (SiNWs) can be used as the basis for SE/QD transistors operating at room temperature [15–17], it is possible to envisage a direct transition from SiNW FETs to SE/QD devices. SiNWs may then inherently provide the basis for a quantum effect 'beyond

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CMOS' technology [14]. This paper uses SiNWs to study the transition to increasingly dominant quantum behaviour.

2. Silicon nanowires

SiNWs defined by lithographic [18, 19], growth [20] or etching techniques [21] have been widely investigated over the last decade. In these devices, the channel cross-section may be scaled in both dimensions to ~10 nm, with gates fully surrounding the channel [18]. However, device operation remains essentially 'classical' in nature. SE devices such as single-electron transistors (SETs), based on SiNWs, have been defined using various approaches [11–13]. A widely investigated approach is to pattern a NW along its length, using either constrictions [22–25] or pattern dependent oxidation (PADOX) [15, 26]. The later technology utilizes areas of increased stress, e.g. at corners where the NW meets source/drain regions, to enhance oxidation and create SiO_2 tunnel barriers. Both single [17] and chains of islands [24], forming a multiple tunnel junction (MTJ), have been used. Alternatively, nanocrystalline silicon [27–29] or silicon nanochain material [30, 31] have been used to define tunnel barriers and islands 'naturally'. Relatively recently, by reducing the Si island size to <10 nm, such that the SE charging energy $E_c \gg k_B T = 26$ meV at 300 K, strong room-temperature SE current oscillations with very large peak–valley ratios have been reported [17, 24, 29, 32].

In contrast to SETs using patterned SiNWs, it has long been recognized that SE effects may be observed at low temperatures even in *un-patterned*, nominally smooth NWs, typically defined in silicon-on-insulator (SOI) material [33]. Here, the SiNWs can be very similar to those used for nanoscale FET application. In early work on SE devices, un-patterned SiNWs were used to fabricate SE memory [34], and logic devices [35]. Although QDs were not explicitly patterned in these devices, it is believed that disorder in the doping concentration, surface roughness or quantum confinement in narrow sections of the NW could pinch-off sections of the NW [33, 36, 37]. This leads to the formation of a MTJ and associated SE effects.

This paper reports on investigations into the formation of QDs along nominally un-patterned uniform SiNWs, having a core diameter of ~5–40 nm, as the NW length is reduced from 1 μm to ~50 nm. The devices are investigated over a wide temperature range, from 8–300 K. This configuration allows us to establish if SE and quantum confinement effects remain significant even if the nanowire length is reduced, nominally reducing the likelihood of QD formation. The NWs are investigated in a SET configuration, with side-gates covering a NW length of either 1 μm or only ~50 nm. The devices are defined in heavily-doped n-type SOI material.

Even without patterning the NW into a chain of islands, we find that in long, uniform NWs, SE effects persist at 280 K and strong SE effects occur up to ~220 K. The SE effects are associated with the natural formation of ~20 QD MTJ in the NW. Arrhenius plots have been used to extract a large activation energy $E_a \approx 0.276$ eV for thermally activated current. This energy is associated with the highest SE charging energy $E_c = \frac{e^2}{2C_T} = 0.2$ eV for a QD having a capacitance C_T along the NW, extracted from the charge stability diagram. In a short ~50 nm NW SET with a Si core of only ~5 nm, Coulomb blockade and a SE current oscillation is observed at 300 K. Here, the charging energy is $E_C \sim 0.5$ eV $\gg k_B T = 26$ meV at 300 K. In a further device with point-gates, ~50 nm in width and on either side of a ~200 nm NW, the number of QDs reduces to only three independent, uncoupled QDs and quantum confinement effects become observable. Based on these values, SE Monte Carlo simulations have been used to model the electrical characteristics of both devices, using capacitances extracted from the charge stability diagram and supported by Arrhenius plots. A comparison between a 1 μm NW and a point-contact three-QD device shows that as the NW length is scaled, quantum effects also become observable explicitly in the electrical characteristics. This highlights the significance of these effects for the limits of CMOS at the <10 nm scale, and the potential of short SiNWs for quantum-effect 'beyond CMOS' technology.

3. Experiment

Electron-beam lithography (EBL) and trench isolation were used to fabricate SiNW SETs in SOI material. Devices with NWs widths down to ~30 nm and lengths 1 μm to ~50 nm have been defined. A schematic diagram of the two device structures is shown in figure 1(a) (parallel side gate) and (b) (point-gates). The SiNW, and dual, in-plane gates parallel to the NW, were defined in the top Si layer of the SOI material, using EBL and reactive-ion etching for trench isolation of the gates. The NW current was controlled using one or both gates. SEM images of two NW SETs (after oxidation) are shown in figure 1 with parallel gate structures along a 1 μm NW (c), and 'point-gate' structures along a ~200 nm NW (d). Figure 1(e) shows an SEM image of a SET with a narrow, 50×50 nm NW and only a single point-gate, before oxidation. Devices (d) and (e) were used in the measurements reported later. The maximum variation in width of the device in (d) is 10%. A gradual transition is used where the NW meets the source/drain contact regions to minimize PADOX effects. As defined, the NWs had a minimum width of ~30 nm. Oxidation of the structure was used to reduce the Si core of the NW to ~20 nm. Trenches ~200 nm deep were used to electrically isolate the device. A group of four transistors with common gates and drain terminals were fabricated on each sample. Details of the fabrication steps are given below:

Samples consisted of (100) oriented 1 cm square SOI chips, doped n-type with a 120 nm thick top Si layer and 130 nm buried oxide layer. These were oxidized at 1100 °C for 2 h in oxygen, with a ramp time of 1 h to maximum temperature, followed by natural cooling to room temperature. This formed a SiO_2 layer ~200 nm thick, capping the top-Si. As the process consumed ~100 nm of the top-Si, this resulted in a top Si layer as thin as ~20 nm. A HF dip of 5 min

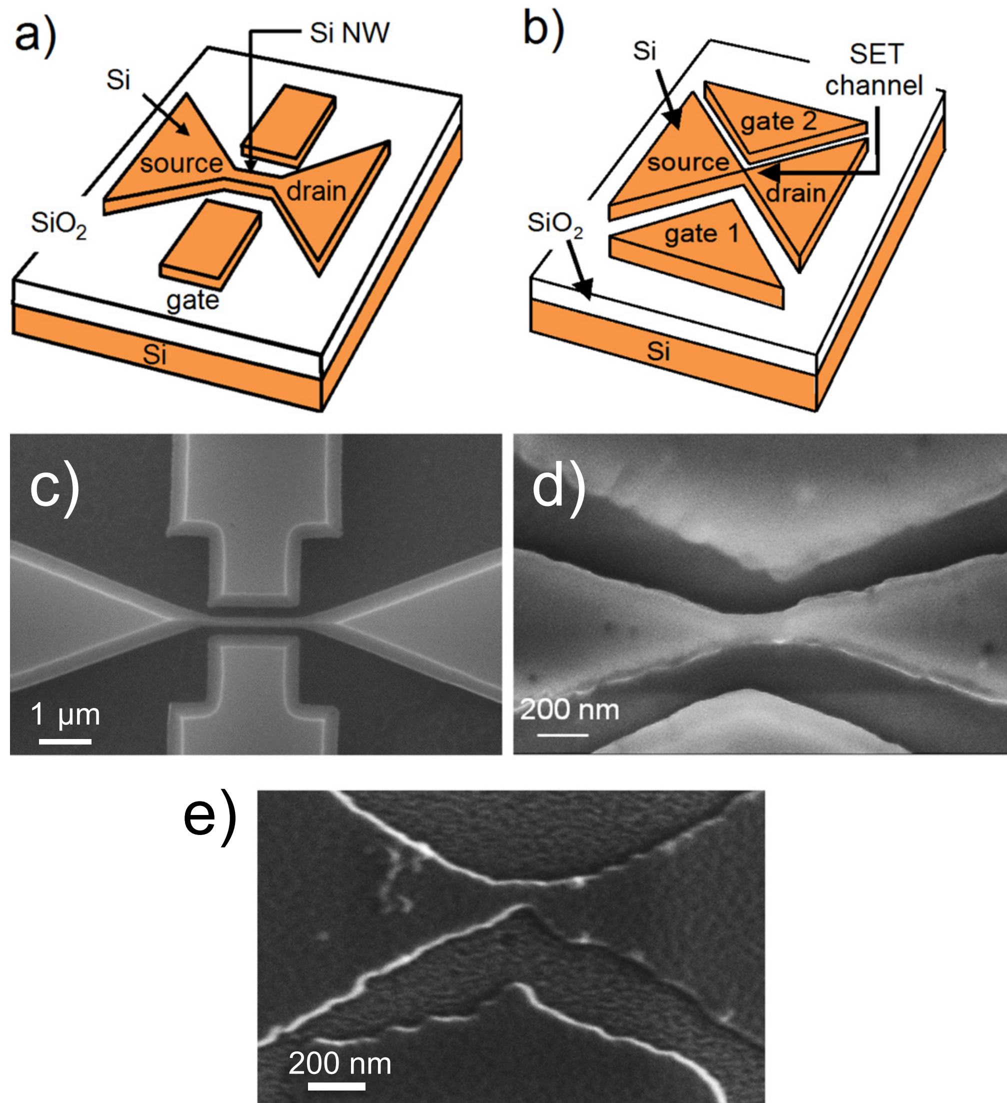

Figure 1. Device structure of NW SETs fabricated on a SOI chip, shown in schematic form, (a) 1 μm NW and (b) ~200 nm point-gate device. (c),(d) show SEM images (after oxidation) of 1 μm NW and ~200 nm NW devices. The higher resolution image (d) is obtained at 30° angle from the horizontal. (e) SEM image of a short 50 × 50 nm NW, taken before oxidation.

was then used to remove the unwanted SiO_2 at an approximate rate of 25 nm min^{-1} [38], with an allowance being made for a small over-etch.

Unlike previous work on Si NWs doped by implantation [38], the top Si layer was doped by the application of a spin-on-dopant (SOD) layer using phosphorus [39]. The SOD layer was applied at 2500 rpm for 50 s, to form a layer ~3 μm thick. This was followed by a bake at 200 °C for 30 min, to make the layer solid. A rapid thermal annealing (RTA) process in nitrogen ambient, lasting 2 min, at 1000 °C, was used for dopant diffusion with the aim of producing a doping concentration of $\geqslant 10^{19}$. This was confirmed using a 4-point probe measurement of resistivity.

The SET patterns were exposed by EBL using a LEO 1450VP SEM operating at 30 kV, modified by the addition of a Xenos pattern generator. A 100 nm thick resist layer of 950 k MW PMMA was spin-coated, from a 2% solution of anisol and developed in 1:3 MIBK: IPA. The NW part of the devices was exposed first, using single-pass lines at a line exposure dose of 2 nC cm^{-1}. This was followed by the source, drain and gate lead-in areas, aligned with the NWs, which were all exposed using an area dose of 300 μC cm^{-2}. This sequence produced a lift-off pattern for the NW with widths ~50 nm, which was then transferred into metal (usually Al) of approximately 40 nm thickness.

Optical lithography was used to define the bond-pad regions in metal, aligned to the EBL patterns, but with a slight over-exposure. The complete metal pattern, i.e. NW/lead-in area/bond-pad patterns, was transferred into the doped Si layer using reactive ion etching in SF_6, using 30 sccm SF_6, with 10 sccm O_2, at a pressure of 100 mbar and a potential of 200 V. Trenches ~200 nm deep were etched using an etch time of 1 min, to isolate the NW from the gates. The samples were then passivated by thermal oxidation at 1000 °C for ~15 min, a process that grew ~10 nm oxide and depending on the initial NW width, reduced the Si core of the NW to an

estimated range ∼10–40 nm. For the device in figure 1(d), the width of the un-oxidized NW was 58 nm. Using the oxidized NW width of 77 nm from figure 1(d), this gives us an un-oxidized Si core ∼40 nm, ignoring non-uniformity in the oxide layer. For the scaled device in figure 1(e), the width of the un-oxidized NW was 54 nm. This device was oxidized to a greater extent, and the oxidized NW width was 115 nm. This left a nominal un-oxidized Si core of only ∼5 nm.

The devices used ohmic contacts, formed by evaporation of 20 nm Cr/200 nm Al layers. These were defined by optical lithography using the same mask as for the bond pads, but with a slight under-exposure to ensure that contact was made only to the doped silicon. The contacts also formed the device bond pads. SETs were arranged as groups of four within a 100 μm square field, and connected to 12 bond pad regions surrounding the field. Finally, all the bond pads were bonded using Au wire in a small dual-in-line package, which could be inserted in a cryostat for electrical measurement.

4. Experimental results

Drain–source current (I_{ds}) versus drain–source voltage (V_{ds}) and gate–source voltage (V_{gs}) electrical measurements were performed on both 1 μm NW and point-gate devices. We first report the characteristics of the 1 μm NW SET and then the characteristics of the point-gate SET. In the latter case, a transition occurs to QD operation.

Figure 2(a) shows the I_{ds} versus V_{ds}, V_{gs} characteristics of the 1 μm NW device at 8 K. Here, a low current 'Coulomb blockade' region [40] is observed with a width varying from ∼±3 to ±5.5 V. This very wide Coulomb gap is indicative of the formation of an MTJ along the NW [13, 31]. I_{ds} versus V_{ds} characteristics are shown in figure 2(b) with curves offset from each other in I_{ds} for clarity. $\log|I_{ds}|$ versus V_{ds} are shown in figure 2(c).

Figure 2(a) shows SE oscillations [40] in I_{ds} (e.g. along the line $V_{ds} = -7$ V) as V_{gs} is swept from 0 to 30 V, with a period ∼3.75 V. While the Coulomb gap cannot be reduced to zero, triangular regions corresponding to half-Coulomb diamonds are observed outside the central region. This implies an effective SE gate capacitance $C_g \approx \frac{e}{\Delta V_{gs}} = 0.043$ aF. The very small value of C_g is due to the wide NW-gate spacing in this device.

The temperature dependence of the $\log|I_{ds}|$ versus V_{ds} characteristics of the device of figure 2, from 8 to 300 K, is shown in figure 3(a). For clarity the curves at each temperature are shown offset by 0.1 nA per temperature step. Figures 3(b) and (c) show the data using a linear scale, with different limits to emphasize features at low/high temperature. These show a current staircase and low current Coulomb blockade regions at low temperatures <220 K. At higher temperatures, a non-linearity corresponding to the Coulomb gap persists, but is overcome progressively by thermal fluctuations. However, traces of the non-linearity persist even at 280 K (figure 3(c), dotted arrow). Figure 3(d) shows an Arrhenius plot of $\ln|I_{ds}|$ versus inverse temperature T^{-1} for the data, at $V_{ds} = 0.075$ V, and $V_{ds} = 0.5$ to 5 V in 0.5 V steps. For low $V_{ds} = 0.075$ V, a thermally activated current region is observed above 200 K. For $T < 200$ K, only a weakly-temperature dependent current is observed. The later corresponds to a region where Coulomb blockade effects are significant. The slope of the Arrhenius plot in the thermally activated region ($T > 200$ K) can be used to extract the activation energy, $E_a = k_B \frac{\Delta \ln(I_{ds})}{\Delta T^{-1}}$. Figure 3(e) shows a linear fit to the data in the temperature range 200–300 K, for $V_{ds} = 0.075$ V. The slope of the fit can be used to extract $E_a = 0.276\ \mathrm{eV} \pm 1.8 \times 10^{-3}$ eV (i.e. ±0.66%).

Figure 4 shows room-temperature Coulomb blockade I_{ds} versus V_{ds}, V_{gs} characteristics from a second SET, with a 50 nm × 50 nm NW and a single point-gate. The nominal un-oxidized core in this device was only ∼5 nm. In the 3D plot shown in figure 4(a), a low-current Coulomb blockade region is seen with Coulomb gap width $\Delta V_c = e/C = 1$ V, where C is the total island capacitance. This implies $C = 0.16$ aF in the device. For larger values of V_{ds}, I_{ds} increases in a non-linear manner and traces of a current step are visible, e.g. at $V_{ds} \sim -1$ V in the I_{ds}–V_{ds} curve at $V_{gs} = 9$ V. Furthermore, a large current peak is observed in I_{ds} as V_{gs} increases, with a shift towards increasing values of V_{gs} as V_{ds} increases. Figure 4(b) shows I_{ds} versus V_{gs} as V_{ds} is increased from −5 V to +4.6 V in 0.4 V steps. These characteristics may be attributed to room-temperature SE charging of an isolated island along the NW, with charging energy $E_c = e^2/2C = 0.5\ \mathrm{eV} \gg k_b T = 26$ meV at 300 K. While multiple current peaks are not observed in this device within our V_{gs} range, the behaviour is similar to other reported work on room-temperature Si SETs using patterned islands [24, 29, 32], where only a few peaks, or even a single peak [24], has been observed. Finally, the possibility of drain voltage induced carrier depletion in a section of the NW near the drain is considered. While this 'classical' effect can lead to current saturation, the observation of a current peak is likely to require additional effects, e.g. SE effects or charge trapping near the channel. In figure 4, Coulomb blockade in the I_{ds}–V_{ds} curves (figure 4(a)) is observed in combination with the current peak in the I_{ds}–V_{gs} curves (figure 4(b)). This behaviour, coupled with the very small size of the SET Si core ∼5 nm, strongly supports a SE origin for these characteristics.

We now consider (figure 5) the electrical characteristics of the device of figure 2(d). In this third device, the NW length is ∼200 nm. The SET point-gate tips are however only ∼50 nm wide and this determines the length of the NW section which can be modulated. Figure 5(a) shows strong Coulomb staircases in the I_{ds} versus V_{ds}, V_{gs} characteristics at 8 K, as V_{gs} varies from 0 to 5 V. In comparison with the 1 μm NW device, the width of the Coulomb gap is strongly reduced, to between ∼±0.2 and ±0.8 V. This demonstrates that as the NW length is reduced, the number of islands in the MTJ is also reduced. A contour plot of $\log|I_{ds}|$ versus V_{ds}, V_{gs} is provided in figure 5(b). These characteristics show a complex structure with V_{gs}, creating current peaks/valleys (marked 1–9), some of which (3–9) are parallel to the V_{ds}

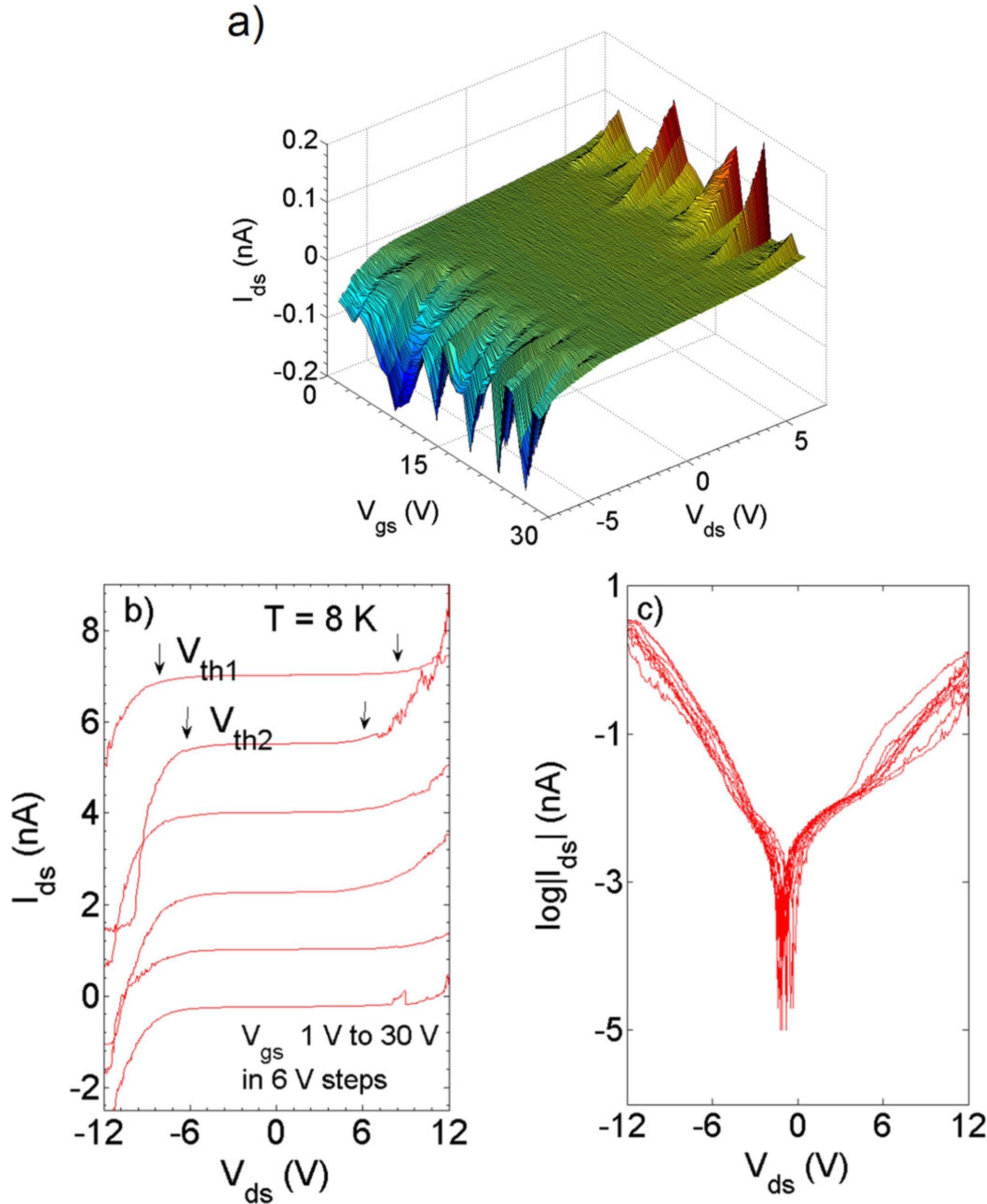

Figure 2. (a) I_{ds} versus V_{ds}, V_{gs} characteristics of a 1 μm NW device at 8 K. (b) Selected I_{ds} versus V_{ds} curves, offset by 6 V for each step in V_{gs}. Arrows mark the threshold voltage for current flow for positive and negative V_{ds}. V_{th1} and V_{th2} indicate the maximum and minimum range of threshold voltages. (c) log|I_{ds}| versus V_{ds} plot of the data in (a).

axis. For V_{gs} values from 0 to 1.5 V, Coulomb diamond characteristics can be seen. This region is shown in detail in figure 5(c) (3D plot) and (d) (contour plot), using drain–source conductance g_{ds} versus V_{ds}, V_{gs} characteristics extracted from the data of figure 5(b). Large and small Coulomb diamond regions can be observed (highlighted by white lines in figure 5(d)), centred at $V_{gs} \sim 0.6$ V and 0.125 V respectively. For $V_{gs} = 1.5$–5 V, the Coulomb gap modulation is relatively weak.

The current valley lines in figure 5(b) are arranged in groups, (group A: lines 1–2, group B: lines 3–5, group C: lines 6–8, and line 9). Lines 3–9 are parallel to the V_{ds} axis, implying that the underlying electron levels are decoupled from V_{ds}. In contrast, lines 1–2 begin at Coulomb diamonds and shift in position with both V_{ds} and V_{gs}, implying coupling to both drain and gate terminals.

As the NW length in this device is short ∼200 nm, with only ∼50 nm of this strongly coupled to the gate, the number of gated islands possible along the NW is limited. Furthermore, the observation of current lines in groups A–C may be associated with quantum confinement levels [41] in QDs formed in the NW.

Figure 6 shows the I_{ds} versus V_{ds} characteristics plotted on a linear (a) and log (b) scale, in the region of group B, as V_{gs} varies between 1.375 and 2.5 V in steps of 0.125 V. The Coulomb gap is 0.3 V wide and a regular multiple-step Coulomb staircase is seen. In the plot of log|I_{ds}| versus V_{ds} (figure 6(b)), the Coulomb staircase is very stable, and

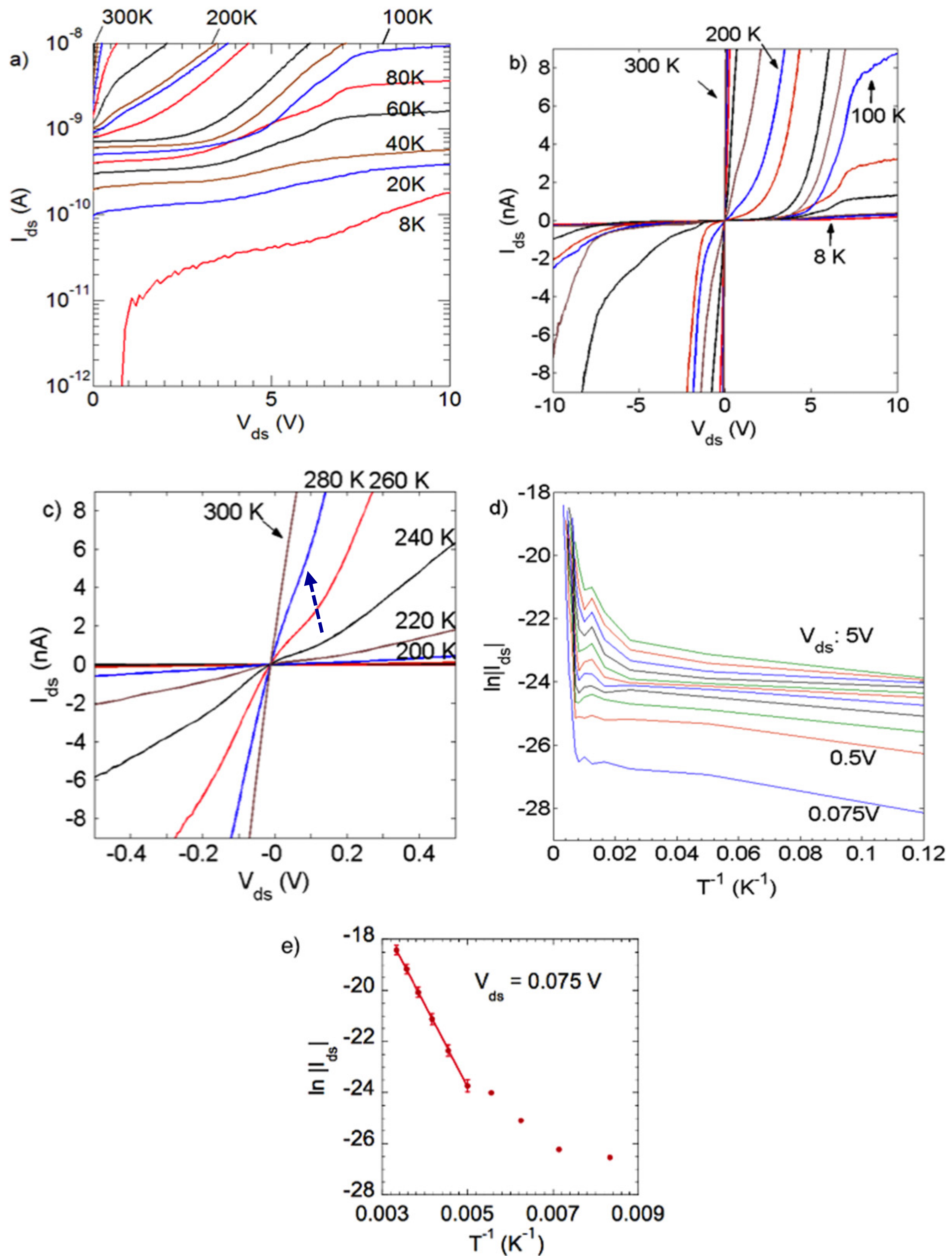

Figure 3. (a) Temperature dependence of $\log|I_{ds}|$ versus V_{ds} characteristics of a 1 μm long NW SET, from 8–300 K (curves offset by 0.1 nA for clarity). Temperature is varied in 20 K steps from 20 K to 300 K. (b) I_{ds} versus V_{ds} characteristics for the data of (a), from 8–300 K. Range of V_{ds} is reduced from ±10 V (b) to ±0.5 V (c), to emphasize the high temperature regime in (c). (d) Arrhenius plots of $\ln|I_{ds}|$ versus T^{-1}, as V_{ds} is varied from 0.075 V to 5 V. V_{ds} varied in 0.5 V steps for $V_{ds} > 0.5$ V. (e) Linear fit (solid line) to Arrhenius plot of $\ln|I_{ds}|$ versus T^{-1}, for $V_{ds} = 0.075$ V for the data from 200–300 K. Error bars represent 1% error. $V_{gs} = 0$ V in all cases, (a)–(e).

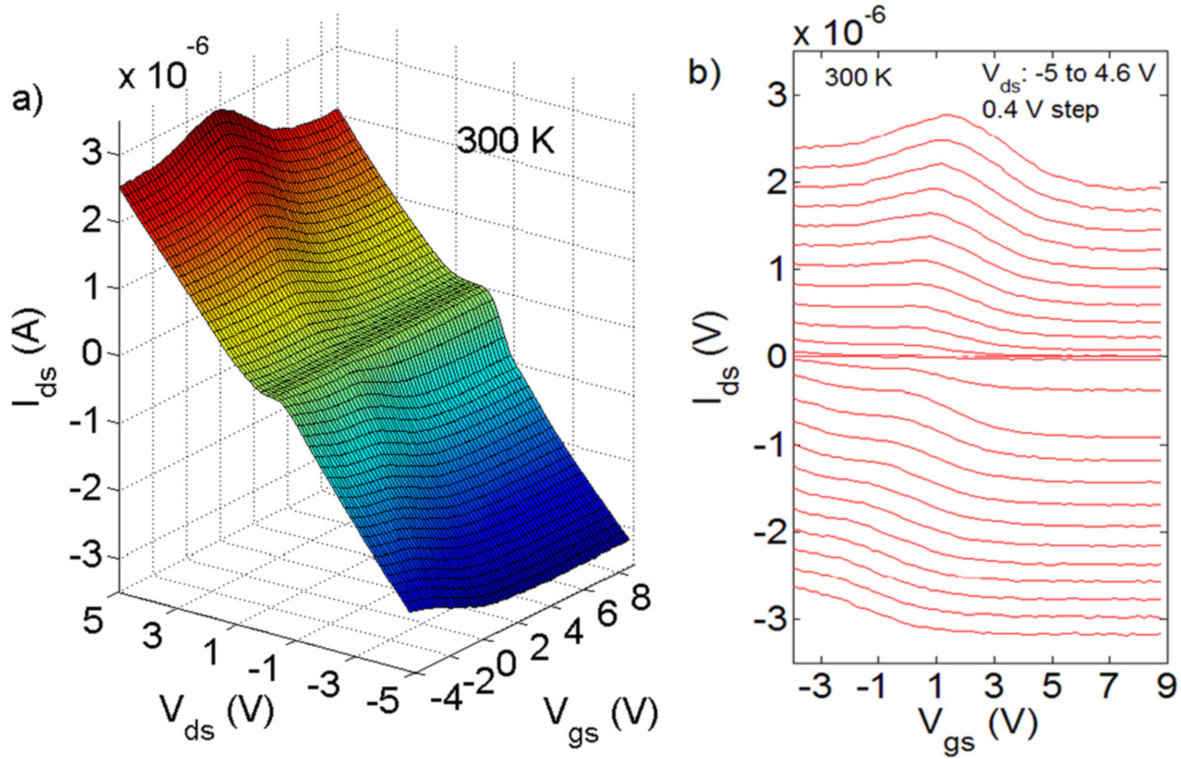

Figure 4. I_{ds} versus V_{ds}, V_{gs} characteristics for a 50 nm NW SET at 300 K. Single-electron operation is observed, with Coulomb blockade in the I_{ds}–V_{ds} characteristics and a single-electron oscillation in the I_{ds}–V_{gs} characteristics. (a) Three-dimensional plot and (b) I_{ds}–V_{gs} characteristics as V_{ds} is increased from −5 V to 4.6 V.

modulated between two distinct curves (*S1* and *S*2). Figure 6(c) shows SE oscillations in the I_{ds} versus V_{gs} characteristics for V_{ds} values from −0.9 to +0.9 V.

5. Discussion

The main features of the electrical characteristics of the short NW point-gate device of figure 5 are as follows:

(i) A strong multiple-step Coulomb staircase is seen, implying very different values of tunnel resistances coupling the island(s). The observation of a staircase with uniform step widths (figure 6(a)) reduces the likelihood of a many-island MTJ, where steps are weak or irregular.

(ii) The Coulomb gap is modulated by both V_{ds} and V_{gs} and two Coulomb diamonds are observed in the region $0\,V < V_{gs} < 1.5\,V$ (highlighted by white lines, figure 5(d)). Coulomb diamond 1 (centred at $V_{gs} \sim 0.125\,V$) is subsidiary and smaller than diamond 2 (centred at $V_{gs} \sim 0.6\,V$). This behaviour has been attributed theoretically to MTJs, e.g. two series, gate-coupled QDs can create major Coulomb diamonds with smaller, subsidiary diamonds intermediate to these [42]. Furthermore, as the Coulomb gap in figures 5(c) and (d) cannot be reduced to zero, there may be a third QD, decoupled from the gate. This may be contrasted with SETs with a single QD, where the Coulomb diamonds can be suppressed by increasing gate voltage, due to an increasing channel current or a reduction in tunnel barrier resistance, such that the QD becomes delocalized [11, 36]. For the region $1.5\,V < V_{gs} < 5\,V$, there are only small variations in the Coulomb gap width.

(iii) When $V_{gs} > 1.5\,V$ the edge of the Coulomb gap and the position of the current steps in I_{ds} versus V_{ds} occurs at approximately the same value of V_{ds}. This implies that in this range of V_{gs}, the corresponding charging island couples strongly to V_{ds} and only weakly to V_{gs}.

(iv) Lines 1 and 2 begin at Coulomb diamonds and shift diagonally across the plot, implying electrostatic coupling to both V_{ds} and V_{gs}.

(v) Lines 3–9 are almost parallel to the V_{ds} axis, implying that the corresponding energy levels couple strongly to V_{gs} and only very weakly to V_{ds}. Furthermore, these lines exist in groups (3–5, 6–8) with a small line spacing within a group and a wider spacing between groups. This resembles the energy spectrum of a QD including both charging and excited states [41].

(vi) Hexagonal regions of charge stability are not observed [43], precluding the possibility of electrostatically coupled QDs.

The patterns in figure 5 may be compared to those typically observed in QDs [44]. In particular, our observation of lines parallel to the V_{ds} axis (point (v)) is not typically seen in QDs. Furthermore, points (iii) and (v) are difficult to reconcile with a single QD, as the Coulomb gap would need

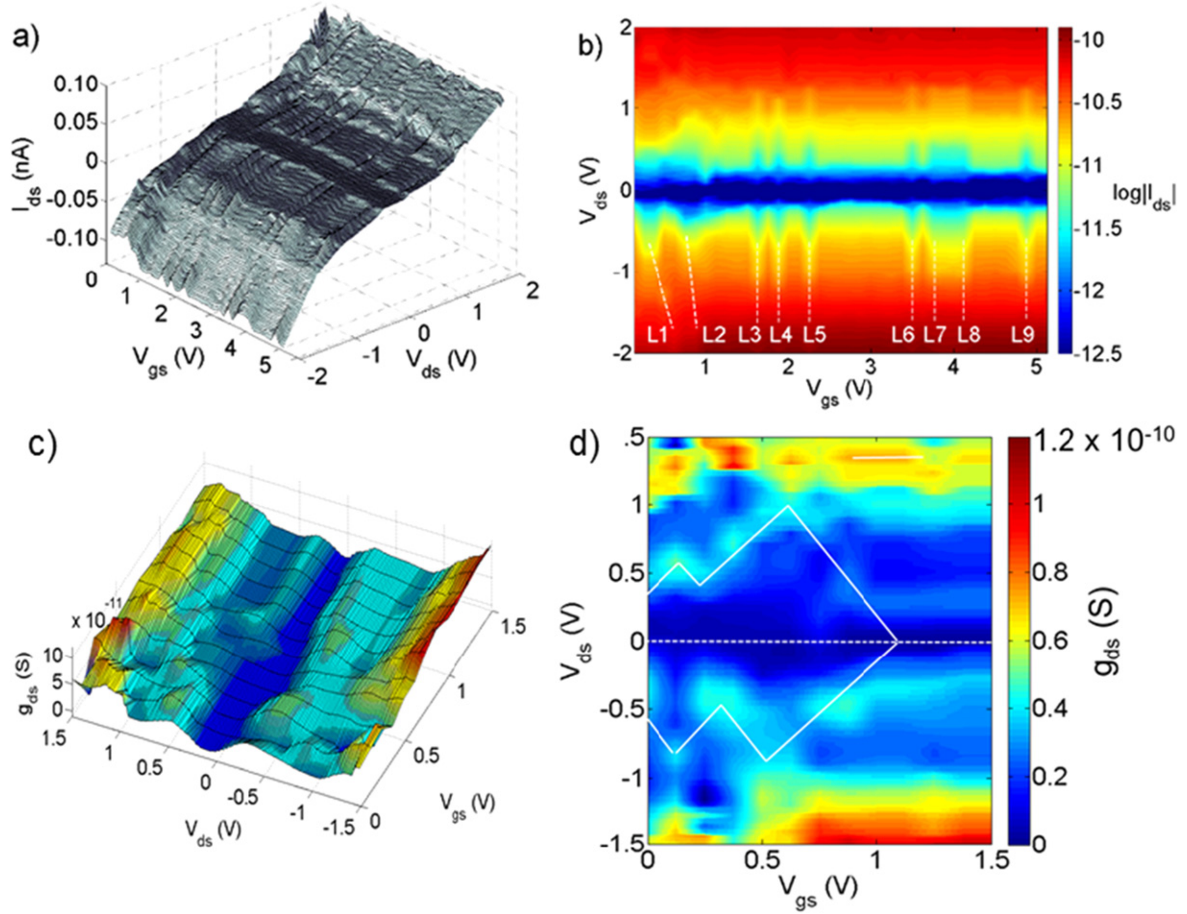

Figure 5. (a) I_{ds} versus V_{ds}, V_{gs} characteristics of a point-gate SET at 8 K. Data obtained using 201 point I_{ds}–V_{ds} curves, for 41 separate values of V_{gs}. (b) log|I_{ds}| versus V_{ds}, V_{gs}. Features labelled *L*1–*L*9 are associated with QD energy levels. (c),(d) Coulomb diamond g_{ds} versus V_{ds}, V_{gs} characteristics for $V_{gs} < 1.5$ V shown as a three-dimensional (c) and contour (d) plot.

to couple only to V_{ds} for point (iii), and lines 3–8 would need to couple only to V_{gs} for point (v). However, it is possible to explain the characteristics using a model based on at least two QDs, where one QD couples strongly to the source, but not to the gate, and another QD couples strongly to the gate, but only weakly to the source. Decoupling of a QD from the source electrode, by a strong intermediate potential barrier has been observed previously in SE transfer devices [45].

We investigate the characteristics of figure 5 further by considering a circuit configuration of three independent QDs (figure 7(a)). QD0 is decoupled from the gate and this prevents V_{gs} reducing the Coulomb gap completely to zero. QD1 tunnel couples to intermediate sections of the NW and is coupled capacitively by C_{g1} to V_g. QD2 tunnel couples to an intermediate NW section and to the drain, and is coupled capacitively by C_{g2} to V_g. As we do not observe hexagonal charge stability regions in figure 5(b) [43], we do not consider direct electrostatic or tunnel coupling between QD1 and QD2. Applying V_{ds} pulls the Coulomb gaps in the QDs down relative to the source Fermi energy E_{FS}. However, QD2 is separated by its left-hand side tunnel barrier and by QD0 and QD1 from the source. Assuming the majority of V_{ds} drops across QD0 and QD1, e.g. due to more resistive tunnel barriers, then this limits the shift in the potential of QD2 with V_{ds}.

The shape of the diamonds in figures 5(c) and (d) (point (ii), above), suggests that there are at least two gate coupled QDs (QD1 and QD2), and the persistence of a Coulomb gap at all values of V_{gs} suggests the presence of a third QD (QD0) decoupled from the gate. Therefore, the formation of large and small Coulomb diamonds can be attributed to QD1 and QD2.

The region $V_{gs} > 1.5$ V in figure 5(b) is now considered. As V_{gs} increases, the tunnel barrier potentials are pulled down relative to the Fermi energy [36]. For a distribution of tunnel barrier heights, likely in our un-patterned NWs, a QD with relatively low tunnel barrier height may then become de-isolated and no longer contribute to the Coulomb blockade. In the model of figure 7(a), if QD1 is de-isolated, then only QD0 and QD2 remain significant. Figure 7(b) shows the energy levels in QD0 and QD2 at $V_{ds} = 0$ V, where the presence of both Coulomb gaps (E_{C0} and E_{C2}) and quantum confinement levels (*a*–*c*, and α–γ) is assumed. Figure 7(c) shows the situation when E_{C0} is overcome by V_{ds} at $V_{gs} = V_{gs1}$. Level '*a*' aligns with E_{FS} and current can flow across the QDs. This corresponds to line 3 in figure 5(b). Increasing V_{ds} charges QD0 with electrons one by one, leading to a Coulomb staircase in the I_{ds}–V_{ds} characteristics.

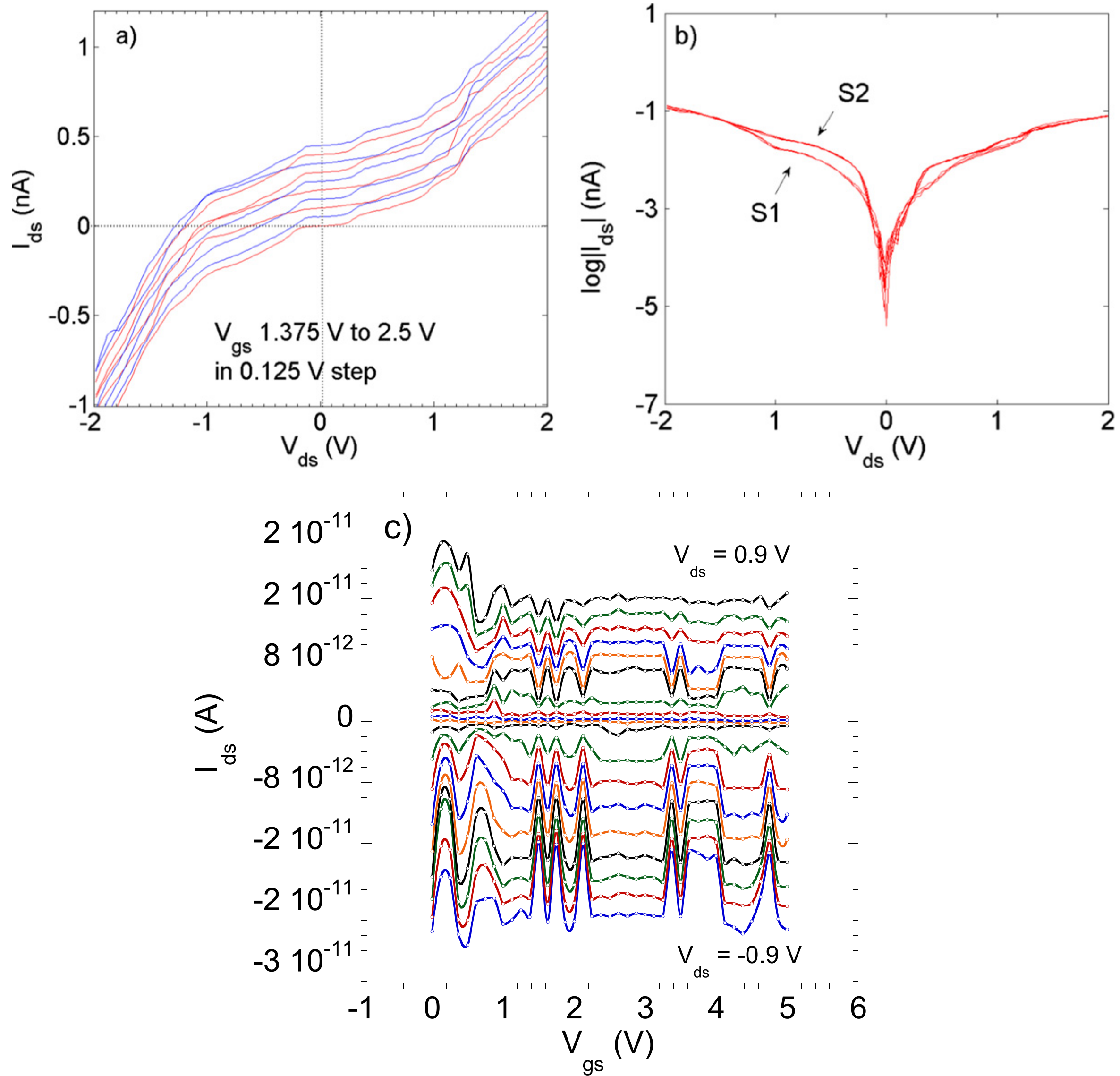

Figure 6. Source–drain characteristics, I_{ds} versus V_{ds}, of a 50 nm long nanowire SET, at 8 K (a) linear I_{ds} scale, (b) log|I_{ds}| scale showing the reproducibility of the characteristics. Curves are offset by 0.5 nA V^{-1} with V_{gs}. (c) Single-electron oscillations in the I_{ds} versus V_{gs} characteristics for V_{ds} values from −0.9 V to +0.9 V, extracted from the plot of figure 5(a). Here, circles show the data points and the curves are interpolated fits through the points.

When $V_{gs} > V_{gs1}$, energy levels α–γ are pulled down successively below level 'a' in QD0 and within the energy window E_{FS}–E_{FD}. Assuming the tunnelling rate for electrons leaving QD2 towards the drain is lower than for tunnelling onto QD2 from QD0, electrons can persist on QD2 and lead to a current valley [41]. This leads to lines 3–5 in figure 5(b). When V_{gs2} is reached, figure 7(d), QD2 charges by one electron, filling level 'α', and shifting levels β–γ to higher energies. As E_{C2} is greater than the energy level spacing ΔE, the separation between lines 5 and 6 is greater than between lines 4 and 5, creating the groups of lines seen in figure 5(b).

We now consider the possibility of stochastic tunnelling between charging levels on two QDs [46]. In this model, electrons tunnel across a junction intermediate to the two QDs, between ladders formed by charging states. Here, the corresponding conductance peaks can be grouped, with equal spacing within groups. As we observe unequal spacing between lines within both group 1 and 2 (figure 5(b)), this suggests that the origin of the lines includes both charging and quantum confinement. However, in the stochastic tunnelling model, the QDs are tunnel coupled, which would lead to the formation of hexagonal charge stability regions. As we do not observe this in figure 5, a model with independent QDs lying at different points along the NW is more likely.

Finally, we discuss the formation of islands along the MTJ. Following the final oxidation stage for passivation, the Si core width of the NW is estimated to be ~30–40 nm. In these NWs, roughness of the SiO_2/Si interface, in combination with disorder in the interface state density or doping concentration variation, can pinch-off sections of the NW and create a chain of tunnel barriers and conducting islands. In the 1 μm NW, the Coulomb gap is very large, in figure 2(a), as

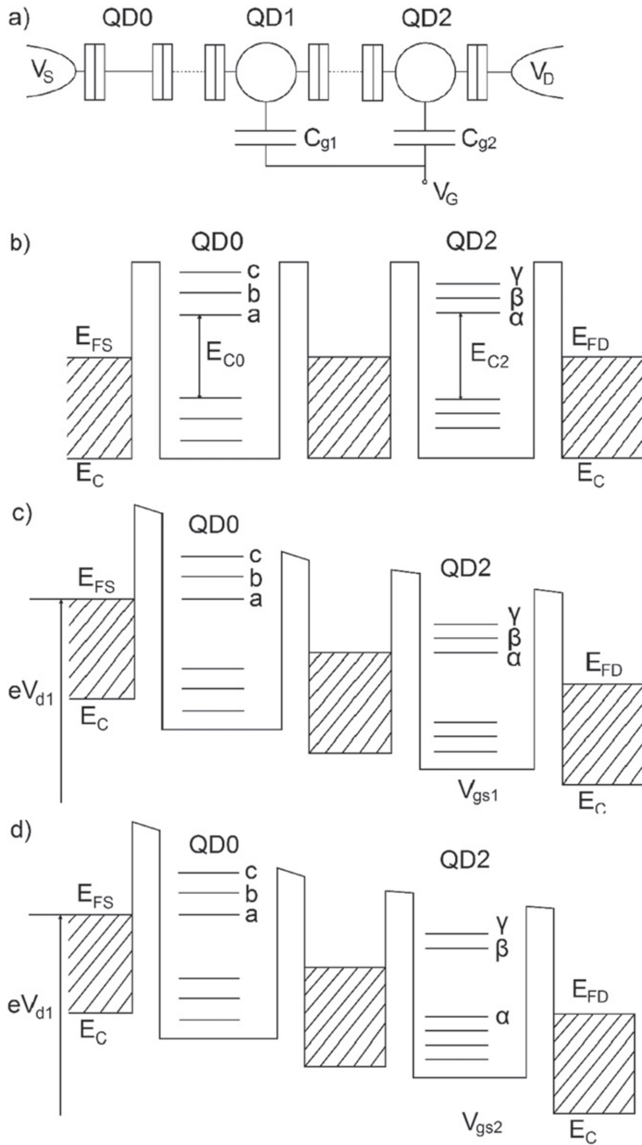

Figure 7. (a) Circuit diagram for the point-gate SET of figures 5 and 6. Schematic energy diagram for (b) $V_{ds} = 0$ V, (c) for $V_{ds} = V_{d1} > 0$ V and $V_{gs} = V_{gs1} > 0$ V and (d) for $V_{gs2} > V_{gs1}$.

this is a function of the combined charging energies of many islands along the NW. The Coulomb gap reduces with increasing temperature (figure 3), implying a variation in island size. Here, due to their smaller charging energies, thermally activated currents overcome SE effects in the larger islands first. The maximum temperature for SE effects is determined, either by the size of the smallest island and/or by the heights of the tunnel barriers.

6. Device simulation

The electical characteristics of our devices have been investigated further, using a SE Monte Carlo simulation. This simulation is based on SE effects only and does not include quantum confinement effects. The general simulation circuit (figure 8(a)) uses an MTJ formed by an array of tunnel

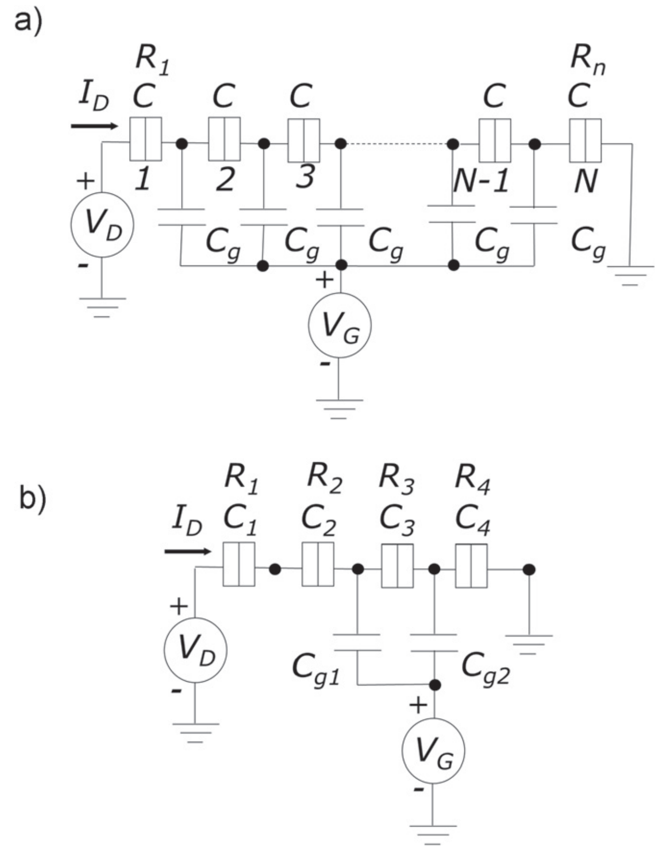

Figure 8. (a) General circuit diagram for single-electron Monte Carlo simulations. (b) Circuit diagram with three quantum dots.

capacitors C_n, with the 'island' regions coupled by gate capacitance C_g to the gate voltage. The tunnel resistances may be varied to create a Coulomb staircase rather than a linear increase in current outside the Coulomb gap.

We model the SE behaviour of the point-gate device characteristics of figures 5(c) and (d), ignoring quantum confinement. The circuit uses three QDs, see figure 8(b). The tunnel barrier resistances and capacitances C_1–C_4, R_1–R_4 and C_{g1}–C_{g2} are adjusted to qualitatively explain the experimental characteritics of figures 5(c) and (d). As a strong Coulomb staircase is observed, un-equal tunnel resistances are necessary. Using $(C_1, R_1) = (C_2, R_2) = (0.6\ \text{aF}, 8\ \text{G}\Omega)$, $(C_3, R_3) = (0.2\ \text{aF}, 16\ \text{G}\Omega)$, $(C_4, R_4) = (0.2\ \text{aF}, 16\ \text{G}\Omega)$, and $(C_{g1}, C_{g2}) = (0.2\ \text{aF}, 0.08\ \text{aF})$, we obtain the Coulomb diamond plot shown in figure 9(b). Figure 9(c) shows the data as a 3D plot. Figure 9(a) repeats the experimental plot of figure 5(d) to allow comparison of the diamond shapes. The simulation characteristics show large and subsidary Coulomb diamonds (black dotted lines). Furthermore, features corresponding to charge stability regions ouside the central Coulomb blockade region, e.g. the region shown by the white dotted line in figure 9(b) are also seen in figure 9(a) (shown by the black dotted lines).

C_3, C_4 and C_{g2} (figure 8(b)) may be used to extract the charging energies of QD2, and hence estimate the energy level seperation ΔE in QD2. Using total capacitances $C_{T2} = C_3 + C_4 + C_{g2} = 0.48$ aF, we find the corresponding

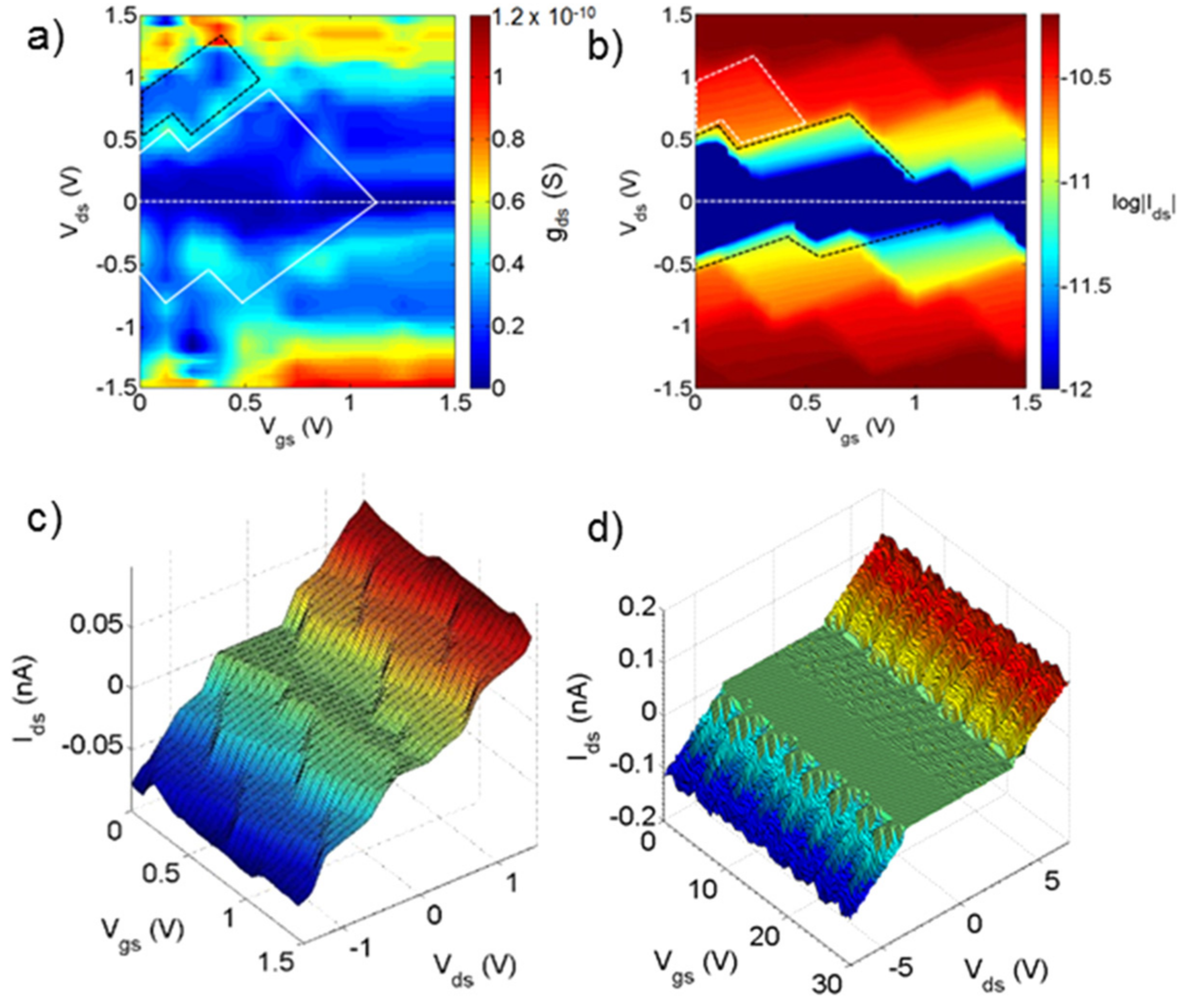

Figure 9. (a) Experimental Coulomb diamond g_{ds} versus V_{ds}, V_{gs} characteristics from figure 5(d). (b) Simulated I_{ds} versus V_{ds}, V_{gs} characteristics at 8 K, for the circuit of figure 8(b), excluding quantum confinement. (c) Three dimensional plot for the data in (b). (d) Simulated I_{ds} versus V_{ds}, V_{gs} characteristics at 8 K for the circuit of figure 8(a), with $n = 20$. C_{gn} is applied only for $n = 5$ to $n = 15$.

charging energy $E_{c2} = e^2/2C_{T2} = 0.16$ eV. Hence, the ratio of the line seperation, $\frac{L_4 - L_3}{L_6 - L_3} = \frac{\Delta E_1}{E_{c2}}$ gives us the energy level separation β–$\alpha = \Delta E_1 = 21$ meV. Similarly, the second energy level separation γ–$\beta = \Delta E_2 = 31$ meV.

The long MTJ SET is now simulated to explain qualitatively the electrical characteristics of figure 2(a). As both the short and long NW devices have the same NW width, it is assumed that the island capacitances are similar. We use a constant $C_n = 0.2$ aF, corresponding to the smaller capacitance value in the simulations of figures 9(a) and (b), and constant $C_{gn} = 0.0043$ aF. This corresponds to a total island capacitance $C_T = 2C + C_{gn} \approx 0.4$ aF, and a charging energy $E_C = \frac{e^2}{2C_T} = 0.2$ eV. E_c is in good agreement with the activation energy $E_a = 0.276$ eV, extracted from the Arrhenius plot of figure 4(c). The number of islands in the simulation is now increased to obtain a Coulomb gap ±3 to ±5.5 V wide. Figure 9(d) shows simulation results for an MTJ with $n = 20$, where the central 11 islands are coupled capacitively to the gate. The simulation shows a wide Coulomb gap, modulated along the edges, and oscillations in I_{ds} as V_{gs} is varied, in a manner similar to the experimental characteristics of figure 2(a). As a metallic island is assumed, we do not have the large modulation of I_{ds} outside the Coulomb gap observed in the experimental results of figure 2(a).

7. Conclusion

We conclude with a brief discussion of the significance of our results for the scaling of 'classical' SiNW FETs. The results show room-temperature Coulomb blockade and current oscillation in nominally uniform, heavily-doped un-patterned NWs, due to QDs inherently formed along the NW. Here, the SE charging energy $E_c = e^2/2C = 0.5\ \text{eV} \gg k_bT = 26$ meV at 300 K. While strong room temperature SE charging has been observed in MTJs formed by patterned NWs, our results show that these effects can persist at room temperature even in uniform NWs. Reduction of the NW width would reduce the size of the QDs and further increase their influence. QDs which are not coupled to the gate can also form in sections of the NW, creating a threshold voltage in the I_{ds}–V_{ds} curves. Furthermore, the gate and drain voltages needed to switch the drain on/off can be <0.5 V, implying that supply voltage

scaling to this range is possible. It is significant that as the NW length is scaled, SE and quantum confinement effects become much clearer, e.g. the characteristics of the 1 μm NW device of figure 2 may be compared to the point-gate device of figure 5. Features such as the Coulomb staircase and confinement levels are much clearer in the scaled device. This demonstrates that the influence of quantum confinement effects on the electrical characteristics is increasingly significant not only as the NW width, but also as the length in a SiNW FET is scaled.

In summary, the electrical characteristics of scaled SiNWs in the SE/quantum confinement limit have been investigated. Room-temperature SET operation was observed in short ~50 nm long NWs where the un-oxidized Si core was only ~5 nm. NWs with width ~30 nm and length 1 μm to ~50 nm, had in-plane parallel or point-gates. It was found that in the 1 μm long, uniform NWs, strong SE effects occurred up to ~220 K, and traces of these effects persisted to ~280 K. This was associated with the formation of a 'natural' 20-QD MTJ along the NW. The maximum island charging energy is $E_C = 0.2$ eV, with good agreement being found between this value and the activation energy extracted from Arrhenius plots. Scaling the NW gated length using a point-gate device reduced the number of QDs along the NW to only three and both SE and quantum confinement effects were observed in the electrical characteristics. Comparison between the 1 μm NW and the point-contact two-QD device showed that as the NW length was scaled, quantum effects dominated the electrical characteristics. The results illustrated the significance of quantum effects towards the limits of CMOS at the sub-10 nm scale, and the potential of short SiNWs for a quantum-effect 'beyond CMOS' technology.

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