

## NEMS Actuators by Sidewall Transfer Lithography

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The reduction of feature sizes in microsensors and actuators below the micron scale offers many advantages, including lowering of inertial mass, mechanical stiffness, thermal mass and thermal conductivity [1]. However, most processes for nanoscale pattern transfer (immersion lithography, E-beam lithography; nanoimprint lithography) are expensive, serial or slow. Here we demonstrate a wafer-scale parallel process for nanoelectromechanical systems (NEMS) based on sidewall transfer lithography (STL), a patterning method widely used to form nanoscale device features in microelectronics [2-6].

The STL NEMS fabrication process involves optical lithography, RF sputtering and deep reactive ion etching (DRIE) as shown in Fig. 1. Using a first mask, a Si substrate is patterned with photoresist to define a set of microscale features. The features are etched into mesas, and the resist is removed. The mesas are then conformally coated with a thin layer of material, which is removed from horizontal surfaces by sputter etching. Material remaining on vertical surfaces can then provide a sidewall mask for nanoscale features (for example, elastic suspension beams). Using a second mask, the Si substrate is patterned to define a further set of microscale features (for example, anchors). Both sets of features are then transferred into the substrate by DRIE, and then undercut for form suspended structures using isotropic plasma etching.

Demonstrator devices (single- and double-ended electrothermal actuators with elastic suspensions up to 1 mm in length) were fabricated in bulk Si. An initial pattern of photoresist lines with widths varying between 2  $\mu\text{m}$  and 30  $\mu\text{m}$  was formed using UV lithography, and etched into 0.5  $\mu\text{m}$  deep Si mesas using a STS ICP DRIE operating a cyclic process based on etching with  $\text{SF}_6/\text{O}_2$  and passivation with  $\text{C}_4\text{F}_8$ . The resist was stripped, and a conformal layer of Au with a Cr adhesion layer was deposited by RF sputtering. Horizontal surfaces of this layer were then sputter etched. A second pattern of anchors and 2  $\mu\text{m}$  wide cross beams was then formed in photoresist. The combined pattern was transferred into the Si by DRIE, and then undercut using isotropic  $\text{SF}_6$  etching. DRIE parameters were adjusted to eliminate grass formation (Fig. 2a) and to minimize scallop size to prevent erosion of the nanoscale suspension (Fig. 2b). Similarly, sputter deposition was optimized to minimize stress and prevent detachment of the sidewall mask (Fig. 2c). It was then possible to fabricate extremely deep (up to 4.5  $\mu\text{m}$ ), narrow (100 nm) structures, Fig. 3a), combined with microscale anchors (Fig. 3b) and crossbeams (Fig. 3c). Undercut of nanoscale features was rapid. However, much longer etch times were required to undercut crossbeams (Fig. 4a), and care was therefore needed to prevent sidewall erosion and excessive heating of suspended beams. However, with practice, single and double-ended structures could be released successfully (Fig. 4b). Small deformations of the released structure were observed (Fig. 4c), due to stresses in the sidewall layers. These stresses are assumed to represent a combination of intrinsic stress in the Cr and stress induced by thermal annealing of the Au during undercut, when the beams are no longer cooled vertically through the substrate. Verification of mechanical motion was carried using a piezoelectrically driven vibration stage, and maximum in-plane displacements of 10  $\mu\text{m}$  were achieved.

The STL process appears suitable for fabrication of movable NEMS with high aspect ratio ( $> 40 : 1$ ) suspensions. Inherent constraints are the constant width of all nanoscale features and the requirement that these follow polygonal perimeters. However, these restrictions are compensated by the low cost of process equipment and rapid parallel fabrication. Further compatible process steps are now being developed.

[1] H.G. Craighead, Science 390 (2002) 1532-1535.

[2] W.R. Hunter, T.C. Holloway, P.K. Chatterjee, A.F. Tasch, IEEE Electron. Dev. Lett. 2 (1981) 4-6.

[3] U. Hilleringmann, T. Vierigge, J.T. Horstmann, Microelectr. Engng. 53 (2000) 569-572.

[4] K.H. Chung, S.K. Sung, D.H. Kim et al. Jpn. J. Appl. Phys. 41 (2002) 4410-4414.

[5] Y.-K. Choi, T.-J. King, C. Hu, IEEE Trans. Electron Devices 49 (2002) 436-441.

[6] J.T. Horstmann, K.F. Gosser, Microelectr. Engng. 61-62 (2002) 601-605.

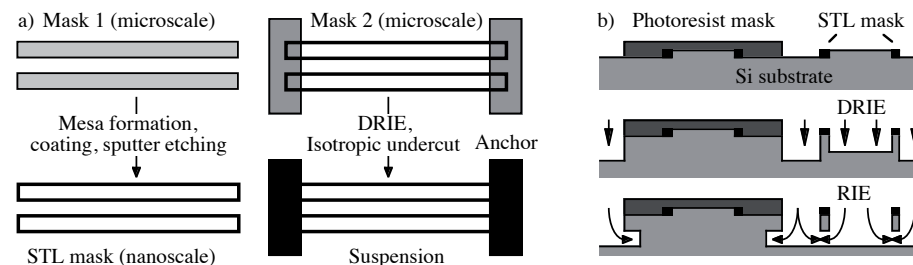


Fig. 1 a) plan and b) section views of STL NEMS fabrication process.

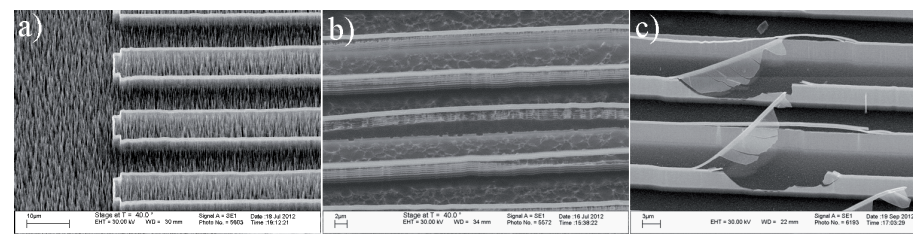


Fig. 2 a) Grass formation, b) sidewall erosion, and c) stress-induced detachment of sidewall mask.

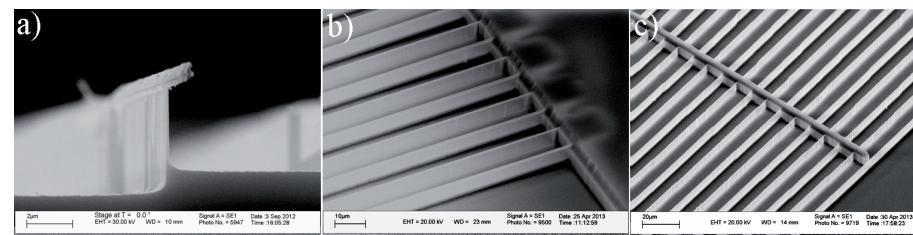


Fig. 3. a) Cleaved nanoscale beam before release; b) and c) beams attached to anchors and cross-beam.

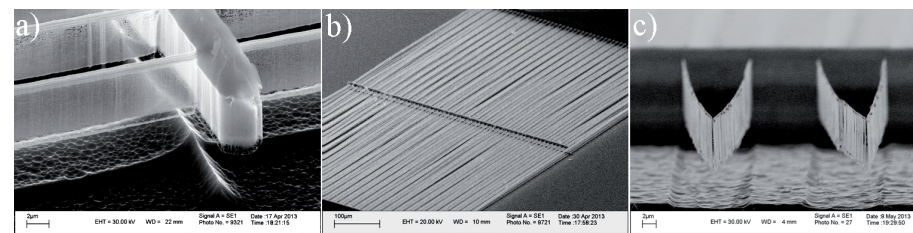


Fig. 4. a) Undercut suspension and b) complete device; c) minor stress effects in cleaved, undercut beams.