Integration of Self-Assembled Inductors with CMOS LC Oscillators

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***Abstract* — The quality factor (Q) of integrated inductors is of great importance to radio frequency applications. Monolithic integration of out-of-plane Au inductors with Complementary Metal-Oxide-Semiconductor (CMOS) LC oscillators is reported in this paper. The recently developed self-assembly process involves in-plane fabrication of Au inductors and subsequent rotation of the structure by surface tension forces of a melting Sn hinge. The CMOS compatibility of this process is demonstrated through the integration of an LC oscillator with the self-assembled inductor using post-CMOS processing. At a 1.48 GHz oscillation frequency, a phase noise of -95 dBc/Hz is reported at a 100 kHz frequency offset. Obtained results show this technique to be promising for the integration of high Q inductors with commercial RF systems.**

***Index Terms* — MEMS, RF oscillators, integrated inductors.**

I. Introduction

Inductors are essential components for radio frequency (RF) circuits. Numerous on-chip Q-improvement techniques have been developed, including micro-machining technologies developed to build RF micro-electro-mechanical systems (RF MEMS). Micro-machining techniques traditionally used to improve inductor Q involve [1], [2]:

(i) Thick metal electroplating to reduce the inductor series resistance (this is primarily used at 0.2 - 6 GHz);

(ii) Implementing 3D solenoid-type inductors to result in large-value designs suitable for 0.2 - 6 GHz;

(iii) Substrate etching underneath the inductor to reduce the parasitic capacitance to the substrate (suitable for 1-100 GHz);

(iv) Rotation of the inductor away from the substrate to reduce the parasitic coupling to the latter (suitable for 1-100 GHz).

In this paper we focus on the integration above CMOS of the self-assembled vertical inductor introduced in [3]. This involves in-plane inductor fabrication and subsequent rotation, using the surface tension forces of a melting hinge. Commercial exploitation of this technique has been limited by the lack of passivation capability required to prevent oxidation of Cu

The phase noise at a given offset of an LC oscillator is proportional to the $1/Q^2$ of the inductor employed. LC oscillators can therefore be used to directly evaluate the benefits of employing a MEMS inductor. Examples of MEMS inductors integrated with CMOS oscillators have been previously demonstrated by [5-8].

In this paper we present the integration of the self-assembled inductor proposed in [3, 4] with a complementary cross-coupled LC oscillator implemented in 0.18 um CMOS technology. We describe the fabrication process adopted for the inductor integration, as well as the design and layout of the LC oscillator. Final measurements are presented and compared to published results for LC oscillators with integrated MEMS inductors.

II. Design And Fabrication

For ease of comparison with previous work, the use of sophisticated designs was avoided, both for the oscillator and the inductor architecture. Thus, a complementary cross-coupled LC oscillator was designed, as shown in Fig. 1, and an RF MEMS meander geometry was adopted for the inductors.

The integration of the MEMS inductor has been performed on 5 mm X 5 mm dies fabricated as part of a Multi-Project-Wafer run in the UMC 0.18 um CMOS technology (6 metal layers, 1 poly layer).

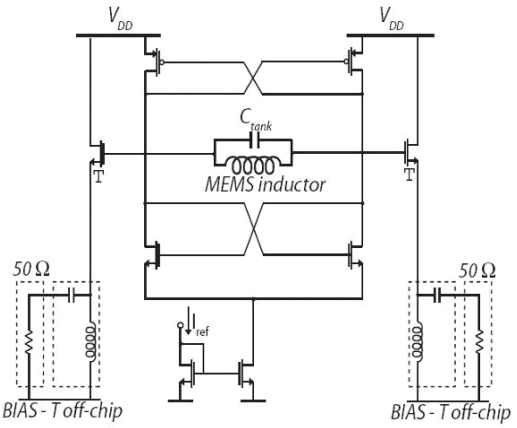

Fig. 1. Schematic of the complementary cross-coupled LC oscillator designed for integration with the MEMS inductor.

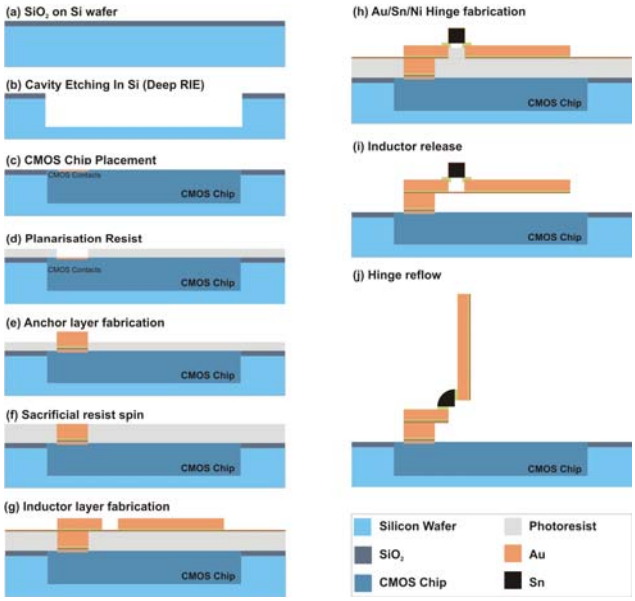

Fig. 2. Post-CMOS MEMS process flow using a carrier wafer.

The fabrication process for the MEMS inductors is summarized in Fig. 2. A carrier wafer is used, allowing post-processing of individual multi project wafer dies [9]. Commensurate cavities are etched by deep RIE (reactive ion etching) in an oxidized Si wafer to accommodate the dies. These are affixed into the cavities by a planarization photoresist layer. Au anchors are fabricated onto associated CMOS contacts by seed layer sputtering, photoresist patterning and electrodeposition of a 3.3 um thick Au layer. A sacrificial resist layer is then spun and patterned to allow the release of the coil structure from the substrate. Subsequently, the Au coil layer and a Sn hinge structure are fabricated with thicknesses 5.3 um and 10 um respectively. The sacrificial resist is stripped, releasing the Au coils and finally, the coil is rotated to the desired angle by reflowing the Sn hinge.

The layout of the oscillator designed for the MEMS inductor integration is shown in Fig. 3. Multiple oscillator structures were implemented on a single die and effort was put into achieving a common pad geometry in order to ease measurements. Probing was chosen as opposed to packaging in order to minimise capacitive loading of the high frequency oscillation signal.

The size of the pads used for dc and RF signals is 59 um x 59 um. The oscillator supply and output Ground-Signal-Ground (GSG) pads form a pi-like structure. Supply pads include dc current/voltage sources, ground and dc control signals. A separate dc pad is always dedicated to the supply of the ESD (electrostatic discharge) protection circuit, to be powered up prior to all other circuit supplies. The GSG output signal pads

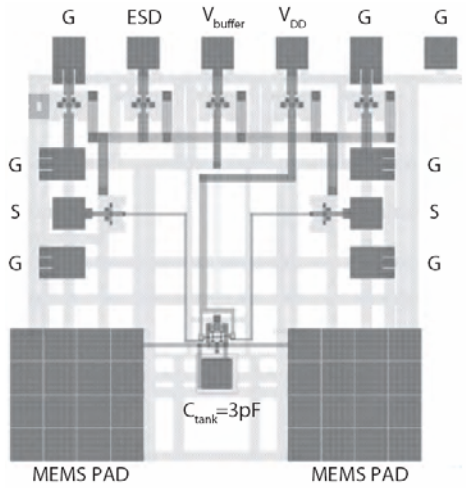

Fig. 3. Layout of oscillator to integrate RF MEMS inductor.

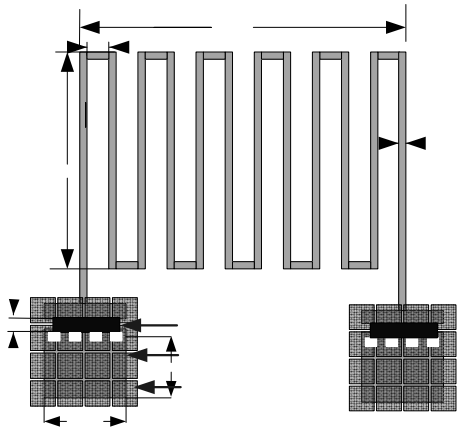

Fig. 4. MEMS meander inductor layout with pad 150 um X 200 um and track of 15 um on CMOS 4 X 4 arrays of pads.

are placed symmetrically at the sides of each oscillator, with a pitch of 100 um.

Finally, a 4 X 4 array of pads provides a large conductive area to electrically connect the MEMS inductor pads and the oscillator circuit. The layout of the MEMS inductor is shown in Fig. 4, where the pads, hinge and meander are shown with their dimensions. The inductor occupies a total area of 770 um X 800 um when in-plane.

III. MEASUREMENTS

An SEM image of an integrated inductor self-assembled at 30^{o} is shown in Fig. 5. The coil has rotated with respect to the CMOS die resulting in a large coil-circuit distance. This is beneficial to the Q of the inductor as it reduces parasitic effects through the conducting CMOS layers. The junctions between the inductor and the circuit can also be observed. A closer, top-view SEM image of the conducting MEMS – CMOS interface is shown in Fig. 6. The 4 X 4 array of CMOS pads allows easy

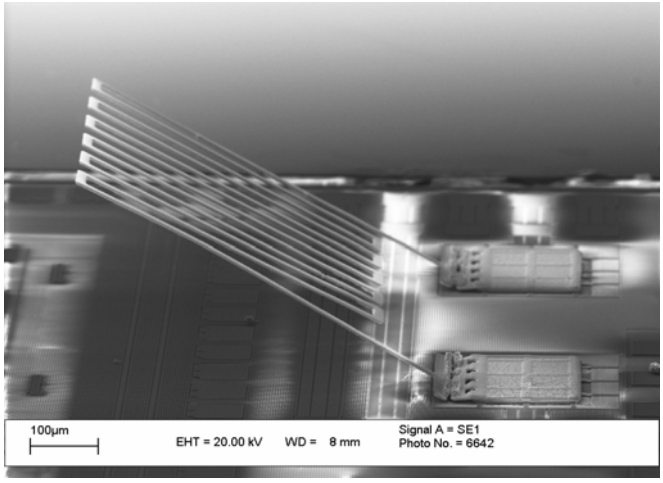

Fig. 5. SEM image of a MEMS inductor self-assembled at 30^o on a CMOS chip.

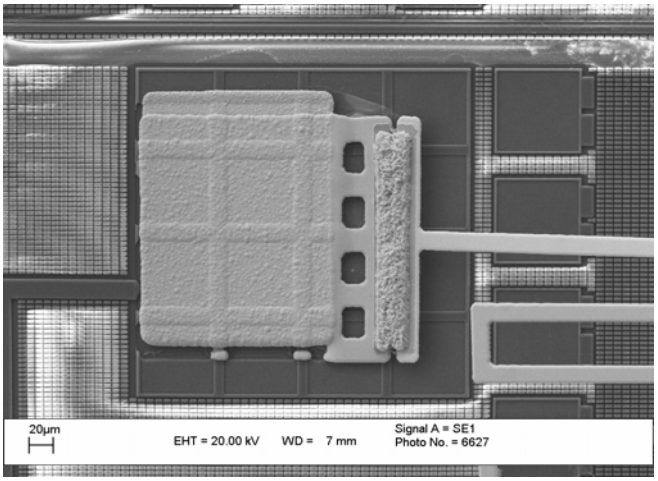

Fig. 6: SEM image of the electrical MEMS pad on CMOS 4x4 array of pads.

alignment and good conductivity. Contacts for dc probing are also visible on the right of the image, below the inductor track. The Au MEMS pad has been electrodeposited on top of the CMOS contact array. The array texture has propagated during electrodeposition to the surface of the pad.

The oscillator circuit in Fig. 1, with the integrated MEMS inductor rotated at a 30^o angle, was measured. An oscillation frequency of 1.48 GHz was obtained. The measured phase noise is plotted in Fig. 7. A value of -95 dBc/Hz was achieved at a 100 kHz offset for a -17 dBm output signal power. The oscillator draws a total of 6 mA from a 1.8 V supply. The oscillator measured results also demonstrate the CMOS compatibility of the proposed monolithic integration method.

III. DISCUSSION

To compare the overall oscillator performance to that of other works reported in the literature, knowledge of the inductor quality factor is required.

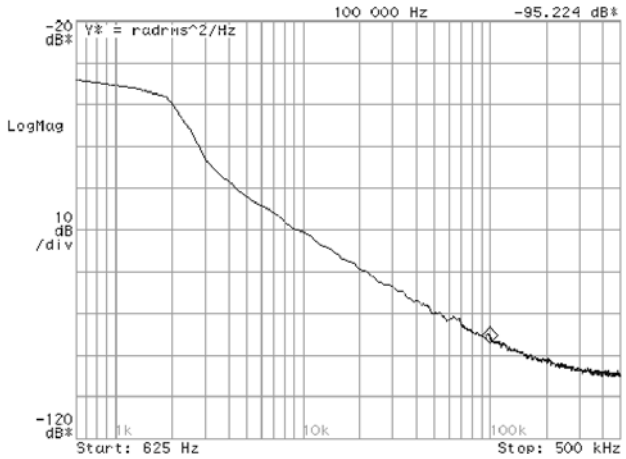

Fig. 7. Measured phase noise performance for an oscillator integrated with a MEMS inductor.

For this reason, the equivalent MEMS inductors fabricated on a SiO_2/Si substrate were characterised. A Q of 5 was observed around the 1.4 GHz oscillation frequency. The maximum Q was 10 at 5 GHz. Pad de-embedding analysis results in doubling of Q, revealing that the performance is limited by the pads' capacitance to the substrate. Since the same MEMS pads have been used for the integrated inductors, similar pad effects are expected for the inductor performance in the oscillators. Therefore, a value of Q = 5 is assumed.

To assess the performance of the oscillator the following figure of merit FOM_{ode} is employed [10], where *ode* stands for oscillator design efficiency.

$$FOM_{ode} = -10\log\left(\mathcal{L}(f_m)\right) + 10\log\left(\frac{kT}{2P_{DC}} \cdot \frac{1}{Q_u^2} \cdot \frac{f_{osc}^2}{f_m^2}\right)$$

P_{DC} denotes the power consumption of the oscillator. Q_u is the quality factor of the tank which in our case is approximately equal to that of the inductor. Finally, $\mathcal{L}(f_m)$ is the phase noise level evaluated at an offset frequency f_m away from the oscillation frequency f_{osc}.

FOM_{ode} is an absolute benchmark and assesses the feasibility of achieving a certain $\mathcal{L}(f_m)$ specification for a given power budget and technology (inductor Q factor). This entails comparing the achieved $\mathcal{L}(f_m)$ with an estimation of the minimum $\mathcal{L}(f_m)$ that could be achieved from a specific design.

Since FOM_{ode} measures efficiency, its value can range from 0 to 100 %, or alternatively from -∞ to 0 dB. State of the art

TABLE I

PERFORMANCE SUMMARY OF PUBLISHED OSCILLATORS WITH MEMS INTEGRATED INDUCTORS

Ref.	Turns	P_{DC}[a] [mW]	f_{osc} [GHz]	L [nH]	Q_L	$\mathcal{L}(f_m)$ [dBc/Hz]	f_m [kHz]	$P_{s,50}$ [dBm][b]	FOM_{ode}
This work	6	10.8	1.48	3.5-4[c]	5[c]	-115	1000	-17	-22.8
[5]	2.5	6.3	2.8	1.53	18.2	-121	600	NA	-19.5
[6]	2.5	3.75	5	1	30	-122	1000	0	-16.2
[7]	3.5	15	1	5	20	-124	300	0	-20.2
[8]	6	10-13	1.2	4	40	-110.9	100	-1.5	-27.6

[a] Power consumption of the oscillator core only.
[b] Output signal power on a 50Ω load.
[c] Values for a MEMS inductor developed over a passive silicon substrate with thick oxide layers.

oscillators reported in the literature range between 10% and 20% in design efficiency [10], i.e. have a FOM_{ode} between -10 dB and -20 dB.

Table 1 [11] reports recent published CMOS oscillators with integrated MEMS inductors, including the work presented. This is the first vertical self-assembled inductor reported in the literature to be integrated over a CMOS LC oscillator. Prior to this work, a self-assembled inductor (solenoid type) has been reported as used in the design of an LC oscillator in a bipolar process [8].

Since the phase noise level at the output of an oscillator is directly proportional to the output signal power, precise evaluation of FOM_{ode} should include the power consumption not only of the core of the oscillator, but of any output/amplifying stages leading to the reported output signal power. However, it is customary to account only for the oscillator core consumption when reporting the P_{DC} value.

Although this work appears to have lower FOM_{ode}, it should be considered that the output signal power for the design presented is ≈17 dBm lower than the average reported in published designs. Including an amplifying output stage in the circuit design would increase the output signal power and lead to a higher FOM_{ode} value.

IV. CONCLUSION

Successful fabrication and integration of the self-assembled inductor onto an LC oscillator circuit in a commercial CMOS technology was demonstrated. The self-assembly process developed for out-of-plane inductor fabrication has been shown to be CMOS compatible. A 1.48 GHz LC oscillator was designed and a phase noise of -95 dBc/Hz at 100 kHz offset was achieved. Measurements obtained from the integration of the CMOS LC oscillator with the proposed MEMS inductor suggest this to be a promising technique for achieving high performance, commercially viable RF integrated circuits.

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