MEMS Post-Processing of MPW Dies using BSOI Carrier Wafers

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ABSTRACT

Multi-project-wafer (MPW) services provide an economical route for prototyping of new electronic circuit designs. However, addition of MEMS functionality to MPW circuits by post-processing (also known as *MEMS-last* processing) is difficult and inefficient because MPW typically yields individual dies. One solution to this problem is to embed the MPW dies in a carrier wafer prior to MEMS processing. We have developed a process which allows 300 µm-thick CMOS dies to be embedded in a BSOI (bonded silicon-on-insulator) carrier prior to low-temperature processing for integration of metal MEMS. Deep reactive ion etching (DRIE) with an STS Multiplex ICP etcher is used to form cavities in the device layer of a BSOI wafer. By adjusting the passivation and etching cycles, the DRIE process has been optimized to produce near-vertical sidewalls when stopping on the buried oxide layer. The cavity sizes are closely matched to the die dimensions to ensure placement of the dies to within ±15 µm. Dies are placed in all the cavities, and then a photoresist layer is deposited by spin-coating and patterned to provide access to the required IC contact pads. The photoresist has the dual role of securing the dies and also planarizing the top surface of the carrier. After an appropriate baking cycle this layer provides a suitable base for multi-level electroplating or other low-temperature MEMS processing.

Key words: MEMS, CMOS, DRIE, BSOI, Die carrier

1. INTRODUCTON

MICROELECTROMECHANICAL systems (MEMS) are presently used in a variety of products for inertial sensing and optical signal processing. The range of applications is also expanding to include RF filters, mixers and switches, and biological sensors, among others. Monolithic integration of electronics (used for control, amplification, and/or signal processing) with MEMS, for improved micro-system performance and reliability, has long been a goal within the MEMS industry. Having the MEMS devices and electronic circuits on the same die reduces packaging complexity and improves reliability by minimizing the number of off-chip electrical connections. Monolithically integrating multiple sensors with electronics enables sensors measuring motion along different axes to be precisely aligned, to share data easily, to have greater accuracy, and to be less susceptible to external disturbance. Depending on the integration strategy that is adopted, there may be significant overall cost savings by co-fabricating or sequentially fabricating the microstructures and electronics on the same substrate. For the semiconductor industry, the integration of MEMS with electronics represents an opportunity to enhance the performance and/or functionality of integrated-circuit (IC) devices, for example by integrating high-Q passive components [1] to enable low-cost, low-power RF communications or by adding sensing and actuating capabilities.

There are three general approaches to integrating MEMS and CMOS. The MEMS fabrication can be done in a module that precedes the electronics module [2], the fabrication steps for the electronics and MEMS can be interleaved [3, 4], or the MEMS can be fabricated modularly after the electronics [5, 6]. Among these three approaches, the MEMS-last approach is particularly attractive because low-cost, state-of-the-art CMOS foundries can be employed. In this case, surface-micromachining processes must be developed that allow MEMS to be fabricated in a modular fashion on wafers with completed electronics. For researchers in universities, and for prototyping in general, it is also useful if methods are available for fabricating MEMS devices by post-processing of individual CMOS dies, as this means that the electronics can be manufactured economically through the use of multi-project-wafer (MPW) services. One approach that makes this possible is to embed MPW dies in a carrier wafer prior to MEMS processing.

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This paper presents low cost techniques for the fabrication of metal microstructures on MPW CMOS dies through the use of BSOI (bonded silicon-on-insulator) carrier wafers. The focus is on methods for achieving acceptable results while keeping costs to a minimum. Techniques for all the necessary process steps, including photolithography, electroplating, etching and release of MEMS structures, have been investigated and implemented. Die-level processing has also been conducted on CMOS dies fabricated through a commercial 180 nm foundry service offered by UMC. On these dies, post-processing has been used to realize metallic structures directly on top of the integrated circuit contact pads. Such structures represent the first step towards multi-level MEMS with monolithically integrated electronics.

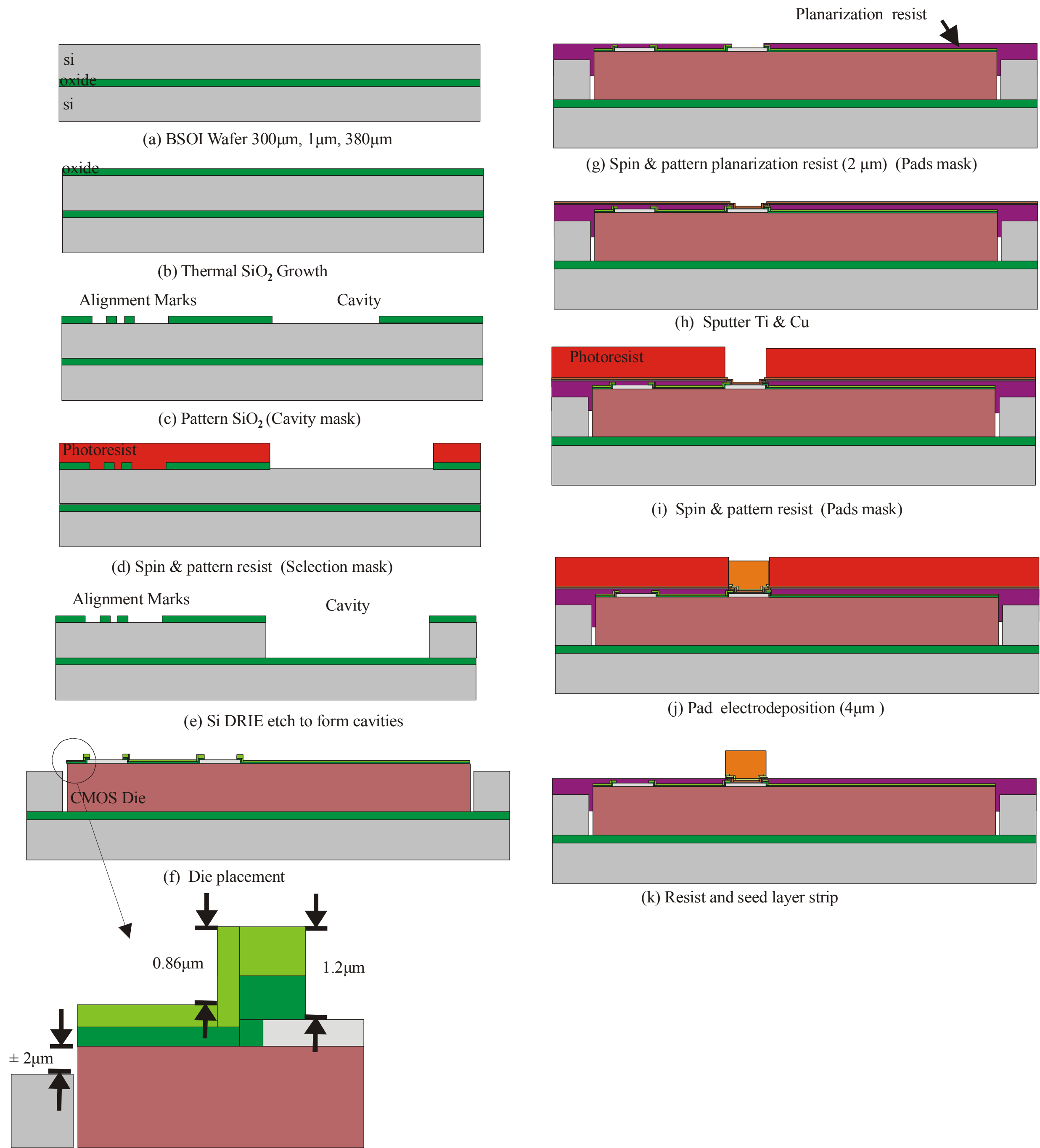

Figure 1. Die carrier process flow.

2. DIE CARRIER PROCESS

The use of a die carrier makes it possible to embed different types of CMOS dies for MEMS processing. This approach allows heterogeneous integration, independent of the wafer size. The process described here uses a 100 mm-dia. BSOI starting wafer, comprising a 300 µm-thick device layer and a 380 µm-thick handle layer separated by 1 µm of buried SiO_2. The die carrier process consists of various steps as given in Figure 1.

Multiple procedures can be performed on CMOS dies, such as photolithography, deep reactive ion etching, material deposition, metal electroplating. However, there are several key points that must be carefully considered when performing these process steps to insure proper operation of the CMOS circuitry:

• the process must be compatible with CMOS technology, implying (a) low temperature and (b) minimal contamination;
• the carrier wafer must be able to protect specific die areas and features from etching solutions.

In this research the UMC foundry service was used for CMOS die fabrication. A 0.18 micron silicided CMOS process was chosen, with 6 available metal layers, 1 poly layer, and a high resistance layer. Stacked contacts are supported, as are MIM capacitors (metal 5 to metal 6, 3 pF total capacitance, 55 x 55 μm^2 area). The process is for 1.8 volt bias applications, although 2.5 volt thick transistors are also available. The dies fabricated were 5120 x 5120 x 284 μm^3 in size, and carried a number of different voltage controlled oscillators for operation up to 5 GHz, the long term aim being to integrate low-loss MEMS inductors with these circuits. Trial experiments were performed on 5110 x 5110 x 297 μm^3 dummy dies to gain some insight into the post-processing steps and to work out some critical issues involved with these steps.

2.1 Deep reactive ion etching

The die carrier process starts with the thermal growth of a 200 nm-thick low-stress silicon dioxide film. This oxide is patterned with a cavity mask to define alignment markers and apertures corresponding to the cavities. In this work the apertures were arranged into 9 identical blocks, with each block containing 9 apertures with varying sizes around the actual die size. By etching a test wafer, the appropriate aperture size for the dies could be identified. The criterion used was that there should be a clearance of 10-15 µm on all sides of the die. For subsequent wafers, a second lithography step was performed using a selection mask (Figure 2b), leaving all apertures other than the correctly sized ones covered by photoresist. The next step is to make the appropriate cavities on the carrier wafer. The ability to microfabricate deep trenches in silicon substrates while maintaining high selectivity to masking material, good profile control and uniformity across wafer has been revolutionized with the current generation of deep-reactive-ion-etching (DRIE) tools. These deep-silicon etching machines can achieve etching rates in excess of 3 μm per min, selectivities to photomasking materials greater than 70:1, excellent profile control and non uniformities across the wafer of 5% or less [7, 8].

Figure 2. Designs for (a) cavity mask, and (b) selection mask for 5140 µm cavity.

The DRIE process used in this work, known as time-multiplexed deep etching (TMDE), offers the advantage of the high silicon etching rate of fluorinated chemistries such as SF_6. In the time-multiplexing scheme, the etching and passivating gases used are applied independently, one at a time, as shown in Figure 3, and the machine alternates between an etching cycle and a passivation cycle. During the etch cycle, exposed silicon is etched in an isotropic fashion, as is typical for fluorine-rich glow discharges. The typical duration of this step is 12 seconds. During the passivation cycle, a protective fluorocarbon film is deposited on all surfaces. The duration of this step is usually 10s and shorter than the etching cycle. In the subsequent etch cycle, ion bombardment promotes the preferential removal of the passivation film from all horizontal surfaces, causing the profile to evolve in a highly anisotropic fashion. This separation of etching and passivating cycles is also known as the Bosch process.

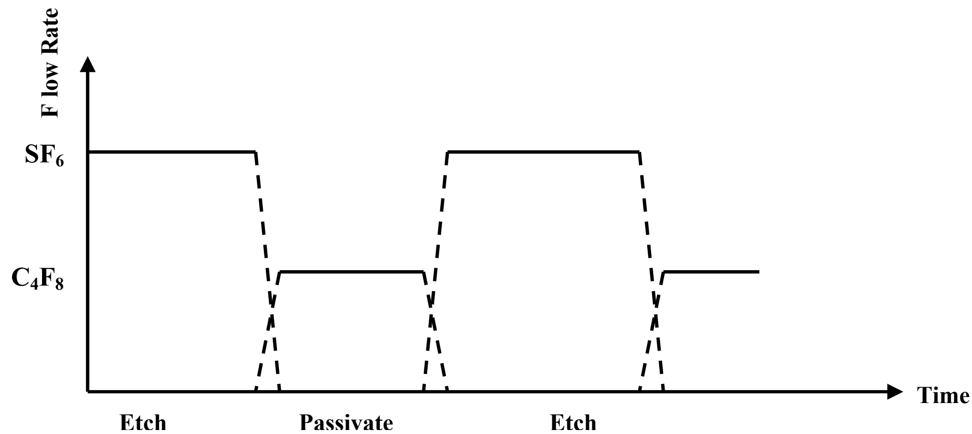

Figure3. During TMDE a single gas species at a time is flowed into the reactor, first SF_6 for etching and subsequently C_4F_8 for sidewall passivation. The overlap between the etching and passivating cycles originates in the finite time response of the mass flow controllers. Typically the durations of the etching and passivating cycles are 12s and 10s, respectively [7].

A process of the type illustrated in Figure 3, implemented on an STS Multiplex ICP etcher, was used to form the cavities in the device layer of the BSOI carrier wafer.

2.2 Die embedding on carrier wafer

Having formed the cavities, the next task is to place the dies and secure them in place. In this work, die placement was done manually with the aid of tweezers. A thin layer of photoresist (PR) was then spin-coated over the carrier, and patterned to open windows down to selected contact pads. This layer served the dual role of planarizing the top surface and fixing the dies in place.

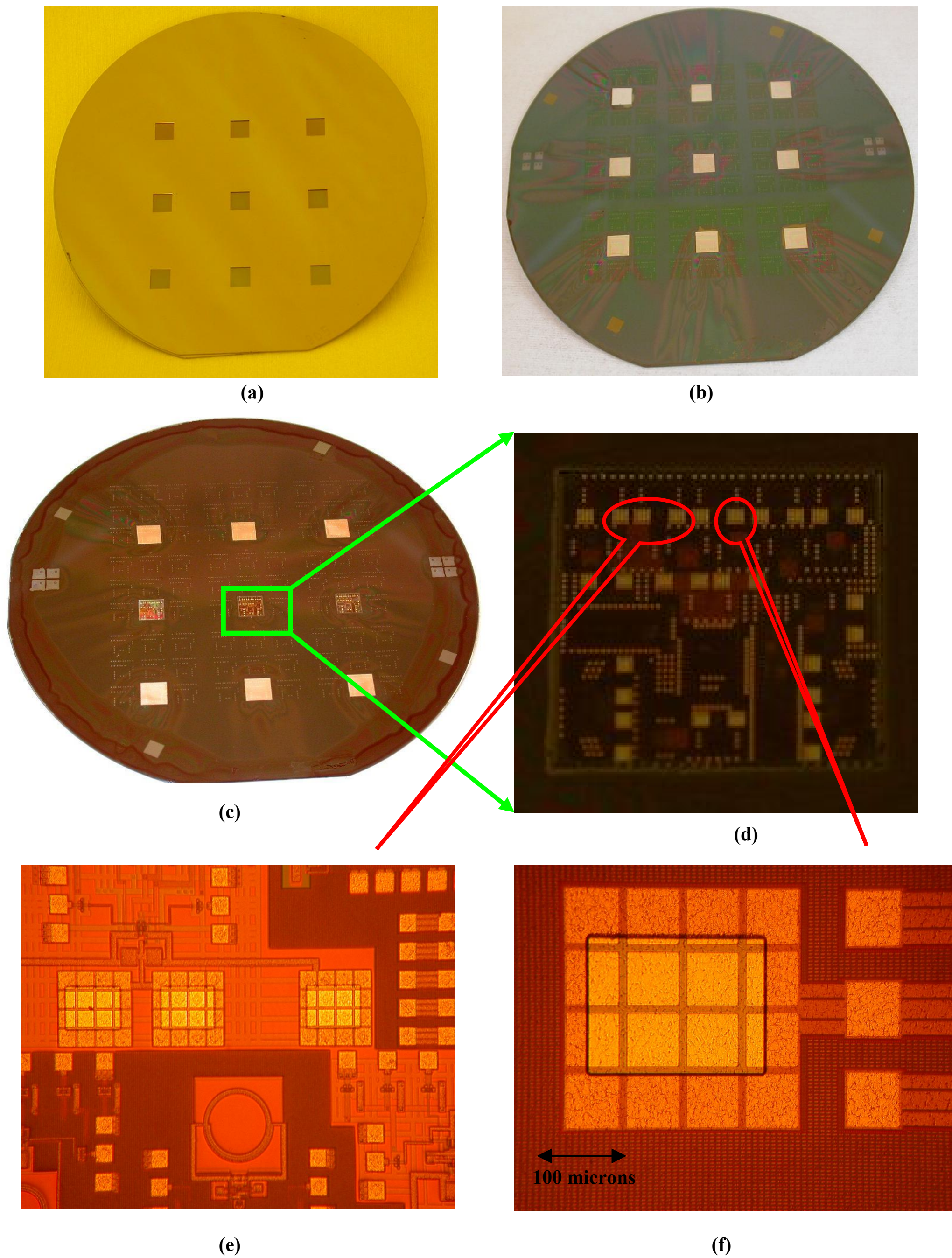

Figure 4. (a) Carrier wafer with cavities; (b) carrier wafer with embedded dummy dies; (c) carrier wafer with embedded UMC dies; (d) –(f) magnified views of central die of (c).

Normally when PR is spin-coated onto a large uniform surface such as a full wafer, good layer thickness uniformity is readily achieved. However, when spin-coating over embedded dies, poor uniformity of the PR layer on the die surface can be an issue. Initial attempts to pattern the planarization layers on carriers with embedded dummy dies yielded poor results, and on investigation it was found that the PR layer was not uniform across the carrier surface. The discontinuities in the surface height surface at the edges of the dies, in combination with the rheological properties of the resist, were causing the PR layer thickness to be increased at the die corners. This thickness variation is undesirable because it makes both patterning of the planarization layer itself and subsequent MEMS processing steps more difficult. It was found that the effect could be significantly reduced by using very low viscosity PR, such as Shipley S1805, deposited at a low spin speed (e.g. 500 rpm). This approach yielded much better uniformity across the die and the PR could be effectively patterned with adequate consistency. Another approach, which was not attempted in this work, would be to use a spray-on PR layer for planarization.

Figure 4 illustrates the various stages in the embedding and planarization process. Figure 4a shows a carrier wafer with cavity size of 5140 µm x 5140 µm, while Figure 4b shows the same carrier after embedding of dummy dies and planarization with Shipley S1828 photoresist spun at 500 rpm for 40 seconds. Some colour variation in the planarization layer, due to the presence of the embedded dies, can be seen in this image Figure 4c shows a carrier wafer containing a mixture of dummy and UMC dies, embedded with planarization resist. Finally, Figures 4d – 4f show magnified views of the central die on the carrier of Figure 4c. In the latter two images, the 200 µm x 150 µm openings in the planarization layer that provide access to the underlying 250 µm x 250 µm contact pads of the UMC chip are visible. These apertures allow electrical and mechanical connection to be made between the MEMS device and the electronic circuit. Figure 5 shows surface profile measurements for an embedded die, before and after spinning of the planarization layer. Note that the cavity is several µm deeper than the die thickness in this case. The large spikes to the right are measurement artefacts.

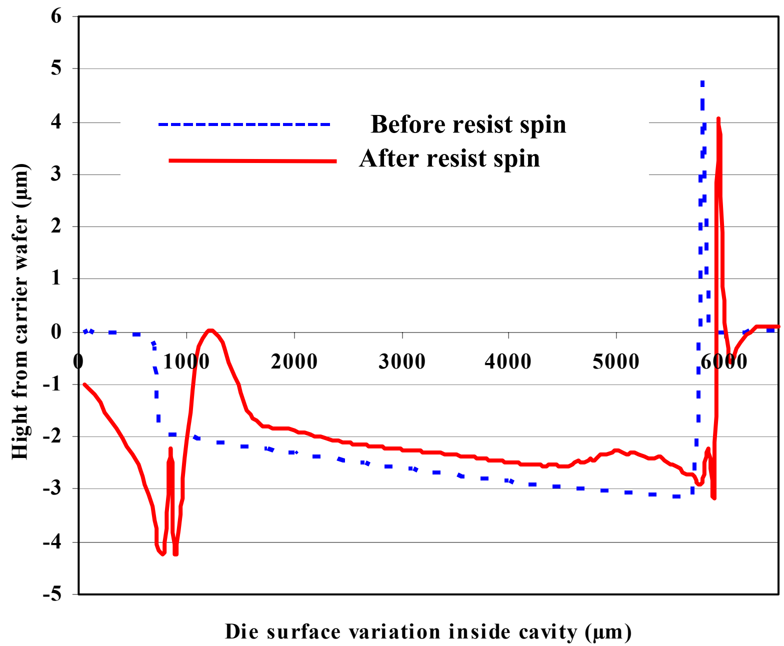

Figure 5. Surface profile measurements on embedded die.

2.3 Seed layer deposition

In standard CMOS fabrication, thin film deposition is the procedure by which various layers of conductive and insulating materials are deposited onto the surface of a silicon wafer. There are two major types of deposition, physical vapour deposition and chemical vapour deposition.

Physical vapour deposition (PVD) is capable of depositing many materials. A target made from the material to be deposited is placed in a chamber that is pumped down to vacuum; the material is then transformed into a gas phase by one of several methods. In this fashion, atoms of the source material are transferred to the target. It is necessary for the molecular species of the source material to be in a gaseous phase and there are three standard techniques utilized to create this condition: evaporation, sputtering, and ion beam deposition. PVD may be used to deposit most metals, insulators, and semiconductor films.

A key feature of each PVD technique is that, while the temperature of the source material is raised significantly, the temperature of the substrate is typically maintained at or near room temperature. A low substrate temperature is attractive for post-processing of CMOS dies, because it means that problems with diffusion and degradation of the CMOS metallisation can be avoided.

The alternative to physical vapour deposition is chemical vapour deposition (CVD). CVD is also used to deposit thin films onto a substrate from a gas phase. Several types of CVD are available: low pressure chemical vapour deposition, plasma-enhanced chemical vapour deposition, and photo chemical vapour deposition. All of these techniques generally raise the substrate temperature above 300 ºC, and this can cause problems for CMOS circuitry. Chemical vapour deposition techniques are favoured for the deposition of insulators and semiconductor materials in IC manufacturing due to the conformal nature of the deposition. However, due to the high temperature, relative complexity, and contamination issues that may arise with CVD, they are not so favourable for use in post-CMOS MEMS fabrication.

In this work it was necessary to deposit a conducting film over the planarization layer, which would act as a seed layer for electroplating. For the reasons discussed above, PVD was chosen as the deposition method for this film. A very thin (37 nm) layer of Ti was deposited for adhesion, followed by a 200 nm-thick layer of Cu. These were deposited by sputtering at 4×10^{-3} millibar pressure.

2.4 Gold electroplating

Gold films are being used increasingly in MEMS devices because of their excellent stability and low electrical resistivity. Applications for gold films include low loss RF MEMS devices [9], high performance electromagnetic MEMS mirrors [10], high reflectivity optical MEMS devices, etc.

In most cases, gold films are deposited either by PVD, electroless plating or electroplating using a seed layer. Compared to vacuum evaporation or sputtering, plating is more suitable for some three dimensional structures because it can cover hidden planes conformally. Gold electroplating is a cathodic electrochemical process, conducted in an electrolytic bath containing complexed gold ions. The item to be plated is suspended in the plating tank, and made into a cathode by connecting it to the negative output of a current source. Also suspended in the tank is an anode, which is connected to the positive output of the current supply. Under imposed bias (cathode sufficiently negative and anode sufficiently positive with respect to the plating solution), electrochemical reactions take place on the cathode and anode. Positive metal ions in the plating solution flow to the cathode and chemically reduce to metal deposited on its surface. At the same time, negative ions are transported to the anode and oxidized.

In this work gold pads were electroplated into photoresist moulds formed in AZ9260 photoresist. Gold was chosen because the ultimate goal is to realise low-loss RF MEMS components over CMOS. The mask used to define the mould was the same as that used to open the windows in the planarization layer, so that the plated pads were formed over the UMC contact pads. The resist mask was subsequently removed, leaving the plated metal pads for further MEMS processing.

A commercial full bright cyanide free gold plating solution was used (Gold ECF 60 with brightener E3, from Metalor), containing 10 g/dm^3 gold. This is a mild alkaline solution, with pH = 9. Gold films were deposited under constant current conditions. The deposition rate was 7 µm/hr with a current density of 1.2 A/dm^2. The gold plating solution was contained in a 2 litre beaker, and the sample was mounted face-down in the bath, with the anode below it, to avoid contaminants dropping on the sample surface. In the course of plating, the plating solution was mechanically stirred from the bottom at

a moderate speed. Figure 6 shows a picture of a 3.5 µm-thick electroplated gold pad on a UMC die, immediately after plating and before stripping of the resist mould.

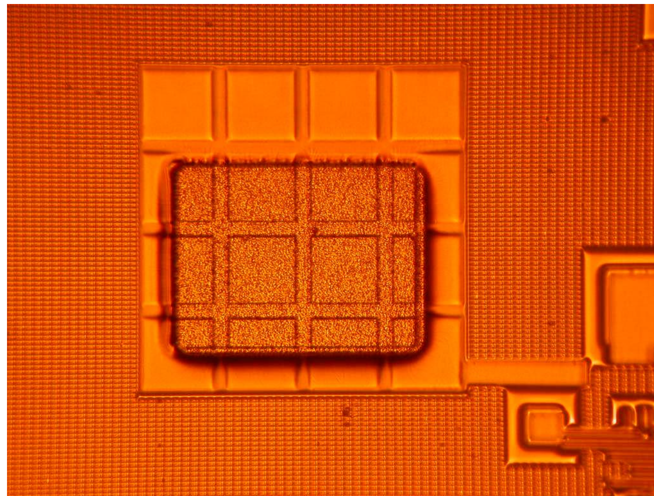

Figure 6. Gold electroplated pad on UMC die, immediately following electroplating.

2.5 Seed layer etching

In general the seed layers used in the fabrication of electroplated MEMS parts are temporary and need to be removed at some point in the process flow. Because of this it is important to choose seed layer materials that can be etched effectively without damaging the electroplated metal. This is relatively straightforward in the case of gold because it is chemically inert. When post-processing CMOS dies, it is also important to avoid any damage to the underlying circuitry. The Ti/Cu seed layer used in this work was removed using a combination of phosphoric, acetic and nitric acids. Figure 7 shows close-up views of electroplated gold pads on a UMC die, following removal of the seed layer. Note that the planarization layer is still in place.

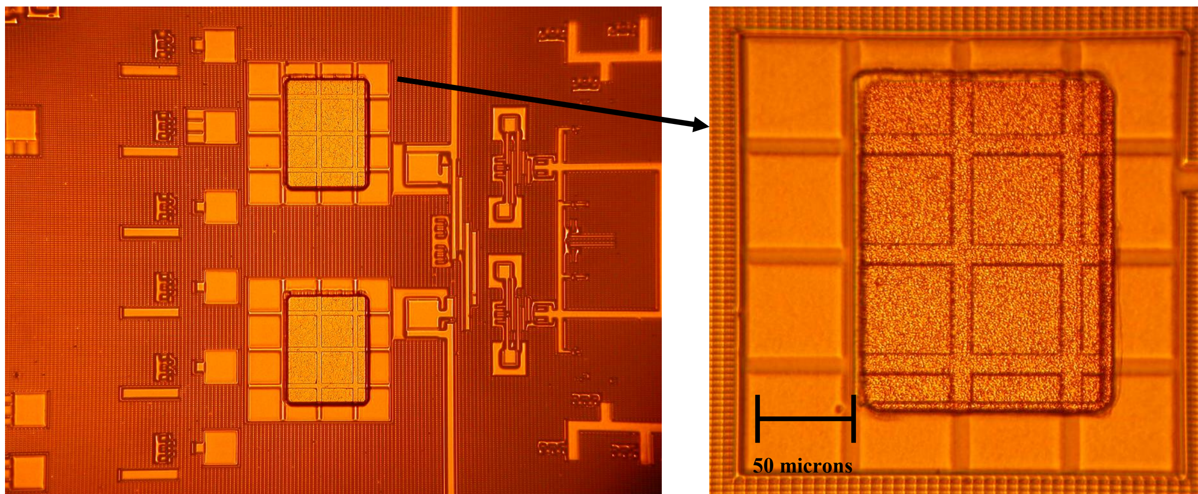

Figure 7. Gold pads on UMC die, ready for further MEMS processing.

3. CONCLUSIONS

A new method has been presented for monolithic integration of electroplated metal MEMS structures with MPW CMOS dies. This is based on post-processing of the MPW dies on BSOI carrier wafers. The low-cost techniques involved can be performed with the equipment available in many university labs. As an initial demonstrator, 3.5 μm-high gold pads have been formed on the contact pads of MPW CMOS dies fabricated using the 0.18 UMC foundry service. In future work, these pads will be used as the mechanical anchors and electrical interconnects for multi-level RF MEMS components such as self-assembled inductors.

4. ACKNOWLEDGEMENTS

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