Electrodeposition of Au for Self-Assembling 3D Micro-Structures

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ABSTRACT

Rotation of structures fabricated by planar processing into out-of-plane orientations can be used to greatly increase the 3-dimensionality of microstructures. Previously this has been achieved by a self-assembly process based on surface tension in meltable hinges. An important application is in fabricating vertical inductors on silicon, to reduce the substrate coupling and thus increase quality factor and self-resonance frequency. Previous processes have used copper tracks, and Pb-Sn hinges. However, the use of Cu limits potential applications because of oxidation, since the final structure is not embedded. Moreover, a substitute hinge material is also required, as a result of legislative restrictions on Pb use. In this paper, Au is used as an alternative to Cu for the fabrication of self-assembled 3D inductors. A process has been developed to overcome photoresist deterioration problems due to the alkaline nature of Au electro-deposition solutions. Furthermore, pure Sn is used instead of Pb-Sn as the hinge material. A Ni metal layer is introduced between the Au coils and the Sn hinge to prevent inter-diffusion and formation of eutectic Au-Sn compounds. Finally a gold capping technique is proposed to protect the Sn hinge from oxidation during hinge reflow. The fabrication techniques developed here are compatible with post-processing on active CMOS circuits, and can be adopted for other MEMS applications.

Keywords: Inductors, MEMS, self-assembly, 3D

1. INTRODUCTION

The fabrication of Radio Frequency (RF) integrated circuits is a cornerstone in research and development for modern electronics. This is due to the large number of applications of devices functioning in RF. Mobile communications devices in particular such as mobile phones, wireless ethernet devices and RF identification (RFID), require Voltage Controlled Oscillators (VCOs), transceivers, filters and power amplifiers working in the gigahertz frequency range. In such devices, inductors are critical components that play a key role in the overall device quality and impose limitations to the scaling and integration capability of the front-end system.

Package-embedded inductors can have a quality factor (Q) of larger than 20[1-2]. Such solutions however are not practical for mobile applications where scalability and integration are essential requirements. The main limitations of integrated inductors are related to losses through the semiconducting substrate at high frequencies, the parasitic capacitance between the inductor and the substrate and the low achievable inductance due to the two-dimensional nature of the conventional microfabrication techniques. In this context considerable research work has been performed on the fabrication of high quality (high-Q) integrated inductors, employing a variety of approaches. Such approaches include dielectric or metal shielding between inductor and substrate[3-5], removal of the substrate at the inductor region[6-8] or using alternative fabrication techniques to achieve three-dimensional structures such as solenoids[9-12]. Typically, such techniques offer limited suppression of the substrate effects, or introduce non-standard fabrication techniques that are difficult to integrate with the CMOS process.

In previous work, a self-assembly technique for the fabrication of vertical inductors has been proposed. Surface tension forces are used to rotate a planar inductor off the substrate and bring it to a vertical orientation[13]. An illustration of this technique, reprinted from Dahlmann et al[14] is given in Fig. 1a. An SEM image of two such vertical inductors is given in Fig. 1b[14]. Although this technique was successful, its applicability to commercial fabrication had some particular limitations. Firstly, the inductor material was copper which can be easily oxidized. Since the structure is not

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embedded, this cannot be prevented by passivation. In addition, the use of lead has recently been restricted by legislation[15] and hence an alternative material to the conventional PbSn solder has to be used. In this paper, the use of Au as the inductor material and Sn as the solder are proposed. A commercially viable fabrication process is presented and particular steps with special technical and scientific importance are discussed. Finally, an Au, lead-free vertical inductor fabricated by this method is presented.

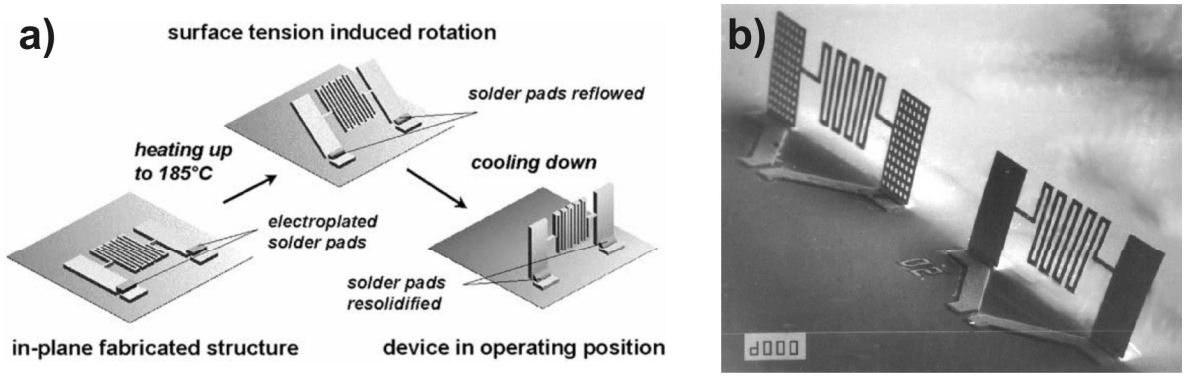

Fig. 1. (a) Simplified illustration of the self-assembly technique for the fabrication of vertical inductors. (b) SEM image of vertical inductors fabricated as described in (a). (images reprinted from Dahlmann et al[14])

2. FABRICATION PROCESS FLOW

A step by step illustration of the fabrication process flow proposed in this paper is given in Fig. 2. Standard commercial, 100 cm diameter, Si wafers are used as a substrate. The substrate is then thermally oxidized to achieve a uniform SiO_2 layer with thickness greater than 2 μm (step 1 in Fig. 2). This ensures that the parasitic capacitance formed between the inductor anchors (the parts of the inductor that remain embedded on the substrate) and the substrate is insignificant compared to the device inductance. This oxide thickness is sufficient for anchors with size 200 μm x 150 μm, a coil inductance smaller than 1 nH and working frequencies up to 10 GHz. Then, a 200 nm thick Cu seed layer is sputtered on the oxide to provide electrical conductivity for the electrodeposition of the anchors. To enhance the adhesion between Cu and oxide, a 20 nm thick Ti layer is sputtered first (step 2 in Fig. 2). A photoresist mould is then spun and patterned for the anchors (step 3), followed by electrodeposition of 3 μm of Au (step 4). Just before Au deposition, a very thin layer of Ni is electrodeposited to prevent the alkaline Au solution from attacking the photoresist at the interface with the seed layer. The resist is then stripped and the Cu and Ti seed layers are etched using an acid etchant (step 5). A sacrificial resist layer is spun and patterned with the anchor mask such that a height alignment at the edges of the anchors of around 0.5 μm is achieved (step 6). Another 200 nm Cu seed layer is then sputtered on top (step 7), completing the first layer of the total structure.

Subsequently, the photoresist mould for the inductor layer is spun and patterned (step 8) and 5 μm of Au electrodeposition follows (step 9). Again, a thin Ni layer is electrodeposited first to protect the seed layer / resist interface from the Au solution. Then, the resist is stripped (step 10) and a new resist layer is spun and patterned (pedestal mask, step 11). The pedestal will be a buffer between the Sn hinge and the Au inductor, to avoid the formation of eutectic Au-Sn compounds during reflow. The pedestal is wider than the Sn hinge to provide for a clear separation. At this stage, pedestal patterning is used to etch the seed layer at and around the hinge area and prevent any electrodeposition under the hinge. This takes place in step 12. A strip resist, re-spin and re-pattern with the pedestal mask follows (step 13) and a 0.5 μm Ni pedestal is electrodeposited (step 14).

Next, the resist is stripped (step 15) and a new mould with the hinge window is defined (step 16), followed by electrodeposition of 6 μm of Sn (step 17). Once again, the resist is renewed using the pedestal patterning (step 18) and a 200 nm thin Au is deposited to protect the Sn from oxidation (step 19). A protective resist layer is spun on top (step 20), the wafer is cleaved into small chips and the resist and the Cu seed layer are removed (step 21). Then, the sacrificial resist is etched either by dry or wet etching to release the inductor structure (step 22) and finally, the hinge is reflowed by heating to the Sn melting point (232^o C, step 23).

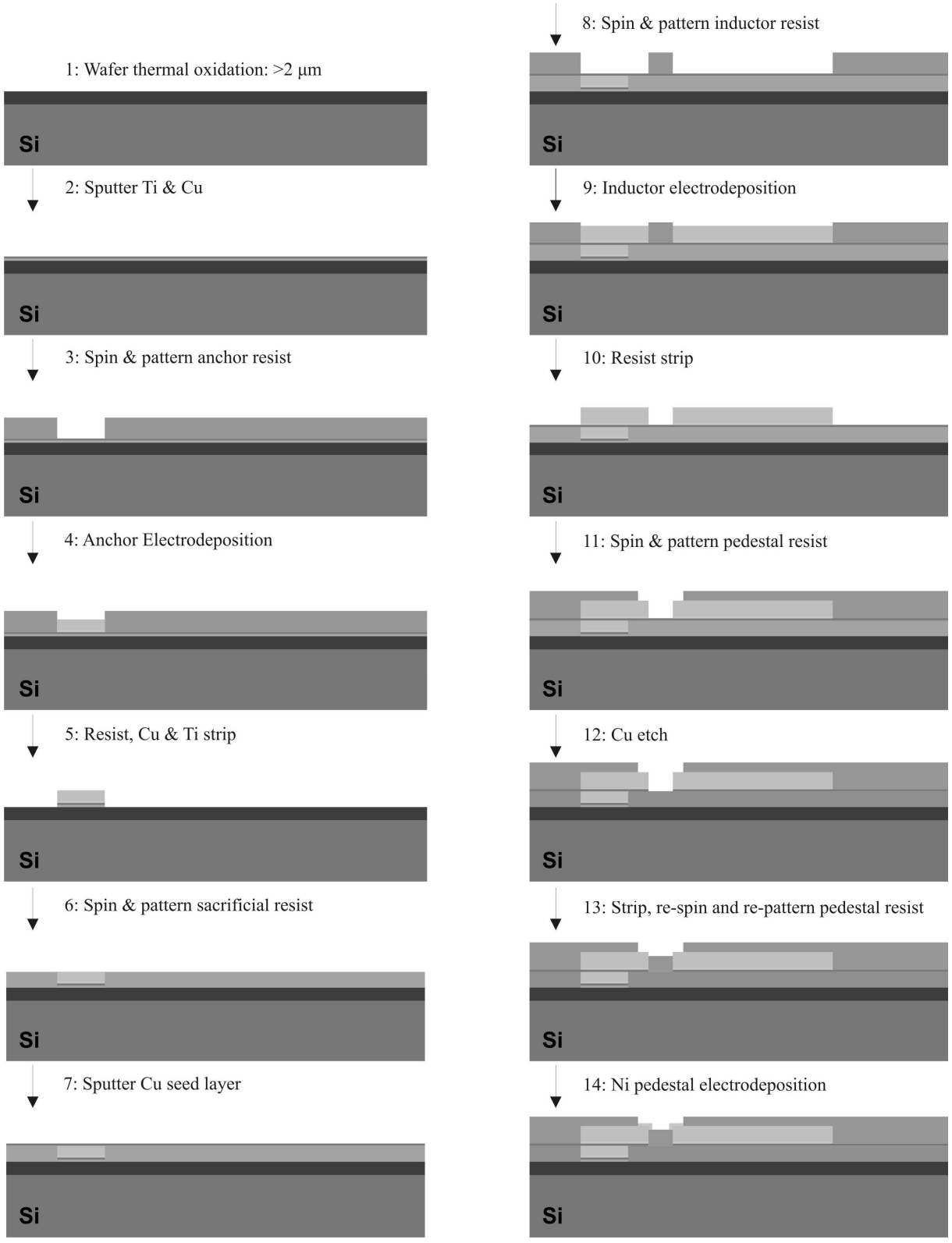

Fig 2. (a) Fabrication process flow (steps 1 to 15)

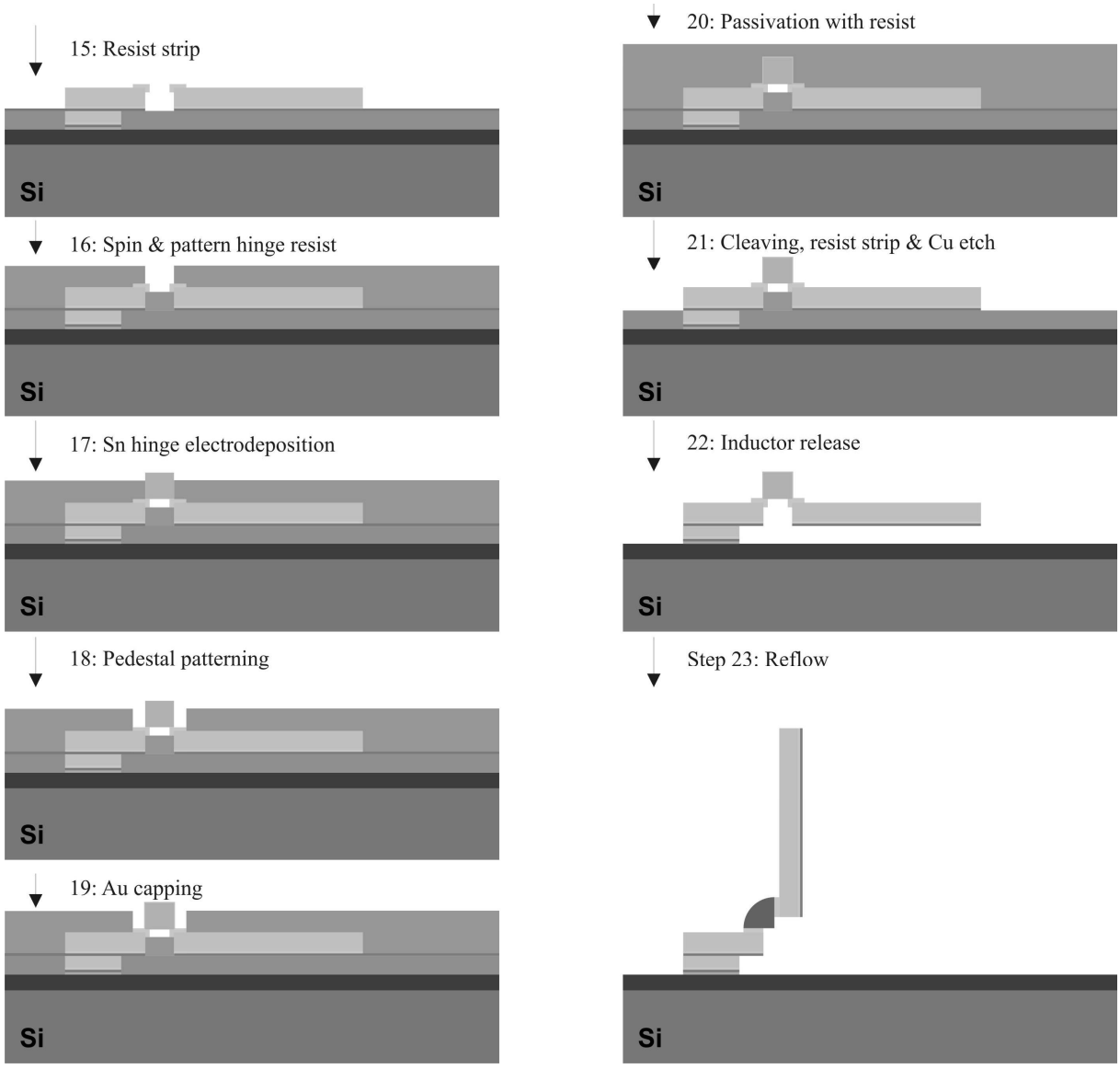

Fig 2. (b) Fabrication process flow (steps 15 to 23)

3. RESULTS AND DISCUSSION

3.1 Au electrodeposition

Au electrodeposition using photoresist as a masking material is a challenging process. This is because the commercially available Au electrodeposition solutions are alkaline and therefore incompatible with photoresists which dissolve under such chemical environments. In this work, experiments were performed using two Au solutions both acquired from Metalor Ltd U.K. The first one was solution ECF-60, sulfite based with pH around 10. The second one was solution HSD, cyanide based with pH around 7.5. In addition, three different types of photoresist were tested, namely AZ9260 (Clariant), Microposit S1828 (Shipley) and Megaposit SPR220 (Shipley).

In Table 1, the details of four characteristic recipes are presented. Optical images of the corresponding results are illustrated in Fig. 3. The rectangular shape of electrodeposition corresponds to one anchor in the process flow described in the previous section. In the first case (AZ9260 baked at 120^{o} C, recipe 1) severe underplating is observed. In the second case (SPR220, baked at 115^{o}) the photoresist disintegrated. This result did not vary although a wide range of

baking temperatures was investigated (60° C – 120° C). In the third case (AZ9260, baked at 120° C) no underplating was observed. Au electroplating was successful. The dark color of the Au surface indicates a high roughness which can be attributed to the use of a high deposition rate and a sulfite based Au electrodeposition solution. Finally, in the fourth case (S1828, baked at 100° C) no underplating was observed. The light Au surface indicates a lower Au roughness as expected due to the use of a cyanide based Au electrodeposition solution.

Recipe	Resist	Spin (Speed/Acceleration/Time)	After spin bake	After developing bake	Au plating solution	Underplating
1	AZ9260	500/500/10+2000/5000/40	90° C (hotplate)	120° C	sulfite based	severe
2	SPR220	4000/1000/40	115° C (hotplate)	-	sulfite based	severe
3	AZ9260	500/2000/10+2000/2000/40	110 ° C (oven)	110 ° C	sulfite based	limited
4	S1828	500/5000/10+1200/5000/40	100 ° C (hotplate)	-	cyanide based	limited

Table 1. Details and underplating results of four characteristic photolithography recipes for Au electrodeposition.

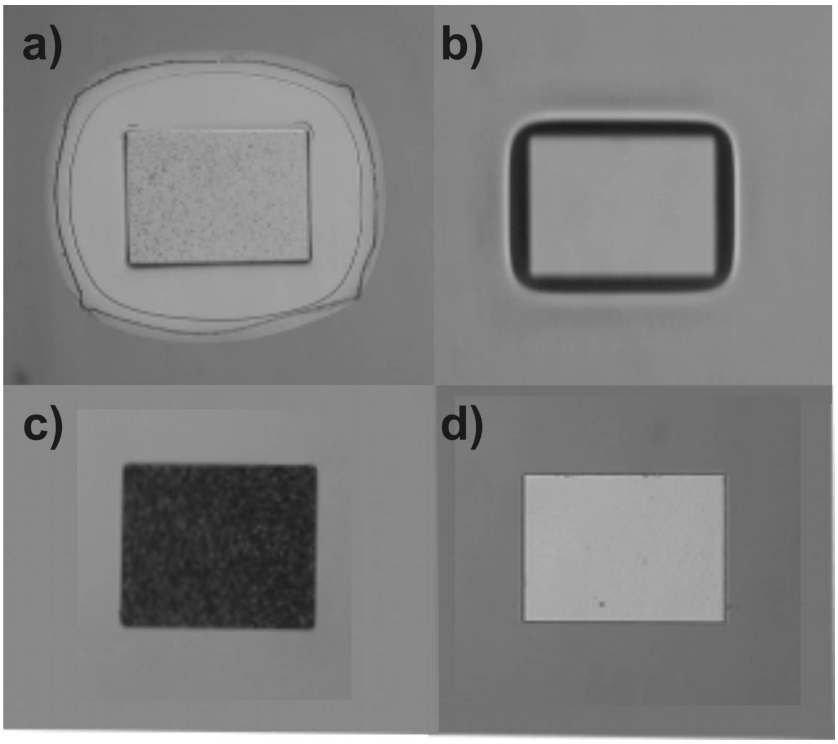

Fig. 3. Results of Au electrodeposition using the photolithography recipes described in Table 1. a) Recipe 1, severe underplating is observed. b) Recipe 2. The resist disintegrated completely and no electrodeposition was possible. Only the resist mould is illustrated. c) Recipe 3. No visible underplating. The Au surface is rough. d) Recipe 4. No visible underplating. The Au surface is smoother.

It must be noted that the peak baking temperature of the photoresist is critical for successful electrodeposition. Also, oven baking gave more consistent results than hotplate baking. A possible explanation of this is that the heat transfer to the wafer and to the resist film is more uniform and slower in oven baking.

3.2 Sn electrodeposition and reflow

The transition from conventional PbSn solder to pure Sn required the identification of a fast and cost effective method for the deposition of high quality Sn films. Electrodeposition using commercially available Sn solutions fulfilled these demands but resulted in a rough surface ($R_a \approx 400$ nm). An SEM image of electrodeposited Sn illustrating the surface roughness is shown in Fig. 4a. Improvement of the surface quality was achieved by filtering the Sn electrodeposition solution by common laboratory filter paper. This is demonstrated in Fig. 4b which shows a smoother Sn surface. Further enhancement of the Sn quality might be possible by optimization of the electrodeposition conditions, i.e. applied potential, temperature and stirring.

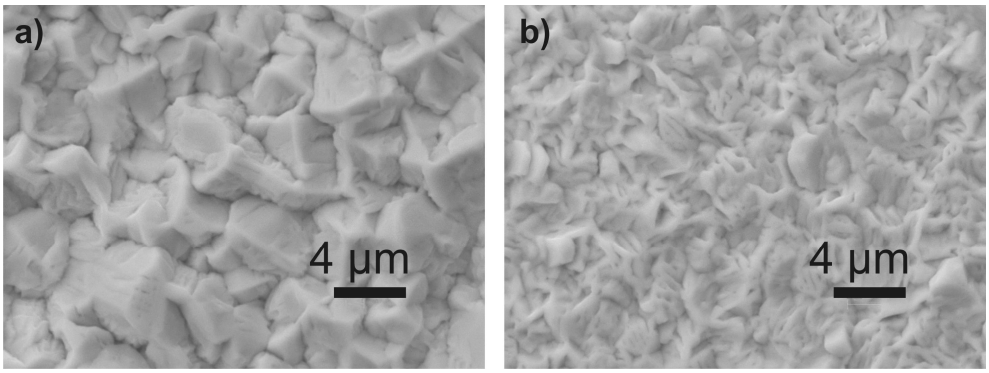

Fig. 4. Sn Electrodeposition: Sn surface roughness reduction by optimisation of electrodeposition parameters. (a) Before filtering, Ra ≈ 400 nm. (b) After filtering, Ra ≈ 250 nm

Another concern arising from the use of pure Sn as the reflowing material is that Sn can be easily oxidized. Oxidation creates a crust around the hinge which cannot melt, leading to poor reflow quality. This becomes a very important problem particularly when Sn is exposed to air for a long time or when the release process (step 22 in Fig. 2) involves the use of oxygen plasma which is strongly oxidizing. A comparison of the reflow quality between unprocessed and oxygen plasma processed Sn hinges is shown in Fig. 5. The reflow quality of unprocessed Sn is good as illustrated in the SEM images in Fig. 5a. In contrast, the oxygen plasma processed Sn gives a visibly lower reflow quality as illustrated in the SEM images in Fig. 5b. In order to explain this effect, EDX measurements were performed on the Sn surface for both cases. In the first case, no oxygen presence was detected (bottom image in Fig. 5a). However, in the second case, a 2.5% (wt) of oxygen is detected (bottom image in Fig. 5b). These results show that when oxygen plasma is used during the release process, the Sn surface is oxidized, leading to poor reflow quality.

To overcome this important limitation, a technique was developed to protect the Sn hinge from oxidation. A thin Au film is electrodeposited around the Sn as described in step 19 of Fig. 2. This thin film forms a eutectic compound with Sn, with a slightly lower melting point than pure Sn[16]. Hence, this additional film does not obstruct the reflow process. On the other hand, the formation of eutectic Au-Sn could also occur by intermixing between the hinge and the Au inductor. This effect would prevent the proper reflow of the hinge. A solution to this problem was found on the introduction of an additional, Ni thin film (pedestal) to function as a buffer between Sn and inductor Au (step 14 in Fig. 2). The choice of Ni was made because it is a material with low tendency to form compounds with either Sn or Au. A simplified schematic description of the hinge structure including the pedestal and the Au-capping techniques is given in Fig. 6a.

The structure described in Fig. 6a was realized as part of the total inductor fabrication process described in section 2. An SEM image before reflow is shown in Fig. 6b. The bottom left layer is the Au hinge part while the bottom right layer is the Au inductor part. The darker layer right on top of them is the Ni pedestal. The top layer is the Sn hinge. The hinge is covered by a thin Au layer which is not visible in this SEM image. From the Au electrodeposition current density and duration, the Au capping layer is estimated to have a thickness of around 100 nm. The structure is shown

after reflow in Fig. 6b. A successful reflow is observed. The Au capping layer was successfully alloyed with the Sn. The Ni pedestal prevented intermixing with the bulk Au of the inductor and the hinge. On the other hand, some remaining sacrificial resist is observed underneath the inductor layer, indicating that the release process was not complete. Incomplete release ultimately prevents the surface tension forces of the hinge from rotating the inductor. This is the reason for not observing any rotation in Fig. 6c.

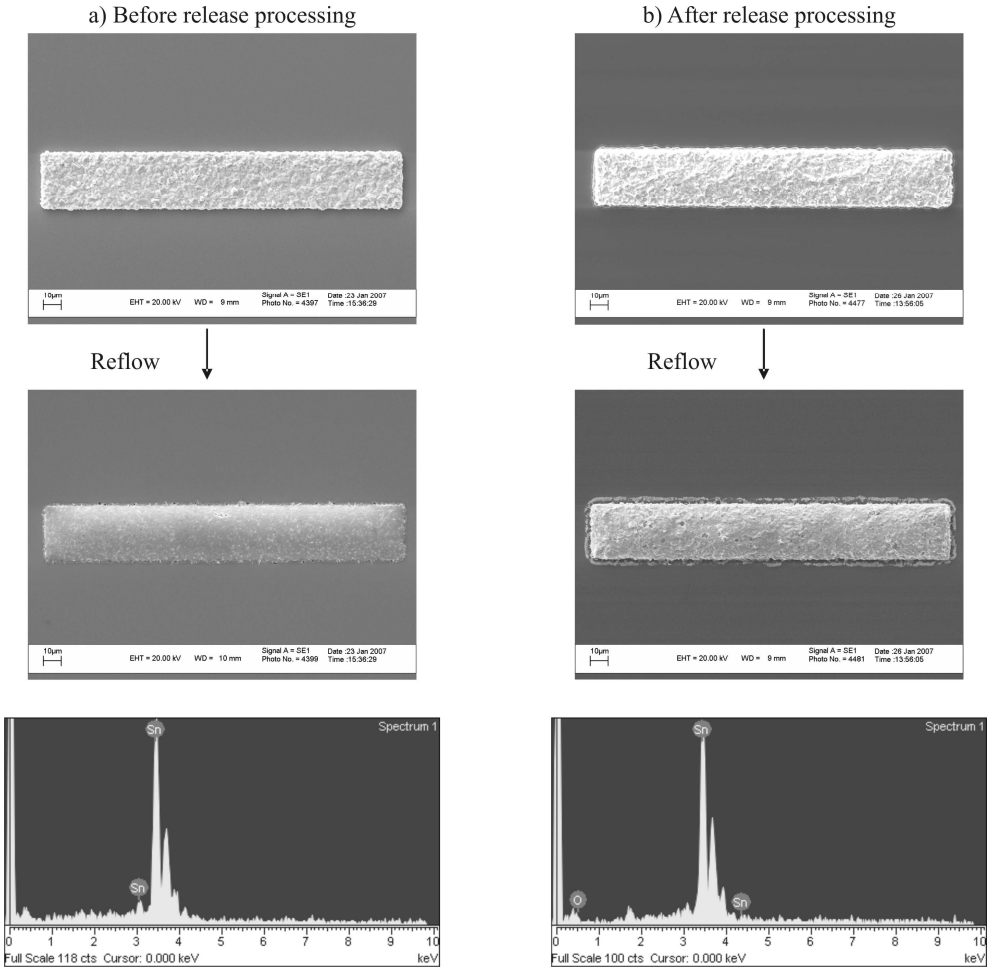

Fig. 5. Sn Reflow, EDX Measurements. (a) Reflow without oxygen plasma release processing (Sn: 100%). (b) Reflow after oxygen plasma release processing (Sn: 97.5% wt, O_2: 2.5% wt).

3.3 Self-assembly

In order to achieve full release of the inductor structures, a combination of dry and wet release processes was employed. In the first step, a dry etch in oxygen plasma was performed to remove the bulk sacrificial resist around the structures. In the second step, the sample was immersed in acetone to achieve isotropic resist dissolution and completely release the structure from the substrate. A self-assembled inductor, successfully released by this method is presented in Fig. 7. The angle between the inductor orientation and the substrate was found to be around 70^o. The inductor is a meander of size 500 x 560, with 5.5 turns and a line width of 15 μm. A full electrical characterisation of such devices at RF circuits is underway.

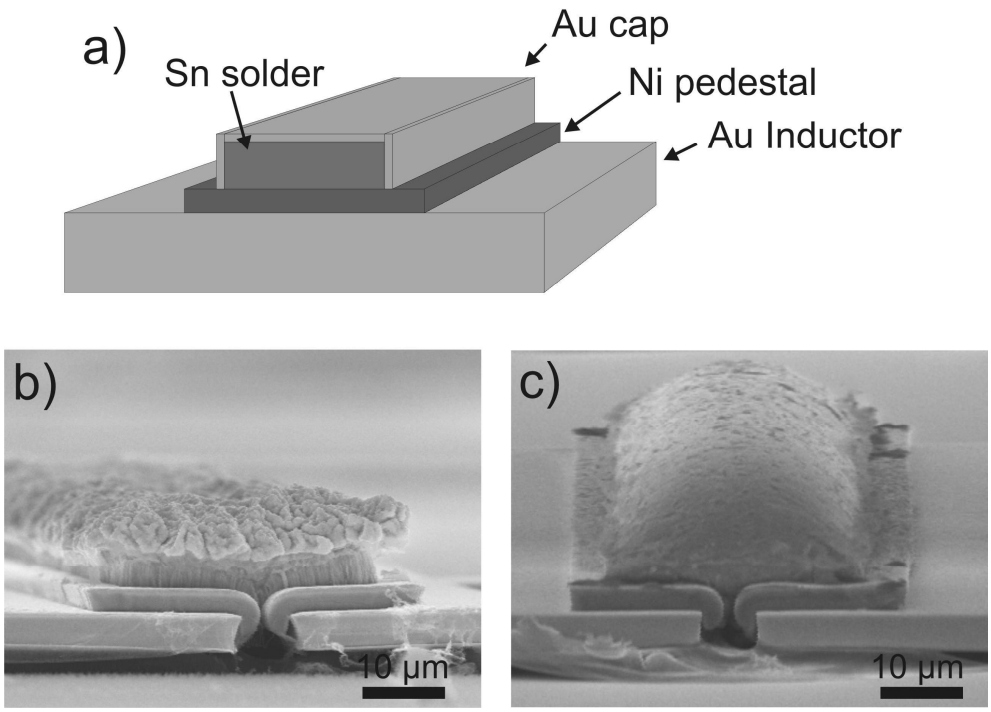

Fig. 6. Ni Pedestal and Au capping

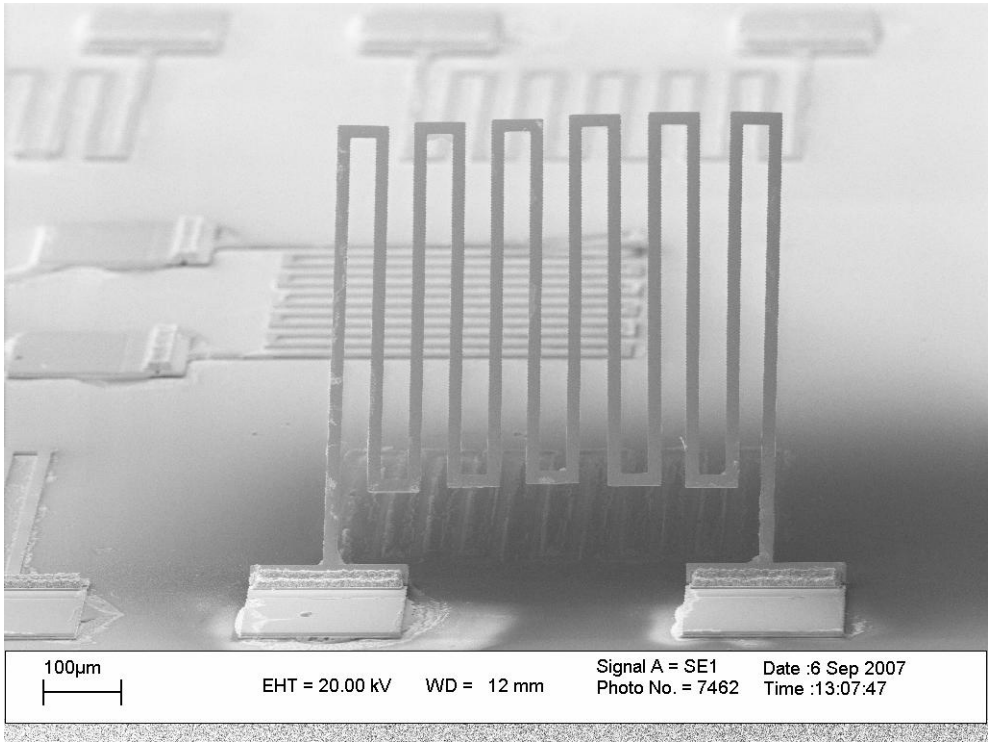

Fig. 7. Example of a self-assembly rotated, 3D Au inductor using pure Sn as solder and the pedestal and Au capping techniques.

It must be emphasised that all the steps used for the fabrication of this device, as described in section 2, are compatible with post-processing on active CMOS systems. Work towards the fabrication of such devices on active circuits has been performed and significant progress towards this direction is being reported elsewhere[17].

4. CONCLUSION

In this paper a new technique for the fabrication of vertical inductors is proposed. Successful transition from Cu to Au as the inductor material and from PbSn to pure-Sn as the hinge material was demonstrated. Special technical challenges including Au electrodeposition, Sn oxidation and Au-Sn intermixing were discussed and appropriate solutions were identified. Successful fabrication of a vertical inductor using this method was demonstrated. This advancement addresses the issues of Cu-oxidation and lead-based solder usage and opens up the way for the commercial exploitation of self-assembled vertical inductors.

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