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# A novel capillary-effect-based solder pump structure and its potential application for through-wafer interconnection

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#### **Abstract**

Through-wafer electrical interconnection is a critical technology for advanced packaging. In this paper, a novel capillary-effect-based solder pump has been proposed and analyzed, which could produce interconnects through and between silicon dies. The principle of this pump is to use the surface tension of a molten solder, introduced in the form of balls, to drive sufficient material into a deep reactive-ion etched hole to form a through-wafer conductive path. The solder pump structure uses unwettable through-wafer holes of different diameters together with wettable metallization on two dies to provide the pressure differential and flow path. Using multiple feed holes and a single via hole complete through-wafer interconnects are demonstrated.

(Some figures in this article are in colour only in the electronic version)

## 1. Introduction

Through-wafer interconnections (TWI) (otherwise known as through-silicon vias) are a critical and enabling technology for 3D wafer-level packaging. Compared to conventional planar feed-through interconnections, TWI offers the advantages of smaller package size, higher connection density and lower resistance [1].

The fabrication of TWI has three requirements: (1) production of a via through the wafer, (2) introduction of a conductive pathway and (3) isolation of this pathway from the rest of the wafer. The most common method of forming a conductive pathway involves metallization of the sidewall of the via hole through deposition followed by electroplating to fill the via.

There are two challenges to such an approach. First, the seed layer deposition has to overcome the problem of ensuring adequate sidewall coverage while being geometrically restricted by the high aspect ratio of the via hole. Second, the electroplating is a time-consuming process, often taking hours to completely fill the via hole, while tight control of all the chemical additives during the process is critical

but costly [2–9]. Other TWI techniques require specialized wafers, silicon with either very low or very high resistivity or glass, limiting the ability to integrate devices onto these wafers and increasing cost [10–12]. The TWI technology developed by Silex Ltd, for example, uses low-resistivity through-wafer silicon pillars, fabricated by deep etching, as the conductive medium [13]. The resistance of highly conducting silicon vias is still higher than that of the metal-based vias, compromising the ability to handle large currents. In addition, all of these TWI technologies require further process steps to attach solder balls if they are to be surface mount compatible.

In this paper, a novel capillary-effect-based solder pump structure is proposed, modeled and implemented [14]. The principle of this technique is to use the surface tension of the molten solder to pump sufficient material into a throughwafer hole to produce a conductive path. The solder itself is introduced in the form of solder balls, a material which has found widespread use in device packaging.

This solder pump technique promises a TWI technology that can be used with standard silicon wafers and does not require sidewall deposition and electroplating steps to produce a conductive path. This new approach should provide a

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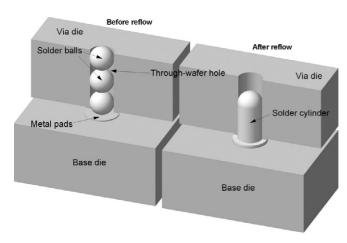


Figure 1. Reflow of multiple solder balls in a single through-wafer hole.

flexible, rapid and low-cost process to produce low-resistivity through-wafer interconnects.

#### 2. Structure and mechanism

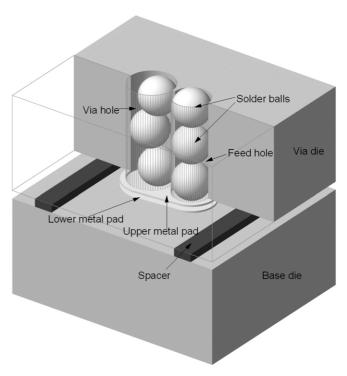
#### 2.1. Solder pump concept

Figure 1 shows a potential way of forming a conductive path using solder balls. The balls are first collected in throughwafer holes. After reflow a column of solder is formed. Since the volume of the solder balls will always be less than that of the hole, the solder is not able to completely fill the hole after reflow. This volume constraint problem can be solved by introducing an additional feed hole containing further solder balls and using capillary action to pump liquid solder from the feed holes to the via hole.

This improved design is shown in figure 2. Two dies are used to form the solder pump structure: a via die in which the TWI will be formed, and a base die which is separated from the via die by spacers to give a controlled gap. The volume of the solder pump is geometrically defined by a feed hole and via hole in the via die and a reflow channel between the two holes constrained by the wettable metallization on either side of the gap between the dies (see figure 2). The diameter of the feed hole is slightly smaller than that of the via hole, generating a pressure differential in the liquid solder between the two holes during reflow. Solder balls are placed in both via and feed holes, with the total volume of solder sufficient to complete a conductive path through the entire thickness of the via die.

## 2.2. Mechanism of the solder pump

The reflow of the solder in the pump structure can be divided into two steps. The first step is the initial coalesence of the solder balls and wicking along the pathway between the two holes to form a contiguous volume of the molten solder. This wicking is facilitated by the wettable metallization on



**Figure 2.** Schematic of the proposed solder pump structure with solder balls placed into the via and feed holes. Note the different hole diameters.

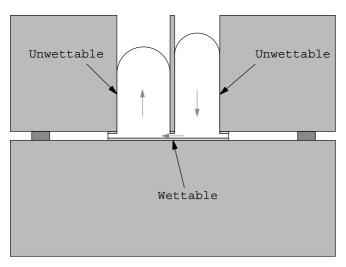
either side of the gap between the dies. The second step is the pumping of the solder from the feed hole to the via hole, driven by the pressure difference. Because the hole sidewalls are unwettable to solder, hemispherical surfaces are formed above the solder in both the via and the feed holes. The pressure thus generated in the molten solder is given by  $2\gamma/r$  where  $\gamma$  is the surface tension of the liquid solder, and r is the radius of curvature of the hemispherical cap, which for an unwettable sidewall is given by the radius of the hole (see figure 3). The driving pressure differential is given by

$$\Delta P = 2\gamma \left( \frac{1}{r_{\text{feed}}} - \frac{1}{r_{\text{via}}} \right)$$

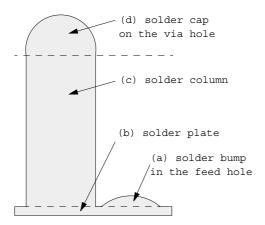
$$\approx 2\gamma \Delta r / r_{\text{ball}}^2, \tag{1}$$

where  $r_{\rm feed}$  and  $r_{\rm via}$  are the radii of the feed and via holes and  $\Delta r = r_{\rm via} - r_{\rm feed}$  is small compared to the ball radius,  $r_{\rm ball}$ , for the approximate relationship to hold. Flow will continue until the two cap radii are equal at which point the surface of the molten solder in the feed hole is lowered to the bottom of the via wafer and further flow would cause an increase in the feed hole cap radius.

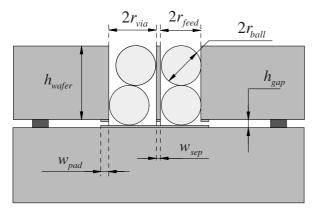
The final solder geometry is thus governed by surfaceenergy minimization. At the completion of the flow, the final geometry of the solder is composed of four volumes: (a) a solder cap in the feed hole; (b) a solder plate between two dies; (c) a solder column in the via hole, which serves as the conductive medium for the TWI and (d) a solder cap on the via hole, as shown in figure 4.



**Figure 3.** Working principle of the solder pump structure. The arrows indicate the direction of solder flow.



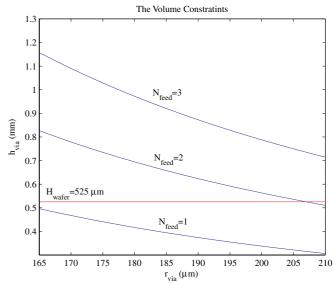
**Figure 4.** Cross section of the solder geometry in the solder pump after reflow. The final solder column extrudes beyond the outlet of the via hole.



**Figure 5.** Main geometrical parameters for modeling the solder pump.

# 3. Design issues

Three main design issues related to the solder pump geometry (see figure 5) need to be considered.



**Figure 6.** Plot of solder column height  $h_{\rm via}$  against via radius  $r_{\rm via}$  and the number of feed holes  $N_{\rm feed}$  for 300  $\mu$ m diameter solder balls. One feed hole is insufficient to ensure the completion of the via (525  $\mu$ m thick silicon wafer). Two feed holes are sufficient for vias up to 208  $\mu$ m in radius.

#### 3.1. Volume constraints

The total solder volume will be multiples of the volume of a single solder ball. Sufficient feed holes are needed to provide enough solder volume to complete the via, with the number depending on the value of  $r_{\rm via}$ . This constraint depends on the exact geometry of the caps, but for simplicity of analysis we assume that volumes (a), (b) and (d) in figure 4 will require one solder-ball volume. The height of the solder column in the via hole  $(h_{\rm via})$  after reflow is then given by

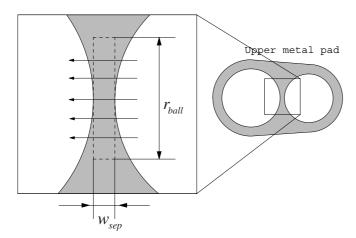
$$h_{\text{via}} = \frac{4r_{\text{ball}}^3}{3r_{\text{via}}^2} [N(N_{\text{feed}} + 1) - 1], \tag{2}$$

where N is the number of the solder balls that can be placed in one through-wafer hole, and  $N_{\rm feed}$  is the number of feed holes. Figure 6 plots  $h_{\rm via}$  against  $r_{\rm via}$  for  $r_{\rm ball}=150~\mu{\rm m}$  and N=2 using one, two or three feed holes.

The required solder column height to create a throughwafer interconnect is shown as a horizontal line for a standard 4" silicon wafer with a thickness of around 525  $\mu$ m.

## 3.2. Pumping time

The second design issue is the time required to complete the flow of liquid solder from one hole to another, which if too long will impact the viability of the technique. This time can be simply calculated under a series of reasonable assumptions. First, the bottleneck of the flow occurs between the two holes, which has a much smaller cross-sectional area compared to the size of the through-wafer holes, as can be seen from figure 3; thus we assume that the pressure drop in the two holes is negligible compared to the pressure differential. Second, we simplify the geometry of the flow between the holes to a notional rectangular region as shown in figure 7. Third, it



**Figure 7.** Solder reflow geometry between two holes. The dashed rectangle indicates the assumed simplified main flow region.

is assumed that the flow between the two holes is laminar, as can be justified by the result.

Under these assumptions, the volumetric flow rate Q is given by [15]

$$Q = \frac{h_{\rm gap}^3 r_{\rm ball}}{12\,\mu} \frac{\Delta P}{w_{\rm sep}},\tag{3}$$

where  $\mu$  is the viscosity of the molten solder and  $w_{\rm sep}$  is the wall thickness between the holes. Using equations (1) and (4) an expression for the reflow time  $\tau$  can be derived:

$$\tau = \frac{4}{3} \frac{N\pi r_{\text{ball}}^3}{Q}.$$
 (4)

Transferring the volume of N solder balls therefore requires a flow time  $\tau$  of

$$\tau = 8\pi N \frac{\mu}{\gamma} \frac{r_{\text{ball}}^4}{\Delta r} \frac{w_{\text{sep}}}{h_{\text{gap}}^3}.$$
 (5)

To verify the assumption of laminar flow, the Reynolds number is calculated as

$$R_e = \frac{\rho QD}{\mu A},\tag{6}$$

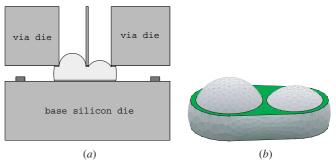
where  $\rho$  is the density of liquid solder, D is the geometry-dependent characteristic dimension, and A is the cross-sectional area of the flow. For a rectangular duct, D is defined as

$$D = \frac{4A}{P},\tag{7}$$

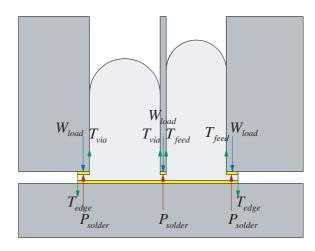
where P is the wetted perimeter. By substituting equations (3) and (7) into (6), the Reynolds number becomes

$$R_e = \frac{2}{3} \frac{\rho \gamma}{\mu^2} \frac{h_{\text{gap}}^3}{w_{\text{sep}}} \frac{\Delta r}{r_{\text{ball}}} \frac{1}{2(r_{\text{ball}} + h_{\text{gap}})}.$$
 (8)

For  $\mu=0.012$  PaS [16],  $\gamma=0.55$  N m<sup>-1</sup> [17],  $r_{\text{ball}}=150~\mu\text{m}$ , N=2,  $w_{\text{sep}}=20~\mu\text{m}$  (limited by the microfabrication process),  $h_{\text{gap}}=25~\mu\text{m}$ , and  $\Delta r$  varying between 10  $\mu\text{m}$  and 100  $\mu\text{m}$ ,  $\tau$  is calculated to vary from 71 ms to 7.1 ms and the Reynolds number between 2.8 and 28, justifying the initial assumption of laminar flow. A detailed analysis of the full flow geometry would give a slightly longer completion time but would not change the conclusion that the pumping process is inherently fast.



**Figure 8.** (a) Schematic view of pump failure due to lifting of the via die. (b) Finite element simulation (surface evolver) of the lifting failure



**Figure 9.** Forces acting on the upper metal pad.

#### 3.3. The lifting force

During the reflow, the solder pressure and the surface tension acting on the upper metal pad generates a lifting force, which if larger than the weight of the via die, will raise the via die and cause failure of the pump. Figure 8 shows the schematic view and a finite element simulation (surface evolver) of this kind of failure.

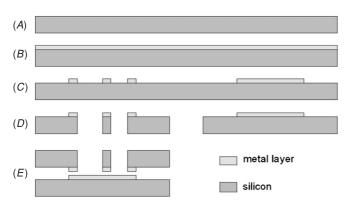
In terms of the forces acting on the upper metal pad, as shown in figure 9, the lifting force can be derived as

$$F_{\text{lifting}} = T_{\text{feed}} + T_{\text{via}} + P_{\text{solder}} - T_{\text{edge}}, \tag{9}$$

where  $T_{\rm feed}$  and  $T_{\rm via}$  are the surface tension forces acting on the edges of the feed and the via hole respectively,  $P_{\rm solder}$  is the force due to the internal pressure of the molten solder and  $T_{\rm edge}$  is the surface tension force acting on the outer edge of the upper metal pad. By assuming that the vertical radius of curvature of the solder between the two metal pads is much larger than the radius of the holes, equation (9) becomes

$$F_{\text{lifting}} = \gamma (2N_{\text{feed}}\pi r_{\text{feed}} + 2\pi r_{\text{via}} - L_{\text{edge}}) + P_{\text{solder}}, \quad (10)$$

where  $L_{\rm edge}$  is the perimeter of the outer edge of the upper metal pad.  $P_{\rm solder}$ , the pressure within the molten solder, is technically not uniform. It varies between  $2\gamma/r_{\rm via}$  and  $2\gamma/r_{\rm feed}$ . To simplify the problem, we assume that the pressure within the molten solder is uniform and approximate it to be



**Figure 10.** Steps of the solder pump microfabrication. (*A*) Standard 4" double-side polished silicon substrate. (*B*) Sputter deposition of a wettable metal multilayer. (*C*) Patterning of the metal pads. (*D*) Through-wafer DRIE to realize via holes and separate the dies. (*E*) Via and base dies forming the basic solder pump structure.

 $2\gamma/r_{\text{feed}}$ . Equation (10) becomes

$$F_{
m lifting} pprox \gamma \left( 2\pi N_{
m feed} r_{
m feed} + 2\pi r_{
m via} + rac{2A_{
m upper-pad}}{r_{
m feed}} - L_{
m edge} 
ight)$$

where  $A_{\rm upper-pad}$  is the area of the upper metal pad.If  $F_{\rm lifting} > W_{\rm load}$ , additional loading is necessary to prevent the lifting of the via die during reflow. Solving equation (11), for  $r_{\rm ball} = 150~\mu{\rm m}$ ,  $r_{\rm feed} = 155~\mu{\rm m}$ ,  $N_{\rm feed} = 1$ ,  $r_{\rm via} = 187.5~\mu{\rm m}$  (1.25 $r_{\rm ball}$ ),  $w_{\rm pad} = 30~\mu{\rm m}$ , gives  $F_{\rm lifting} \approx 0.73~{\rm mN}$ , which is in good agreement with the value of 0.68 mN predicted by the FEA simulation.

## 4. Demonstration

# 4.1. Microfabrication

Various samples have been fabricated to experimentally validate the presented solder pump approach. The prototypes use standard 300  $\mu$ m diameter solder balls. Allowing for the tolerance of the solder balls, the feed hole diameter was set to 310  $\mu$ m ( $r_{\rm feed}=155~\mu$ m). We chose  $w_{\rm pad}=40~\mu$ m and  $w_{\rm sep}=20~\mu$ m. Solder pumps with the following feature dimensions have been realized: (1)  $r_{\rm via}=165~\mu$ m (1.1 $r_{\rm ball}$ ),  $N_{\rm feed}=3$ ; (2)  $r_{\rm via}=187.5~\mu$ m (1.25 $r_{\rm ball}$ ),  $N_{\rm feed}=1$  and (3)  $r_{\rm via}=210~\mu$ m (1.4 $r_{\rm ball}$ ),  $N_{\rm feed}=4$ .

All demonstrators were fabricated on standard 4" diameter, 525  $\mu$ m thick, double-side polished silicon wafers. The fabrication involves two main steps: the deposition and patterning of solder wettable thin-film metal pads, and the etching of through-wafer holes into the silicon substrate. The chosen process flow is illustrated in figure 10. The metal layer is a sputtered multilayer formed by Cr (35 nm), Ni (250 nm) and Au (100 nm).

The through-wafer holes were dry etched by deep reactive ion etching (DRIE) using the STS/BOSCH process [18].

### 4.2. Reflow process

Alignment of the via and base dies is achieved with the help of a simple alignment jig, see figure 11. Both the via and base

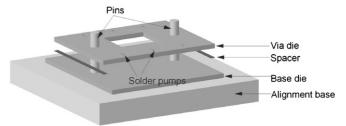
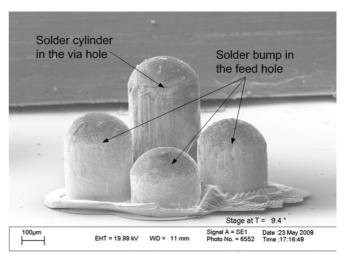


Figure 11. Jig for demonstrator assembly and solder reflow.



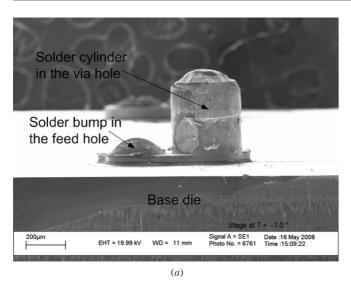
**Figure 12.** Failure of the solder pump reflow due to too low  $\Delta r$  margin. Parameters:  $r_{\rm feed} = 155~\mu{\rm m}$ ,  $r_{\rm via} = 165~\mu{\rm m}$  (1.1 $r_{\rm ball}$ ),  $N_{\rm feed} = 3$ . The solder in the three feed holes has not been completely transferred to the via hole. Note that the via die has been removed for clarity.

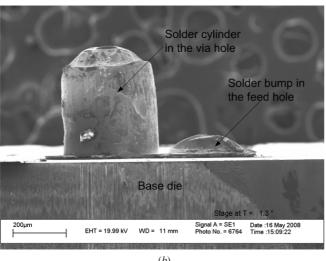
dies have holes etched during the DRIE step for insertion of alignment pins. The gap between the dies  $h_{\rm gap}=25~\mu{\rm m}$  is achieved by placing thin metal foil spacers between the two dies. Lifting of the via die during reflow is prevented by additional small weights on top of the via die.

The used solder balls were lead-free (ECO brand from Senju Metal Industry Co. Ltd) with a composition of Sn-3.0 Ag-0.5Cu and a melting point between 217 and 220 °C [19]. Two solder balls were loaded into each feed hole and the via hole. The die assembly was placed on a hotplate in a gastight reflow chamber together with microscope slides lightly sprayed with resin flux (electrolube brand). After an initial 15 min nitrogen purge, the hotplate was ramped to 250 °C at 25 °C min<sup>-1</sup> for reflow and then returned to room temperature.

## 4.3. Reflow results

Initial results confirmed that too small a difference between the feed and via hole diameters can cause failure of the solder pump. Figure 12 shows the reflow result of a solder pump with  $r_{\rm via} = 165~\mu{\rm m}~(1.1r_{\rm ball})$  and  $N_{\rm feed} = 3$ . The via die is removed for clarity. As can be seen, the pumping process was not completed, with solder still left in the three feed holes.



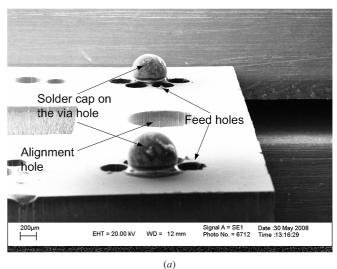


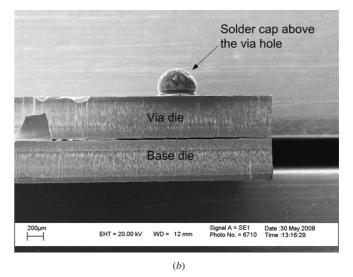
**Figure 13.** Reflow results for two different solder pump samples with  $r_{\rm feed} = 155~\mu{\rm m}$ ,  $r_{\rm via} = 187.5~\mu{\rm m}$  (1.25 $r_{\rm ball}$ ),  $N_{\rm feed} = 1$ . Note that the via die has been removed for clarity.

Figure 13 shows SEM images of solder pumps after reflow (via die removed) with a larger difference between the feed and via hole radii with  $r_{\rm via}=187.5~\mu{\rm m}~(1.25r_{\rm ball})$  and  $N_{\rm feed}=1$ . Only the solder cap remains in the single feed hole, with the bulk of the solder pumped over to the via hole. Thus a clear  $\Delta r$  margin between 32.5  $\mu{\rm m}$  and 10  $\mu{\rm m}$  appears necessary for the successful operation of the solder pump. This may be due to the roughness and variation in the cross-sectional area of the holes, both imperfections introduced by the DRIE process.

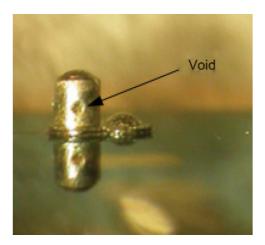
Figure 14 shows the reflow results in solder pumps with multiple feed holes to more than adequately meet the volume constraint. Here  $r_{\rm via} = 210~\mu{\rm m}\,(1.4r_{\rm ball})$  and  $N_{\rm feed} = 4$ . Solder bumps considerably larger than the original solder-ball size were formed above the via hole. Figures 13 and 14 clearly demonstrate the proof of concept for the proposed solder pump.

Voids in the solder column have been observed (figure 15). These voids are probably formed during the initial coalescence of the solder balls. Evidently such minor voids,





**Figure 14.** Reflow results for a solder pump with  $r_{\text{feed}} = 155 \, \mu\text{m}$ ,  $r_{\text{via}} = 210 \, \mu\text{m} \, (1.4 r_{\text{ball}})$ ,  $N_{\text{feed}} = 4$ : (a) front view, (b) side view.



**Figure 15.** A void created in the solder column during reflow.

whether at the solder-silicon interface or within the solder volume, do not stop the pumping process.

#### 5. Discussion and conclusions

A novel capillary-effect solder pump structure for TWI has been proposed, analyzed and demonstrated. Electrical isolation between the solder via and the bulk silicon substrate has not been demonstrated here, but can be achieved by growth or deposition of an insulating layer on the through-hole sidewalls. Both silicon dioxide and silicon nitride are suitable candidates, as both are unwettable to the molten solder.

The size of the solder pump is only limited by the size of the used solder balls. For our experiments, we have used solder balls of 300  $\mu m$  diameter. These are still relatively easy to handle and commercially available. The presented process is scalable and could be automated by using solderball placement instruments reducing the minimum diameter to 200  $\mu m$  [20]. Since multiple feed holes are needed to provide sufficient solder volume, the overall areal density of connections is reduced. A possible improvement could be to etch the feed holes into the base die, hence forming a vertical pump structure. Although the technique produced consistent results under the required geometry, further work is needed to demonstrate sufficient yield in larger volumes.

Compared with other TWI technologies, there are several potential advantages of this approach: (a) The process is fast compared to electroplating; (b) a protruding solder bump can be formed on the via after reflow which can be used for direct flip chip assembly, avoiding an additional solder reflow process; (c) metallization of the via-hole sidewall is not necessary so that the step coverage problem of metal deposition may be avoided; (d) the resistance of the via is in the m $\Omega$  range due to the low electrical resistivity of solder and the relatively large cross-sectional area of the via.

# Acknowledgment

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# References

- [1] Jozwiak J, Southwick R G, Johnson V N, Knowlton W B and Moll A J 2008 Integrating Through-wafer interconnects with active devices and circuits, advanced packaging *IEEE Trans.* 31 4–13
- [2] Yue C P, Mccarthy A, Ryu C, Lee T H, Wong S S and Quate C F 1999 Ultra-low resistance, through-wafer via (TWV) technology and its applications in three dimensional structures on silicon *Japan. J. Appl. Phys.* 38 2393–6

- [3] Neysmith J 2001 Modular, device-scale, direct-chip-attach packaging for microsystems *IEEE Trans. Compon. Packag. Technol.* 24 631–4 (see also Compon. Packag. Manuf. Technol. Part A: Packaging Technologies)
- [4] Ok J S 2003 IEEE Trans. Adv. Packag. 26 302–9 (see also IEEE Transactions on Components, Packaging and Manufacturing Technology, Part B: Advanced Packaging,)
- [5] Hilbert C, Nelson R, Reed J, Lunceford B, Somadder A, Hu K and Ghoshal U 1999 Thermoelectric MEMS Coolers pp 117–22
- [6] Wu J H 2004 A through-wafer interconnects in silicon for rfics Electron. Devices IEEE Trans. 51 1765–71
- [7] Lin C-W, Yang H-A, Wang W C and Fang W 2007 Implementation of three-dimensional SOI-MEMS wafer-level packaging using through-wafer interconnections J. Micromech.. Microeng.. 1200–5
- [8] Saadaoui M 2007 Local sealing of high aspect ratio vias for single step bottom-up copper electroplating of through wafer interconnects *Proc. IEEE Sensors 2007 Conf.* pp 974–7
- [9] Jozwiak J 2008 Integrating through-wafer interconnects with active devices and circuits *IEEE Trans. Adv. Packag.* 31 4–13 (see also IEEE Transactions on Components, Packaging and Manufacturing Technology, Part B: Advanced Packaging)
- [10] Lin C-W 2008 Implementation of SOG devices with embedded through-wafer silicon vias using a glass reflow process for wafer-level 3D MEMS integration *IEEE 21st Int. Conf. on Micro Electro Mechanical Systems (Tucson, Az)* ed C-P Hsu (Piscataway, NJ: IEEE) pp 802–5
- [11] Leung L L W and Chen K J 2005 Microwave characterization and modeling of high aspect ratio through-wafer interconnect vias in silicon substrates *IEEE Trans. Microw. Theory Tech.* 53 2472–80
- [12] Tian J, Iannacci J, Sosin S, Gaddi R and Bartek M 2006 Rf-MEMS wafer-level packaging using through-wafer via technology 8th Electronics Packaging Technology Conf., 2006 EPTC '06 pp 441–7
- [13] Rimskog M 2007 Through wafer via technology for MEMS and 3D integration. 32nd IEEE/CPMT International Electronic Manufacturing Technology Symp. 2007 IEMT '07 pp 286–9
- [14] This technique has been filed for granting a patent,
  Application Number GB reference number: P45708/JEP
- [15] Alexandrou A 2001 Principles of Fluid Mechanics 1st edn (Englewood Cliffs, NJ: Prentice-Hall) p 237 Chapter 7
- [16] Pape U and Schulz J-U 2006 Characteristics of lead-free solders during flow soldering (selective and wave soldering) Ist Electronics System Integration Technology Conf. 2006 vol 1 pp 139–44
- [17] Kaban I, Mhiaoui S, Hoyer W and Gasser J-G 2005 Surface tension and density of binary lead and lead-free Sn-based solders J. Phys.: Condens. Matter. 17 7867–73
- [18] Schilp A and Laermer F 1996 Method of anisotropically etching silicon *US Patent* US5501893: Robert Bosch GmbH (March 26 1996)
- [19] http://www.senju-m. co.jp/en/product/ecosolder/index.html
- [20] www.chipscalereview.com/archives/ES/issues/1102/ solder\_ball\_placement.pdf