Solid-State Electronics 83 (2013) 107–112

Contents lists available at SciVerse ScienceDirect

Solid-State Electronics

journal homepage: www.elsevier.com/locate/sse

n-Si–p-$Si_{1-x}Ge_x$ nanowire arrays for thermoelectric power generation

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ARTICLE INFO

Article history:
Available online 29 March 2013

Keywords:
SiGe nanowire array
thermo-electric generator
Si nanowire
Thermoelectricity

ABSTRACT

The output power of a discrete assembly of n-Si–p-$Si_{1-x}Ge_x$ ($0 \leqslant x \leqslant 0.4$) thermoelectric generators is measured as a function of load resistance. The influence of Ge content and nanowire structures on the performance of thermoelectric devices is evaluated in measurements around room temperature. The nanowire arrays are etched using a metal induced local oxidation and etching process, based on self-assembled Ag nanoparticles and HF. The use of nanowires and SiGe with dimensions smaller than 30 μm, is beneficial for an improvement of, at least, a factor of 10 in the output power. However, better performance improvements can be obtained by optimising the thermal and electrical contact resistances at the interfaces. Optimisation of the electrical contact results in a performance boost by a factor of 25.

1. Introduction

Thermoelectricity (TE) offers an excellent clean energy generation opportunity due to its lack of moving parts and simple fundamental structure based on pn-junctions. Progress in this field was hindered due to the Wiedemans–Franz law that describes the coupling between the electrical and thermal conductivity [1]. The low conversion efficiency and high costs currently limit its practical application. Much effort is still needed to enhance its efficiency and reduce its cost. However, with the introduction of nanotechnology, thermoelectric power generation is attracting renewed attention in the last few decades. It was shown that the replacement of bulk semiconductor materials by nanowires (NWs) can uncouple the electrical σ, and thermal κ conductivity [2] and thus boost thermoelectric performance. Nanostructures have been proven to greatly enhance the thermoelectric figure-of-merit (ZT) because of increased phonon scattering at the interfaces. It is well known that Si bulk, due to its high thermal conductivity, is a poor material for thermoelectric power generation. However, due to it ubiquitous use, research on Si based materials for TE is thriving. It has been demonstrated that single Si nanowires (NWs) exhibit a 60 times higher ZT than Si bulk [3]. Meanwhile, SiGe alloys can also reduce the thermal conductivity κ via alloy scattering [4] without deteriorating the other performance parameters such as Seebeck coefficient, S and electrical conductivity, σ. SiGe NWs thus promise to offer even better thermoelectric performance than SiGe bulk or Si NWs. The use of single NWs is an excellent approach to investigate their physical properties in function of geometrical parameters. However, in order to exploit the improvements of nano-materials in thermoelectric systems, a more straightforward structure is needed. We propose to use arrays of vertically upstanding Si or SiGe nanowires attached to a Si substrate as the legs in a thermo-electric generator (TEG). Some groups have already investigated the thermo-electric performance of arrays of nanowires [5].

In this work, we will show our recent research results on the fabrication and thermoelectric characterisation of SiGe nanowire arrays (NWAs) in a pn-junction TEG configuration. The NWAs are arrays of millions ($\sim 10^7$) of parallel upstanding NWs attached to Si bulk, rather than single NWs as studied before.

The manuscript is organised as follows: in Section 2, material preparation will be explained and in Section 3 the set-up and its influence on the measurements. In Section 4 we give the output power as a function of load resistance for different pn-leg TEG configurations including SiGe NWAs with different Ge concentration. In Section 5 we show the influence of optimising the electrical contact characteristics and conclude in Section 6.

2. Material preparation

Three wafers were prepared with a relaxed $Si_{1-x}Ge_x$ layer grown epitaxially on lowly doped p-Si (100) substrates using reduced pressure chemical vapour deposition (RP-CVD) [6] In the first step, a linearly graded relaxed $Si_{1-x}Ge_x$ layer (3–4 μm) was deposited to overcome the lattice mismatch between Si and SiGe, followed by a 2 μm thick constant composition layer. The constant composition layer contains x = 20%, 30% and 40% per wafer. EDX measurements confirm the Ge concentration to be respectively 22%, 30.9% and 44.4%. The SiGe layer is unintentionally p-doped.

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http://dx.doi.org/10.1016/j.sse.2013.01.038

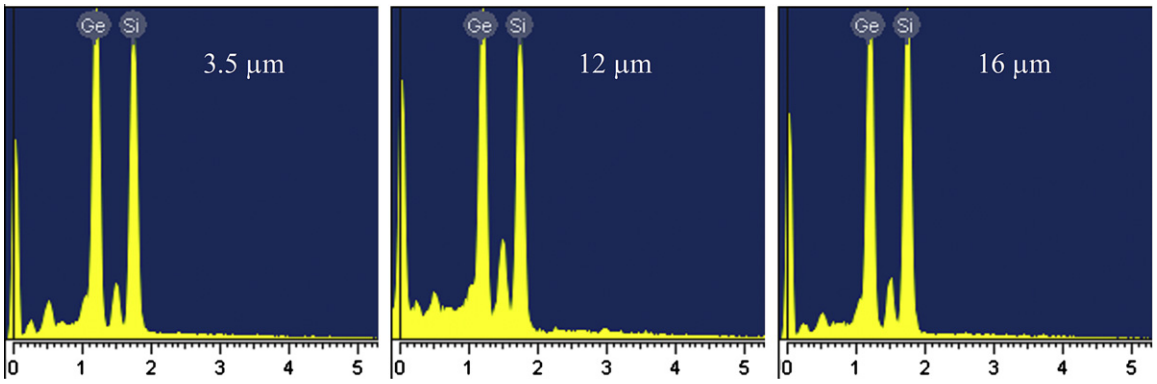

Fig. 1. EDX results for the $Si_{0.7}Ge_{0.3}$ sample for an etch time of, from left to right 15 min, 60 min and 4 h. The corresponding lengths are 3.5, 11 and 16 μm.

The resistivity of the p-Si substrate for the SiGe containing samples was measured by the four-point-probe technique [7] on samples from which the SiGe layer was removed and is found to be $\rho_{Si} = 2.7\ \Omega$ cm. The resistivity of the material is chosen to be relatively high in order not to interfere with the nanowire fabrication process. For thermo-electric power generation however, the free carrier concentration in the layers should be higher to increase the electrical conductivity [1]. In Section 5, we shall demonstrate the performance improvement of the output power of Si NWAs obtained by decreasing the wafer's resistivity.

Metal assisted chemical etching (MACE) [8] is known to offer a simple and cost-effective way to prepare large-area arrays with long vertically upstanding crystalline Si NWs. In this process Ag nanoparticles (NPs) are first deposited on the Si surface in a $AgNO_3$ (0.06 M):HF (40%):H_2O solution with a volume ratio of 2:5:13, followed by a Si etch in an HF (40%): oxidising agent mixture that is catalysed by the Ag NPs. For the Si NWs prepared for these experiments we have used HF (40%):H_2O:H_2O_2 (0.6 M) with a volume ratio of 2:1:1. This etch is selective along the [100] directions, forming crystalline (depending on the concentration of the oxidising agent) NWs with a diameter between 50 and 200 nm. The length of the NWs is controlled by the etch time and the availability of Ag NPs and oxidising agent. After etching, the residual Ag particles are removed by a solution of concentrated HNO_3 (5 M). Though MACE has proven successful with Si, SiGe is easily attacked by oxidising agents such as H_2O_2, resulting in the fast removal of the SiGe layer during the etching process. Experimental results show that MACE side etching firstly attacks the defect-rich relaxed $Si_{1-x}Ge_x$ buffer layer, under-etching the NW structure [9]. We have adapted the etching process to avoid the removal of the SiGe layers during chemical etching of SiGe NWs. A single stage $AgNO_3$ (0.06 M):HF (40%) solution with a volume ratio of 1:1 can be used for the etching of SiGe NWs. We have shown that arrays of $Si_{1-x}Ge_x$ NWs with x up to 40% can be fabricated using this 1-step MACE [10]. SEM and energy-dispersive X-ray spectroscopy (EDX) techniques are used to characterise the SiGe containing NWAs. The EDX results indicate that the SiGe NWAs are properly prepared with limited side etching using the 1-step MACE, even for longer etching times. This is illustrated for the 30% SiGe sample for different lengths of the NWs in Fig. 1. Fig. 2a shows an SEM cross section of the NWA. The etch rate decreases non-linearly with increasing Ge concentration for the same etch conditions, given in Fig. 2b for an etch time of 15 min. and for the same chemical recipe. For short etch time, the etch rate is limited by the Ge concentration. For longer etch times, the etch rate is limited by the supply of chemicals and Ag NPs.

3. Measurement set-up

Due to the sub-mm thickness of the semiconductor samples that form the TEG, a set-up has been built to allow contacts for temperature and voltage measurements. A schematic drawing of the setup is given in Fig. 3. Two small Cu blocks, with an area of 2 cm × 2 cm and thickness of 0.5 cm, are used as independent bottom contacts to each sample which have each a cross sectional area of 1.5 cm × 1 cm. For the NWA side, the effective transport cross sectional area reduces by approximately 50%. A larger Cu block is used at the hot side to form the electric contact between the two semiconductor samples. This places the two semiconductor sam-

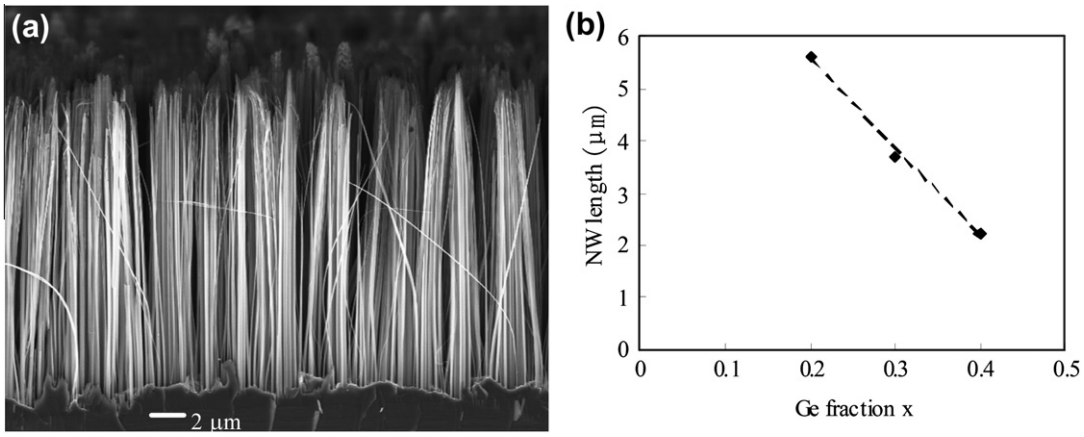

Fig. 2. (a) SEM cross section of a $Si_{0.6}Ge_{0.4}$ NWA. (b) The length of the NWs for an etch time of 15 min as a function of Ge concentration etched with the same chemical recipe.

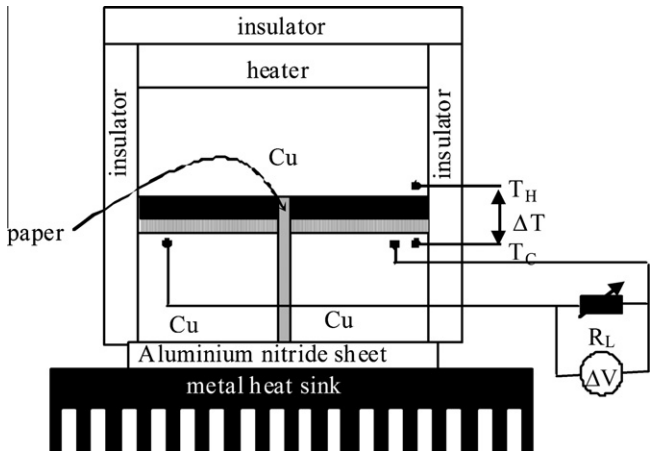

Fig. 3. Schematic drawing of the set-up to measure the thermo-power of the TE leg. The sample is the black and vertically hatched structure between the Cu blocks.

ples electrically in series and thermally in parallel. The Cu blocks also provides contacts for the Cu/constantan thermocouples connected to a Fluke 52II digital thermometer and the Cu leads connected to a high impedance Keithley 2000 multimeter and/or load. For this, two small (~1 mm diameter) holes are drilled in the Cu approximately 1 mm away from the interface. In order to decrease the electrical and thermal resistance between the Cu blocks and the TEG, a pressure of around 270 N is applied in all measurements. Two screws are used in order to create a more homogeneous pressure on the system. No metal contacts are evaporated onto the TEG legs to prevent large temperature drops due to the metal–metal interface roughness which have been found to be larger than the Cu-block – semiconductor thermal contact resistance [11]. An aluminium nitride layer is used as efficient thermal conductor and electrical insulator. This ensures that the cold temperature, T_C is the same for both TEG legs. In order to improve this feature, the samples are placed very close together and are insulated electrically and thermally by a sheet of paper. A 10 cm × 10 cm black metal heat sink with cooling fins is used to cool the cold side. The sides of the TE structure are insulated with a 0.5 cm thick layer of polystyrene and the setup is placed in a glove box at atmospheric pressure and room temperature to prevent influences from external air flow variations. Heat is provided by a power resistor clamped to the top of the structure. For all measurements, the power in the resistor is the same, thus keeping the supplied heat flux the same.

The mechanical pressure contact in this discrete set-up will cause both a thermal as well as an electrical contact resistance. The thermal contact resistance is a result of both the nano/micro roughness of the semiconductor and the metal, as well as the phonon momentum discontinuity between the different materials.

In order to evaluate the impact of these interface resistances, experiments have been performed. It is well known that to reduce the thermal contact resistance a thin layer of Ag foil can be used. This layer reduces the air gaps between the materials and is an excellent thermal conductor. The results of the measurements with and without foil give an indication of the temperature drop that will occur across the interfaces. The results of the temperature difference as a function of the power measured by heat flux sensor – which is placed between bottom copper block and heat sink – is given in Fig. 4a. At the highest thermal input power, the temperature drop across the interfaces is of the order of 50% of the externally measured temperature difference. The electrical performance is measured via current–voltage measurements at room temperature using an Agilent 4155B semiconductor parameter analyser. These measurements show that the Cu–semiconductor pressure contacts have a non-linear character due to the work function difference between semiconductor and Cu and the nano-air gaps at the junction. The extracted resistances are of the order of kΩ in the forward bias direction. The current–voltage characteristics are given in Fig. 4b. The resistance for the NWA samples is smaller since under pressure, the tops of the NWs collapse and form a better contact. The SiGe sample gives an even lower resistance due to the smaller work function difference between SiGe and Cu.

4. TEG measurements

4.1. Measurement of the Seebeck coefficient

For the measurements of the Seebeck coefficient, S, a set-up similar to that in Fig. 3 is used with an electrical open circuit. In order to improve the accuracy of the extraction, the open circuit voltage ΔV is measured for different values of the temperature difference, ΔT across the structure. S is then derived from the gradient: $S = \frac{\Delta V}{\Delta T} S$ of the samples is thus measured with respect to Cu. S_{Cu} = 1.84 μV/K, negligible compared to S for semiconductors. Since the measurements are done relative to Cu, the gradient of the ΔV–ΔT graphs (see Fig. 5) is opposite to the sign of S of the semiconductor samples. The offset in ΔV for ΔT = 0 K is due to internal electric fields build-up via charge accumulation at the contacts caused by the very high input impedance voltmeter. It is useful to note

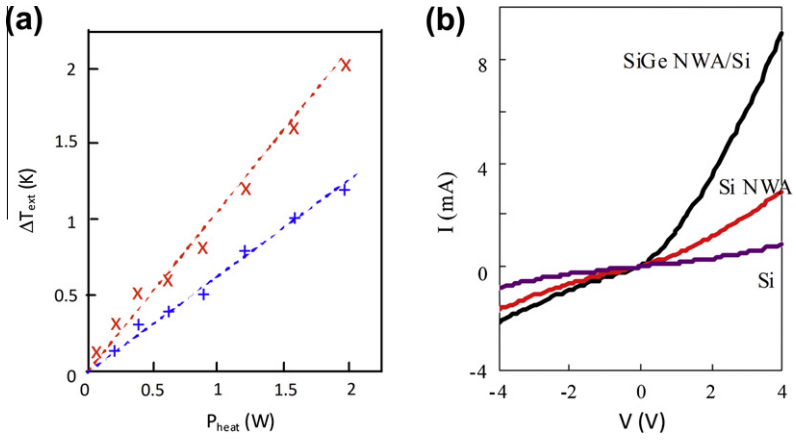

Fig. 4. (a) Measured temperature difference ΔT_{ext} as a function of heater power P_{heat} for a SiGe NWA sample between two Cu blocks without (×) and with (+) Ag foil at the interfaces. The markers are the measurements, the dashed lines are a guide to the eye only. (b) The current–voltage characteristics for the SiGe NWA, the Si NWA and the Si bulk sample. No Ag foil was used in these measurements.

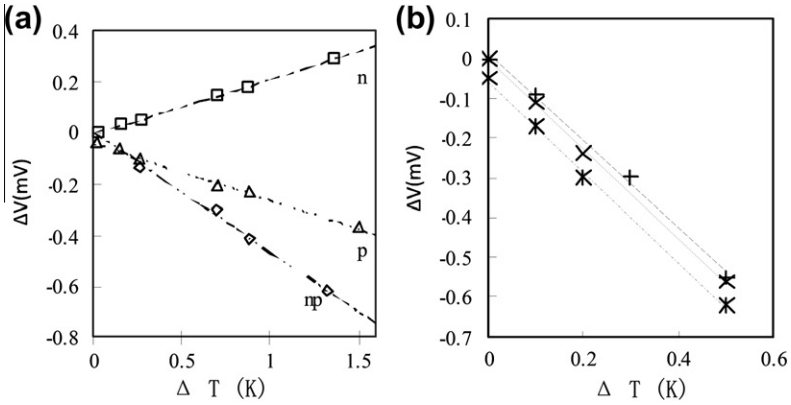

Fig. 5. Measurement of the Seebeck coefficient. (a) For the individual Si n (dashed) and p (dotted) NWA and the np junction (dashed–dotted) made with the same material. No Ag foil is used and no pressure is applied. (b) For all three SiGe samples containing a SiGe NWA array. Ag foil is used to minimise the temperature drop across the interface and a pressure of 250 N is applied. ×: $x = 0.2$, ⁕: $x = 0.3$ and +: $x = 0.4$.

Table 1
Length of the NWs, L_{NWA}, the measured Seebeck coefficient, S for the different Ge concentrations and the effective Seebeck coefficient, S_{eff} that takes into account the temperature drop at the interfaces.

Material	L_{NWA} (μm)	S (mV/K)	S_{eff} (mV/K)
n-Si	15	−0.21	−1.05
p-Si	16	0.22	1.1
pn-Si	16/15	0.47	2.35
$Si_{0.8}Ge_{0.2}$	14	1.12	/
$Si_{0.7}Ge_{0.3}$	12	1.14	/
$Si_{0.6}Ge_{0.4}$	18	1.01	/

that this offset voltage together with the stability of the voltage measurement at $\Delta T = 0$ K, is a good material control parameter. For NWAs with a highly porous character – as a result of the etching process – ΔV was observed to be high and measurements at $\Delta T = 0$ K unstable. This is caused by the high resistance of the NWA when porous in character. Fig. 5a gives the measurement of S for an n and p-type Si NWA with NW length of resp. 14.72 μm and 16 μm. The extracted S is given in Table 1. These measurements were done without Ag foil and without pressure which results in a ∼80% temperature drop across the interfaces between sample and Cu [9]. As a consequence, the extracted values for S are too low as the effective ΔT across the sample is ∼20% of the measured one. Taking this into account gives more realistic values of S for a substrate resistivity of $\rho_{Si} = 5.6\ \Omega$ cm from which these NWA are made. The estimated effective S, S_{eff} is given in Table 1.

The choice to measure S without pressure and Ag foil, is imposed by the need to re-measure the same samples in a pn-junction configuration. Due to the combination of Ag foil and pressure on the NWAs, removal of the sample from the set-up also removes the NWAs from the Si substrate as they remain stuck to the Ag foil. The measurement results of the pn junction can also be found in Fig. 5a and Table 1. We expect that the total S_{tot} for the pn junction is the sum of that of the individual n and p junction. We find $S_{tot_{eff}} = 2.35$ mV/K, while the sum $S_{tot_{eff}} = |S_{n_{eff}}| + |S_{p_{eff}}| = 2.15$ mV/K, reasonably close to the expected value.

Similar measurements have been carried out for the SiGe NWAs for the different Ge concentrations. In this case, samples were not re-used and therefore both Ag foil and a pressure of 250 N could be applied. The results are given in Fig. 5b and Table 1. S of the SiGe NWA samples have a similar magnitude and are also similar to that of Si NWA. This is not surprising as literature shows that S does not vary as a function of Ge concentration and moreover, the length of the NWAs is much smaller than the thickness of the remaining bulk.

4.2. Measurement of the output power

The measurements of the output power, P_{out} were done as a function of load resistance, R_L using the set-up as drawn in Fig. 3. For the n-leg, Si bulk or NWA, as appropriate, was used in all cases.

For the p-leg the p-Si was replaced by the SiGe samples. The cross sectional area of all samples was approximately 1.5 cm × 1 cm. The lengths of the NWAs were kept at approxi-

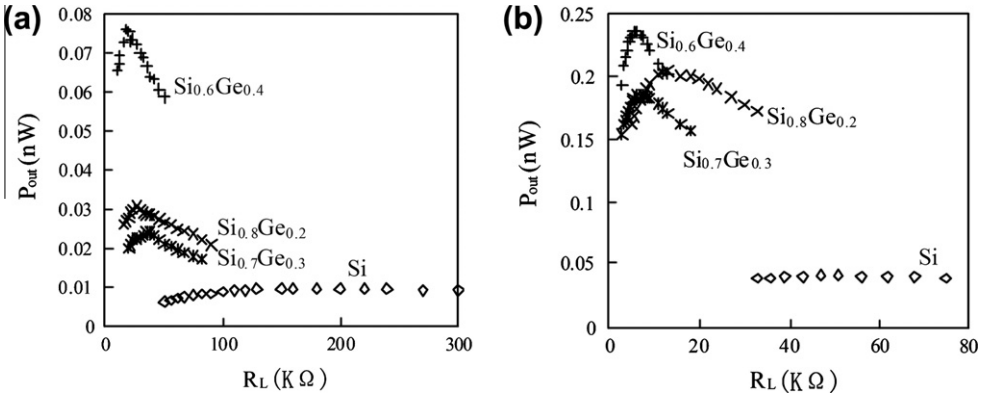

Fig. 6. Output power, P_{out} as a function of load resistance, R_L for four different pn-junction configurations. Labels: +: n-Si–p-$Si_{0.6}Ge_{0.4}$; ⁕: n-Si–p-$Si_{0.7}Ge_{0.3}$; ×: n-Si–p-$Si_{0.8}Ge_{0.2}$. (a) Bulk samples. (b) NWA samples.

Table 2
Performance parameters for the different TEGs: maximum output power, P_{out}^{max}, internal resistance, R_{int}, temperature difference, ΔT, open circuit voltage, V_{oc}, and NWA length, L_{NWA}. Subscript p and n in the last column indicate the doping type of the NWA.

Material	P_{out}^{max} (nW)	R_{int} (kΩ)	ΔT (K)	V_{oc} (mV)	L_{NWA} (μm)
Si bulk	0.01	160	2.4	2.85	0
Si NWA	0.04	51	2.6	2.98	$10_p/16_n$
$Si_{0.8}Ge_{0.2}$ bulk	0.03	30	2.8	1.9	0
$Si_{0.8}Ge_{0.2}$ NWA	0.2	13	3.3	3.28	$23_p/16_n$
$Si_{0.7}Ge_{0.3}$ bulk	0.02	39	2.8	1.81	0
$Si_{0.7}Ge_{0.3}$ NWA	0.19	7.5	3.3	2.4	$25_p/16_n$
$Si_{0.6}Ge_{0.4}$ bulk	0.08	20	2.9	2.32	0
$Si_{0.6}Ge_{0.4}$ NWA	0.24	6.2	3.3	2.38	$31_p/16_n$

mately the same value for all samples; differences in length will degrade the contacts or break the wires. The samples were clamped under pressure of 270 N but no Ag foil was used in order to allow repeated measurements.

This implies that the measured output power will suffer from a power reduction due to the thermal and electrical contact resistances at the Cu–semiconductor interfaces. Simulations of the influence of these interface resistances are presented in [12]. In the next section, the results of the investigations on the impact of the reduction of the electrical contact resistance will be presented.

The results of the measurements of P_{out} as a function of R_L are given in Fig. 6a for bulk and b for the NWA samples. These measurements follow the expected variation of P_{out} as a function of the load. The maximum output power is reached when the load, R_L is equal to the internal resistance, R_{int} of the TEG. R_{int} includes both the electrical contact resistances at the sample-Cu interfaces as well as the resistance of the sample itself. Since the thickness of the sample is only 500 μm, R_{int} will be determined by the contacts in these measurements [12].

From Fig. 6a we see that the SiGe alloy with the Ge content of 40% outperforms the others, attributed mainly to a better contact resistance. This changes for the NWA samples where the observed performance improvement of the 40% NWA is less than that of the 30% and 20% samples. We attribute this to a degradation of the SiGe layer upon NWA etch for higher Ge concentrations or the too high strain of the SiGe NWA due to the larger difference in length between the p and n leg in the TEG.

Table 2 summarises the most important parameters extracted from these measurements. It is clear that the contact resistance of the bulk sample is higher than that of the NWA samples. This is due to a poorer pressure contact on bulk than NWA because, under pressure, the tops of the NWAs bend and some break but also adhere strongly to the Cu. The contact resistance on the SiGe samples is found to be smaller than that on the Si sample. This is attributed to a lower work function difference between SiGe and Cu than Si and Cu. The performance of the SiGe containing samples is better than Si. This is due to both a better contact resistance on the SiGe samples as well as a higher temperature difference that is maintained in the SiGe samples. Changing a small part of the bulk into NWAs increases the output power by a factor of ~10, proving experimentally the performance increase to be gained from the introduction of even a small region of NWs. This improvement is a result of both an improved contact resistance as well as an improved ΔT across the NWA samples.

5. Optimisation of the Si TEG

As stated before, in order to improve the output power of the TEG based on thin material films, it is not only important to optimise the thin film itself – by including SiGe alloy and NWAs – the contacts to the external world have a severe impact on the performance.

In order to improve the thermal contact resistance, it was shown that Ag foil and pressure are effective in reducing the temperature drop across the interfaces. However, this approach is not a commercially sustainable one. An integrated structure with good thermal contacts is essential.

To improve the electrical contact resistance, standard microelectronics techniques can be applied.

Our approach to improve the contact resistance is to use spin-on-doping (SOD) on the bulk wafers before the NWAs are etched. Since the etch process is sensitive to the doping type and concentration in the wafers, adjustments to the recipe are essential in order to obtain sufficiently long NWAs of good material quality. The SOD approach before etch ensures that the top of all the NWs in the array will be heavily doped. The SOD process is done by spin coating of a boron/phosphorous solution on p/n type silicon surface followed by a 20 min. preheating on a hot plate at 200° and annealing at 900 °C in argon atmosphere for 20 min. to diffuse the boron/phosphorous into Si.

The output power of thermoelectric devices without and with Ohmic contact doping is given in Fig. 7a and b respectively. An excellent improvement of a factor of 25 in the output power is observed by reducing the contact resistance. We notice that the contact resistance of the bulk is much more reduced than that of the

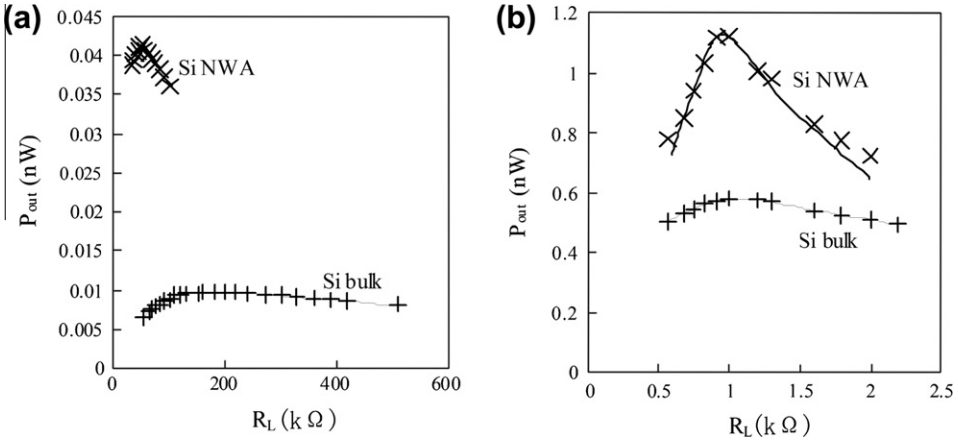

Fig. 7. Output power, P_{out} as a function of load resistance, R_L for Si bulk and Si NWA pn TEGs. The resistivity of the starting wafer is ρ = 5.6 Ω cm. Labels: +: Si bulk; ×: Si NWA. (a) No Ohmic contact doping. (b) Ohmic contact doping.

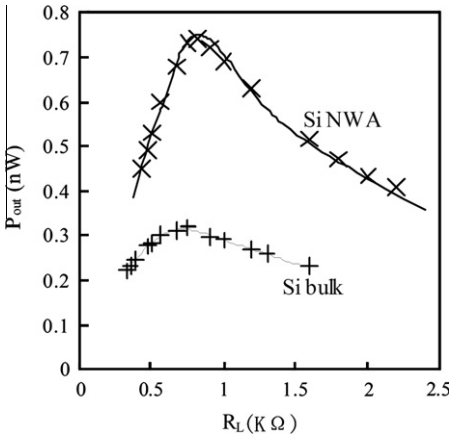

Fig. 8. Output power, P_{out} as a function of load resistance, R_L for Si bulk and Si NWA pn TEGs. The resistivity of the starting wafer is $\rho \approx 0.01\ \Omega$ cm. Labels: +: Si bulk; ×: Si NWA. No additional Ohmic contact doping.

Table 3
Performance parameters for contact doping and low resistivity samples in comparison to high resistivity sample performance.

Material	ρ bulk (Ω cm)	Contact doping	P_{out} (nW)	R_L (kΩ)
Bulk	5.6		0.01	160
NWA	5.6		0.04	51
Bulk	5.6	√	0.58	1
NWA	5.6	√	1.12	1
Bulk	0.01		0.32	0.75
NWA	0.01		0.74	0.82

NWA sample. This is because the contact area to the NWA is approximately 1/3rd of that of the bulk. This will always impose a limitation on the Ohmic contact improvement of the NWA structures. The length of the NWs is similar to that in Section 4. A pressure of 270 N is applied but no Ag foil is used for these measurements.

The second approach to boost the thermoelectric performance is an increase in carrier concentration. Again MACE on heavily doped material poses challenges and the recipe has to be adapted to allow for sufficiently long, good quality NWAs. In Fig. 8 we show the results for a starting wafer with a resistivity of $\rho \sim 0.01\ \Omega$ cm, approximately 500 times lower than previously used. Pressure on the contacts of 270 N is applied but no Ag foil, nor Ohmic contact doping was used.

An improvement of a factor of ~20 is obtained. For a higher doping, the open circuit voltage decreases due to a decrease of S with increasing carrier concentration. This is imposed by the classical Wiedemann–Franz relationship. Further improvements are possible by using SOD for Ohmic contact doping. Table 3 summarises some of the performance parameters.

6. Conclusion

The influence of Ge content and nanowire structures on the performance of thermoelectric devices is evaluated. The use of SiGe nanowires with a length less than 30 μm is beneficial for an improvement of at least a factor of 10 in the output power of the pn TEG. A better performance improvement can be obtained by using SiGe-based structures for both TEG legs as well as via optimising the electrical contact resistances at the interfaces. Optimisation of the Ohmic contact by spin-on-doping results in a performance boost by a factor of 25.

Acknowledgement

This work was financially supported by the *e-on* International Research Initiative project.

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