Fabrication of 2D Silicon Nano-mold Based on Sidewall Patterning

Helin Zou[1,a], Jie Rao[1,b], R.R.A.Syms[2,c], E Cheng[1,d]

[1] Research Center for Micro System Technology (MST), Dalian University of Technology, Dalian, China

[2] Optical and Semiconductor Devices Group, EEE Dept., Imperial College London, UK

[a] zouhl@dlut.edu.cn, [b] wsrj2008@hotmail.com, [c] r.syms@imperial.ac.uk, [d] snchenge@163.com

Keywords: Sidewall Patterning, 2D Silicon Nano-mold, Sputtering, Etch-back, Deep Reactive Ion Etching (Deep RIE)

Abstract: In the light of sidewall patterning technique, a photolithography-based process was described here to fabricate 2D silicon nano-mold. By combining the conformal deposition of Au-sputtering and anisotropic Deep RIE processes based on mixtures of SF_6, O_2 and C_4F_8 plasma, 200nm in width and 350nm in height silicon nanowire arrays can be routinely produced.

1 Introduction

Nanofabrication methods can be divided usually into two groups: bottom-up and top-down methods. Bottom-up methods begin with atoms or molecules to build up nanostructures, in some cases through smart use of selforganization[1, 2]. The method is mainly used for the formation of nanotubes and nanotunnels but not for network structure, therefore it's not suitable for nanofabrication. Top-down methods start with patterns made on a large scale and reduce its lateral dimensions before forming nanostructures, mainly including direct laser or focused beams writing[3-5], sacrificial layer surface-machining[6], nanoimprint lithography (NIL) [7, 8], chemical-mechanical polishing (CMP) [9], thermomechanical deformation[10], etc. However, these methods above require expensive equipment, complex processing or high fabrication costs, which have limited the development of nanofabrication technology.

Sidewall patterning is a process to define line patterns by using a sidewall spacer as an etch mask [11-13]. In this technique, by conformally depositing a material that has a different etching property over a lithographically defined pattern layer and selectively removing the deposited material, the sidewall material is preserved and can serve as nanopattern mask for further processing. The resolution of this method is not limited by photolithography but by the thickness of the material deposited. In this respect, the sidewall patterning technique makes it possible to form very fine line patterns without the need of e-beam technology equipment. From the economic point of view, it is competitive and has an obvious advantage in accuracy, uniformity and reproducibility.

In this paper, a method based on sidewall patterning technique to fabricate 2D silicon nano-mold over a full wafer is presented. The process delivers nano-structures over a large area, and can be adapted to comprise various geometries by conformal deposition and RIE and to meet specific needs by modifying the photolithography mask design.

2. Experimental

2.1 Experimental materials and equipments

100-mm, n-type (100) silicon wafers with a thickness of 0.5 mm was used as the starting material. After the wafer was pretreated with HMDS as an adhesion promoting layer from the gaseous phase on the heated substrate, the positive photoresist (AZ 701) with a thickness of 500 nm was coated on it. Then the wafer was delivered into the process of sidewall patterning, shown in Fig. 1.

The main equipments include: mask aligner(SUSS MicroTec MA/BA6)for lithography, thin film deposition system(Kurt J. Lesker LAB18) for aurum sputtering, ICP (ALCATEL AMS100SE) etcher system for DRIE,

scanning electron microscope(JEOL JSM-6360LV), surface profiler (Kosaka Laboratory Surfcorder ET 4000M,), plasma unit with RF generator(Quorum/Emitech K1050X) for photoresist removing.

2.2 Sidewall patterning

The side wall process consists of the following steps, shown in Fig. 1: (a) The AZ 701 positive photoresist is spin coated on the wafer with a thickness of 500 nm which has treated with HMDS as an adhesion promoting layer, then the wafer is exposed to UV light and the photoresist is developed into arrays composed of lines with a width of 2um, which is the formation of photoresist mesas; (b) A layer of aurum with a thickness of 200 nm is conformally deposited over these mesas by sputtering; (c) The aurum material is selectively removed from horizontal surfaces by argon-ions bombarding in the Kurt J. Lesker LAB18 thin film deposition system. The remaining vertical surfaces then act as the sidewalls, whose width is about 200 nm and height 500 nm; (d) The photoresist mesas are removed by oxygen plasma with silicon exposed; (e) The wafer is etched to a depth of 200 nm by DRIE process through a mask of aurum sidewalls; (f) A 2D silicon nano-mold is formed after removing the aurum mask.

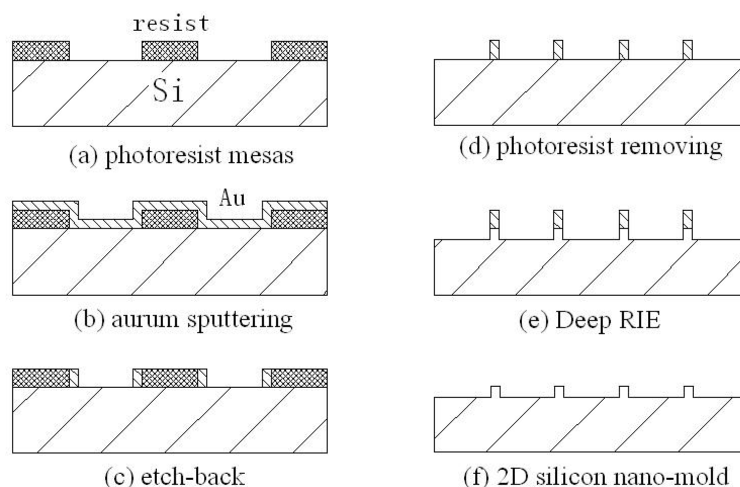

Fig. 1. Schematic diagram of sidewall patterning process

2.3 Sputtering and etch-back

Sputtering and etch-back both take place in the Kurt J. Lesker LAB18 thin film deposition system. In the process of sputtering, the target of aurum material acts as a negative electrode and metal cylinder of the sputtering chamber as positive electrode, argon-ions then bombard the targets in electric field. After a layer of aurum with a thickness of 200 nm has been deposited over the mesas by sputtering, the wafer holder acts as negative electrode and chamber cylinder as positive electrode, argon-ions then bombard the wafer, the aurum material is selectively removed, which is etch-back process, shown in Fig .1(c). In etch-back process, the horizontal and vertical surfaces have different etching rates over bombarding. After the horizontal surfaces were removed from the mesas by controlling etch time, we got aurum sidewalls of the left vertical surfaces, which formed the mask of subsequent Deep RIE process.

One set of typical parameters of aurum sputtering in our system is designed as follows: 140 sccm argon, 150 W power, 10 mTorr pressure, sputtered for 25 minutes. After measured by Kosaka Laboratory Surfcorder ET 4000M surface profiler, the thickness of aurum layer is 217 nm. The parameters of etch-back in our system are designed as follows: 140 sccm argon, 100 W power, 13 mTorr pressure, etched for 35 minutes.

2.4 Deep reactive ion etching

ALCATEL AMS100SE ICP etcher system is used for Deep RIE. SF_6/O_2 and C_4F_8 are poured into chamber alternately through gas inlet, shown in Fig. 2. The plasma source generates a very high density plasma by efficient

inductive coupling of radio frequency power at 13.56 MHz in a dielectric alumina cylinder. The high density plasma then diffuses into the diffusion chamber. Then the substrate holder (SH) electrode which controls the energy of bombarding leads the plasma downward to wafer in diffusion chamber. The distance between the plasma source and the substrate holder is set as 200 mm. In all of the experiments described below, the wafer temperature is cooled by a helium back side flow.

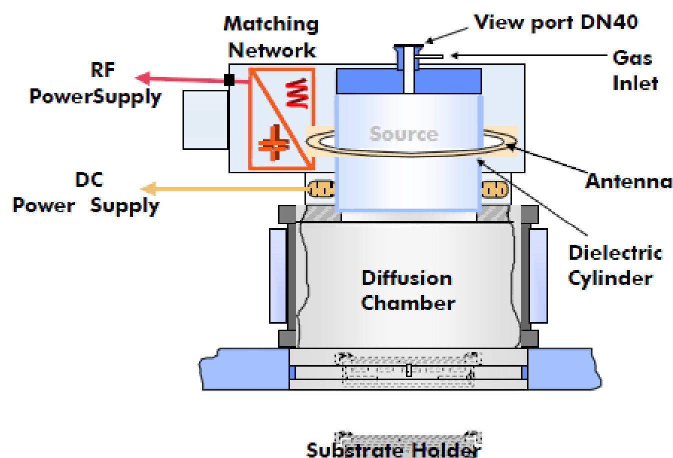

Fig. 2. Schematic diagram of ALCATEL AMS100SE ICP etcher system

One typical parameters table of DRIE process in our system is shown in Table 1. The distance between substrate holder and source electrode is 200 mm, and the temperature of diffusion chamber is kept at 10℃.

Table 1. One typical parameters table of DRIE process in our system

Values of Parameters	Main DRIE Parameters				
	Flow （sccm）	Cycle （s）	Pressure (mBar)	Source Power (w)	SH Power (w)
SF_6/O_2	140/7	3	0.019	1500	50
C_4F_8	125	2	0.024	1500	0

3 Results and discussion

Based on sidewall patterning technique, we successfully fabricated a 2D silicon nano-mold using a photolithography-based process, shown in Fig .3. The width and height of the silicon nanowires is separately 200 nm and 350nm, measured by JSM-6360LV scanning electron microscopy. By combining the conformal deposition of Au-sputtering and anisotropic Deep RIE processes, this method shows great potential in fabricating 2D silicon nano-structure.

4 Conclusions

In this paper, a method based on sidewall patterning technique to fabricate 2D silicon nano-mold over a full wafer is presented. 200nm in width and 350nm in height silicon nanowire arrays which formed silicon nano-mold can be produced. In our future work, PDMS will be cast on the silicon nano-mold for fabrication of 2D polymer nanochannels. By combining bonding between PDMS chips with nanochannels and other chips with microchannels, we will futher the investigation of micro- and nano-fluidic chips system.

5 Acknowledgement

This project is supported by National Natural Science Foundation (No.20890024).

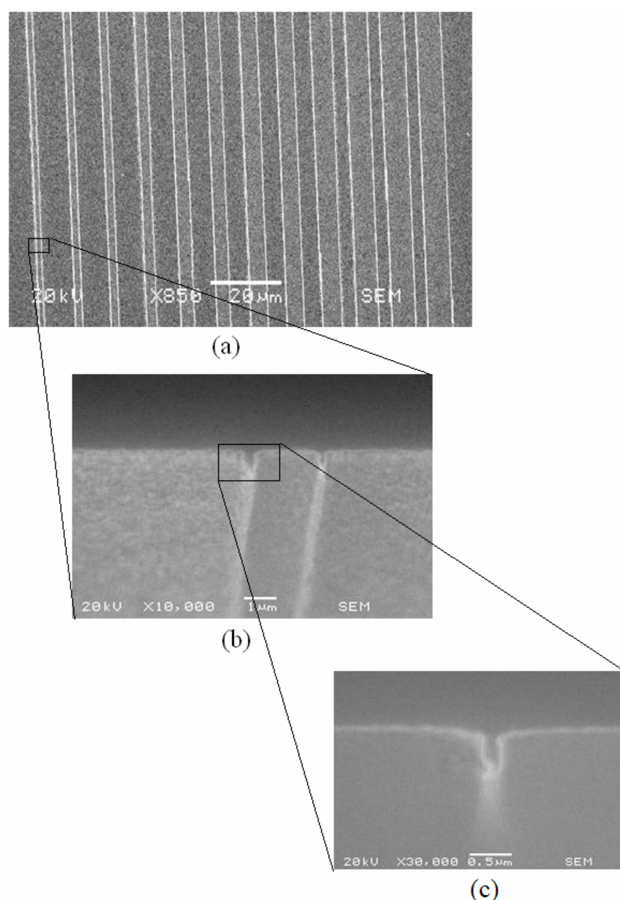

Fig. 3. SEM view of 2D silicon nano-mold. (a) top view of silicon nanowire arrays, (b) oblique view of nanowire cross section, (c) cross section view of nanowire with 200nm in width and 350nm in height.

Reference

[1] Xia, D.Y. and S.R.J. Brueck, J Vac Sci Technol B, 2005. **23**(6): p. 2694-2699.

[2] Zeng, Y. and D.J. Harrison, Anal Chem, 2007. **79**(6): p. 2289-2295.

[3] Rill, M.S., et al., Nat Mater, 2008. **7**(7): p. 543-546.

[4] Mahabadi, K.A., et al., J Micromech Microeng, 2006. **16**(7): p. 1170-1180.

[5] Shao, P.G., et al., Nucl Instrum Meth B, 2007. **260**(1): p. 479-482.

[6] Cheng, G.J., D. Pirzada, and P. Dutta, J Microlith Microfab, 2005. **4**(1): p. -.

[7] Yang, B. and S.W. Pang, J Vac Sci Technol B, 2006. **24**(6): p. 2984-2987.

[8] Cao, H., et al., Appl Phys Lett, 2002. **81**(1): p. 174-176.

[9] Lee, C., et al., Nano Lett, 2003. **3**(10): p. 1339-1340.

[10] Sivanesan, P., et al., Anal Chem, 2005. **77**(7): p. 2252-2258.

[11] Choi, Y.K., et al., J Phys Chem B, 2003. **107**(15): p. 3340-3343.

[12] Haneveld, J., et al., J Micromech Microeng, 2006. **16**(6): p. S24-S28.

[13] Zhang, Z., et al., Microelectron Eng, 2006. **83**(11-12): p. 2107-2111.