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Excited states and quantum confinement in room temperature few nanometre scale silicon single electron transistors

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Abstract

Single nanometre scale quantum dots (QDs) have significant potential for many 'beyond CMOS' nanoelectronics and quantum computation applications. The fabrication and measurement of few nanometre silicon point-contact QD single-electron transistors are reported, which both operate at room temperature (RT) and are fabricated using standard processes. By combining thin silicon-on-insulator wafers, specific device geometry, and controlled oxidation, <10 nm nanoscale point-contact channels are defined. In this limit of the point-contact approach, ultra-small, few nanometre scale QDs are formed, enabling RT measurement of the full QD characteristics, including excited states to be made. A remarkably large QD electron addition energy $\sim$0.8 eV, and a quantum confinement energy $\sim$0.3 eV, are observed, implying a QD only $\sim$1.6 nm in size. In measurements of 19 RT devices, the extracted QD radius lies within a narrow band, from 0.8 to 2.35 nm, emphasising the single-nanometre scale of the QDs. These results demonstrate that with careful control, 'beyond CMOS' RT QD transistors can be produced using current 'conventional' semiconductor device fabrication techniques.

Supplementary material for this article is available online

Keywords: single electron transistors, quantum dot, nanodevices, room temperature single electron effects

(Some figures may appear in colour only in the online journal)

1. Introduction

Developing quantum electronics into a practical technology requires devices at the single-nanometre scale, which both operate at room temperature (RT) and are manufacturable. Single nanometre quantum dots (QDs) [1] have great potential in this regard, for applications in 'beyond CMOS' nanoelectronic circuits [2], quantum computation [3], single molecule sensing [4], and energy scavenging [5]. QD transistors are particularly attractive because, unlike 'classical' transistors, a reduction in size inherently improves their performance. QDs may now be defined towards the single

nanometre scale, or even by a single donor atom [6], of great interest for quantum computation devices [3].

Single-electron transistors (SETs) operating at RT, where the presence of a sub-10 nm scale 'island' or QD for single-electron charging is essential, have been reported by several groups using various approaches. These include QDs formed 'naturally' within Si nanowires in the presence of surface roughness or doping disorder [1, 7–10], high-resolution lithographic and pattern dependent oxidation of nanowires and point contacts to define QDs in a more controlled manner [11–13], Si nanocrystals and nanochains using QDs formed by material synthesis [2, 14–16], and ultrathin Si channels

where surface roughness forms QDs [17]. In recent work, RT SETs based on ~10 nm Si nanowires with omega gates have been demonstrated using completely standard CMOS based processing [10], demonstrating that a direct transition from classical Si transistors to RT quantum effect devices is possible. High-resolution lithography is essential for many of these approaches, either to pattern the QDs directly, or in combination with material synthesis methods. However, while these works all show RT Coulomb blockade, direct observation of excited states at RT is lacking. Furthermore, in most of these devices, QDs are still created randomly, though a single QD may be dominant, or parasitic QDs exist in addition to those defined intentionally by lithography. The problem becomes more significant the greater the volume within which QDs may form. Using a point contact [13, 14] greatly limits the device volume available where a QD can be formed, such that single QDs become more likely. Finally, even though the QD may be a 'random' structure, for example a single dopant atom or Si nanocrystal within the point-contact, such a structure is inherently smaller in size and has higher charging energy than QDs defined purely by lithographic methods.

This paper shows that in the limit of the point-contact approach, it is possible to form ultra-small, few nanometre scale QDs, where the full QD characteristics, including excited states, are measurable at RT. By combining thin silicon on insulator (SOI) wafers, specific device geometry, and controlled oxidation, it is possible to define <10 nm nanoscale point-contact channels using 'conventional' techniques. These are small enough to allow a dominant QD associated with a Si nanocrystal, or a dopant atom [6], to be addressed. A remarkably large QD electron addition energy ~0.8 eV, and a quantum confinement energy ~0.3 eV, are observed, implying a QD only ~1.6 nm in size. These large values enable RT observation not only of Coulomb blockade, but also of resonant tunnelling through excited states. In measurements of 19 RT SETs, the likelihood of finding one of these devices is seen to increase with reduction in point-contact size to the ~10 nm scale, and the extracted QD radius is found to lie within a narrow band, from 0.8 to 2.35 nm. At these scales, in addition to the single-electron charging energy, the effect of quantum confinement and resonant tunnelling effects on the electrical characteristics cannot be ignored. Finally, it is seen that the QD radius tends not to reduce as the point-contact dimensions are reduced, supporting a picture where the QD is associated with the material properties such as donor atoms, rather than directly with the point-contact size.

2. Device fabrication

The point-contact devices were fabricated using electron beam lithography and a 'geometric oxidation' process in (100) oriented, degenerately doped SOI chips, either with a ~20 nm thick top Si layer doped n-type at ~10^{20} cm^{-3}, or with an ultra-thin 12 ± 1 nm thick top Si layer doped n-type at 5×10^{20} cm^{-3}. A trench isolated and oxidised Si point-

contact pattern facilitated the formation of QDs smaller than the lithographic limits (details of fabrication methods are given in supplementary material available online at stacks. iop.org/NANO/28/125208/mmedia). Schematic diagrams of the device structure and QD formation through controlled oxidation are shown in figures 1(a) and (b). Scanning electron micrographs of SETs after oxidation are shown in figure 1(c) in (d), where the later provides a high-resolution plan view. In (d), the minimum point-contact width is 37 nm. For this device, oxide layers ~15 nm thick were grown, such that an un-oxidised channel with a nominal width of ~7 nm remained. The oxide thickness was chosen such that for the point where point-contact width is minimum, the SiO$_2$ layers growing from the Si surfaces were close to contact with each other, ensuring the smallest possible un-oxidised Si volume. Here, in contrast to a scaled 'nanowire' device configuration, the point-contact configuration minimises the length separating the source from the drain, allowing electron tunnelling to occur. With the point contact geometry, stress and quantum confinement in the Si means that as the SiO$_2$ regions develop the surfaces may overlap to leave an un-oxidised Si island QD [18]. However, as the average inter-dopant separation is only ~2 nm, when the point-contact is oxidised and the Si core is reduced to this scale, it is also possible that a single dopant atom, or a few dopant atoms, within the core may define one or a few QDs [6]. If the QD size is sufficiently small (<10 nm), the QD addition energy E_a and any excited states are ≫ $k_B T$ (= 25 meV at 290 K) such that these states control electron tunnelling across the QD and SiO$_2$ tunnel barriers even at RT. At RT, thermally excited electrons from the Boltzmann tails of the Fermi–Dirac distribution in the source region contribute strongly to the tunnel current, leading to a regime which is very different from typical measurements on larger SETs at low temperature.

3. Experimental results

The (RT = 290 K) drain–source current (I_{ds}) versus drain (V_{ds}) and gate (V_{gs}) voltage 'Coulomb diamond' characteristics [19–21] for a single nanometre scale QD (QD1) are shown in figure 2. All measurements are performed using an Agilent 4155B parameter analyser. Here, the QD diameter is estimated to be only ~1.6 nm (value extracted from electrical characteristics, see below). The characteristics are plotted (a) using a 3D plot, and (b), as $\log|I_{ds}|$ versus V_{ds}, V_{gs}. The drain–source differential conductance g_{ds} versus V_{ds}, V_{gs} characteristics are shown using 3D (c) and colour scale (d) plots. Multiple Coulomb diamonds, seen clearest in (d), and Coulomb staircases, seen clearest in (a), are observed in the characteristics. Within the Coulomb gap, I_{ds} is strongly suppressed by Coulomb blockade to within the measurement noise floor (~1 pA). However, noise peaks inherent to the device at the ~10 pA scale are seen at some gate voltages, e.g. these are more prominent for V_{gs} values from 6.5–8.5 V. In comparison with QD measurements at cryogenic temperatures, as our measurements were at much higher (room) temperature, thermally activated stochastic charging of defect
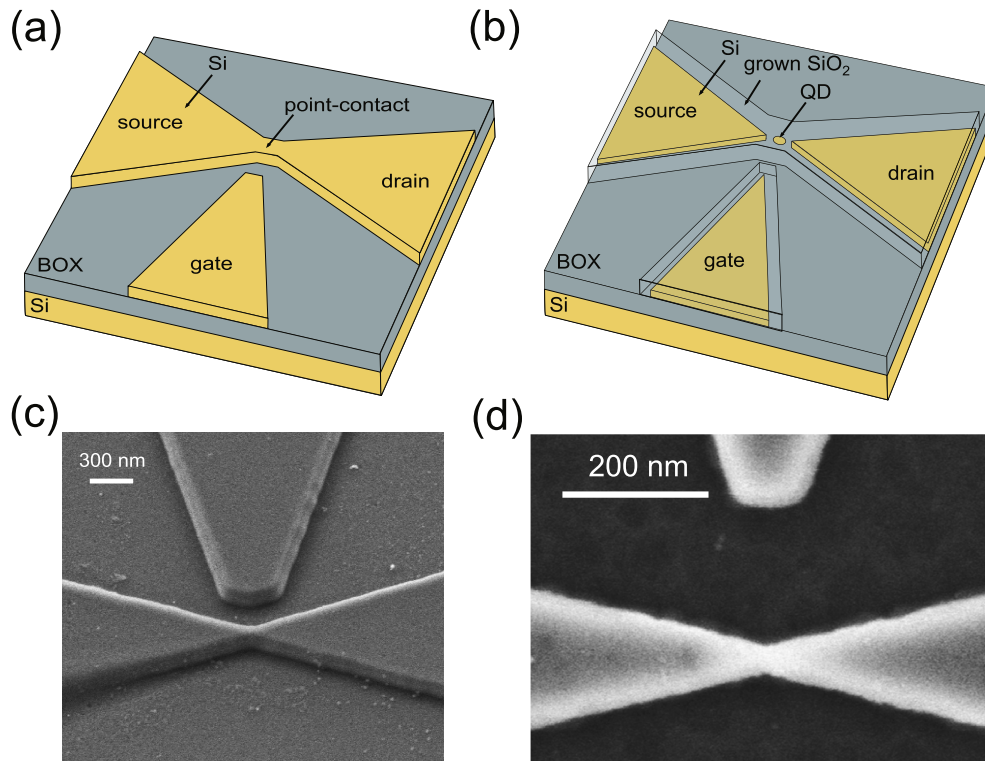
Figure 1. Device fabrication. (a) Schematic diagram of a silicon-on-insulator wafer with n-type, degenerately doped ($>10^{20}$ cm^{-3}) top silicon thinned to 20 nm or less, defined by electron beam lithography, and plasma etched to leave a narrow point contact. (b) Following oxidation at 850 °C, the silicon is both thinned and a quantum dot (QD) formed between the source (S) and drain (D). A side gate (G) controls the QD characteristics. (c) Scanning electron micrograph (SEM) of the final device, taken at high angle to show the etched and oxidised device structure on the buried oxide (BOX). The QD is encapsulated within the oxide at the centre of the S/D contacts. (d) A second device seen at higher magnification, from a plan view orientation.

states nearby the QD can occur, leading to noise in the device. Figure 2(e) shows single-electron oscillations in I_{ds} versus V_{gs}, for constant V_{ds} values. A large peak–valley ratio $\sim$10 is observed, e.g. for the negative current peaks at $V_{gs} = 1.5$ and 3 V. The I_{ds} magnitudes and oscillation peak heights are greater for negative V_{ds} bias, due to a small diode-like asymmetry in the characteristics.

Resonant tunnelling occurs through QD excited states [22], even at RT, in the device. In figures 2(c) and (d), differential conductance peaks running parallel to the Coulomb diamond edges are seen e.g. indicated by arrows in (c), and forming bright lines in (d), a signature of resonant tunnelling through excited states [19]. Given that these features run parallel to the diamond edges, both the diamonds and the features are associated with states in the same, dominant QD. For $V_{gs} < 4$ V, it is seen that the diamonds do not reduce to zero, implying either a potential barrier in addition to the QD, or a band offset between the energy at the base of the QD and the source conduction band edge. In the former case, the potential barrier may be associated with additional series QDs, i.e. a multiple tunnel junction (MTJ) system [9], or with a SiO$_2$ or depleted Si region in series with the dominant QD. The threshold voltage V_t for I_{ds} is then given by a combination of the voltage drop across this barrier and QD Coulomb blockade. The former is pulled down in energy as V_{gs} increases, reducing V_t. In the case of additional series QDs forming an MTJ, a dominant QD is still necessary to explain

the observation of resonant tunnelling lines running parallel to the diamond edges. Within the MTJ model, if multiple QDs of various sizes are capacitively coupled to the gate, this leads to the formation of subsidiary, smaller Coulomb diamonds lying between larger diamonds in the electrical characteristics [23]. In figure 2(d), the Coulomb diamond at $V_{gs} = 2.4$ V may be formed by this effect. Finally, vertical features, parallel to the V_{ds} axis are also observed in (b) and (c). These appear to have only weak, very limited dependence on V_{ds}, implying that the underlying level is decoupled from V_{ds}. These lines may be associated with charging of a defect state in the oxide in the proximity of the QD as V_{gs} is varied, or with an additional QD within an MTJ, where this is only weakly coupled to the drain, similar to doped nanowire SETs [9].

RT single-electron effects have been observed in multiple devices (19 devices), fabricated using 4 processing runs, on different samples. The characteristics from a second device (QD2) are shown in figures 3(a)–(c). Current oscillations with changing V_{gs} at V_{ds} values between $+0.4$ and -0.4 V are shown in (b) and multiple Coulomb diamond like features (c) can be identified (e.g. one of these is marked in (c)), corresponding to a large, one-by-one change in electron number N. As in QD1, a small diode-like asymmetry is seen in the characteristics, increasing the current magnitudes for negative V_{ds} values and creating a small asymmetry in the diamond shapes in (c). In comparison with QD1, any additional potential barriers or band offsets are less significant,
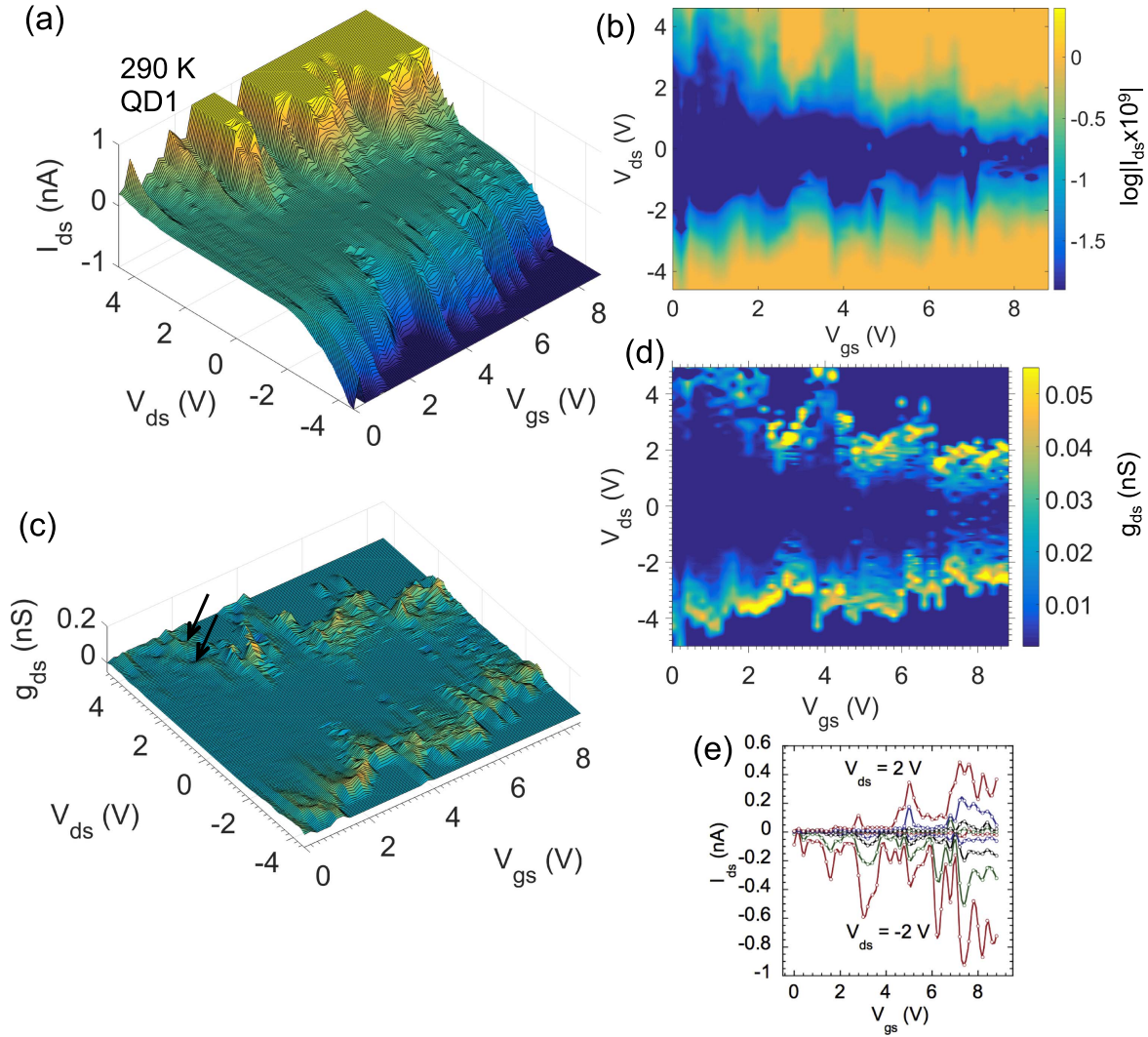
Figure 2. Room-temperature (RT = 290 K) drain–source current (I_{ds}) versus drain (V_{ds}) and gate (V_{gs}) voltage 'Coulomb diamond' characteristics for a point-contact QD device (QD1), with point-contact pre-oxidation width of ∼25 nm. I_{ds} in the measurement is limited to ±1 nA to avoid device damage. The characteristics are plotted (a) using a three-dimensional (3D) plot, and (b), $\log|I_{ds}|$ versus V_{ds}, V_{gs}, using a linear colour scale. (c) The drain–source differential conductance g_{ds} versus V_{ds}, V_{gs} characteristics, shown using a 3D plot, and (d) in a colour scale plot, with a linear colour scale for g_{ds}. (e) Oscillations in the device current I_{ds} versus V_{gs}, at values of V_{ds} between + 2 and −2 V.

with a minimum threshold voltage ∼ ±25 mV. However, a variation in Coulomb diamond size occurs, suggesting an MTJ is formed where the constituent QDs are gate-coupled [23]. Figure 3(d) shows a Coulomb diamond in detail, from an additional device (SET A) at 290 K. Here, any additional potential barrier is negligible as the diamond 'pinches-off' to zero width along V_{ds}, at $V_{gs} = 1.4$ and 1.8 V. This behaviour is less typical in our devices, where the fabrication process in likely to form an additional potential barrier creating a constant threshold voltage offset. The differential conductance at $V_{ds} = 0$ V changes from $g_{ds} \sim 60$ pS at $V_{gs} = 1.4$ V to $g_{ds} \sim 12$ pS at $V_{gs} = 1.6$ V.

A third quantum dot (QD3) has been fabricated in SOI material with a higher doping level (5×10^{20} cm^{-3}). This allowed electrical characteristics to be measured down to 150 K, below which an increasing device resistance prevented further measurements. The effect of temperature on the

electrical characteristics are shown in figure 4, with I_{ds} versus V_{ds}, V_{gs} characteristics at (a), (b) 290 K and (c) 150 K. Figure 4(b) shows in detail the I_{ds} versus V_{ds}, V_{gs} characteristics at 290 K (measured in a different cycle to (a)), around a region of Coulomb oscillations in I_{ds}, at a higher $|V_{ds}| \leqslant 4$ V. A rich structure is seen, with multiple step Coulomb staircase I_{ds}–V_{ds} characteristics (e.g. steps labelled 'A'), where the shoulders form diagonal lines (e.g. labelled 'B'). Resonant tunnelling current peaks may also be seen, with negative differential resistance regions, e.g. labelled 'C'. The device resistance is ∼20 MΩ outside the central potential barrier region, much lower than in QD1. Intermediate temperature dependencies are shown in figure 5, discussed in detail later. Arrhenius plots of $\ln(I_{ds})$ versus $1/T$ extracted from these are shown in figure 4(d) and the variation with V_{ds} of the activation energy E_A obtained from these is shown in (e). These characteristics, and those shown in figure 5 illustrate the
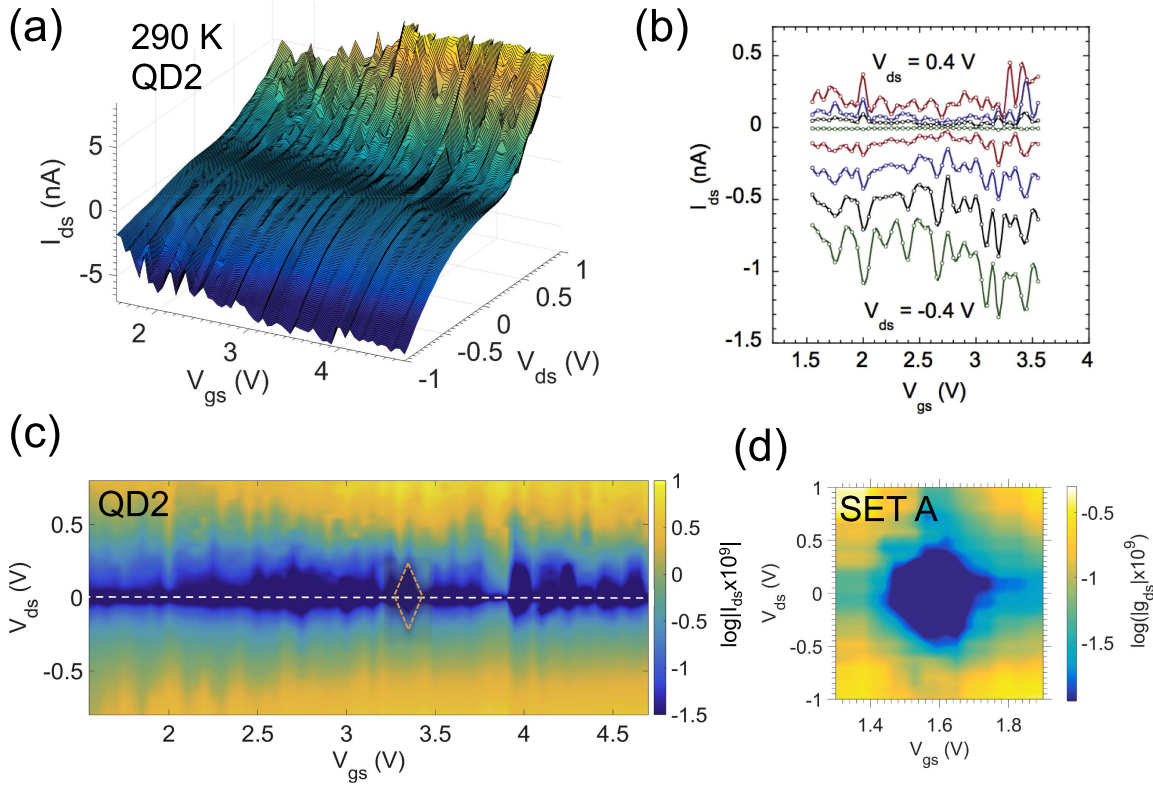
Figure 3. Electrical characteristics at RT for an additional device, QD2 (a) measurements of I_{ds} as a function of V_{ds} and V_{gs} at V_{ds} values between ± 1 V, shown using a three-dimensional (3D) plot. (b) Oscillations in the dependency of I_{ds} on V_{gs} at values of V_{ds} between $+0.4$ and -0.4 V. (c) The $\log|I_{ds}|$ versus V_{ds}, V_{gs}, characteristic of QD2 shown with a linear scale for $\log|I_{ds}|$. A large number of Coulomb diamonds are shown, with one highlighted as an example. (d) Coulomb diamond in an additional device (SET A) at 290 K. The diamond 'pinches-off' to zero width along V_{ds} at $V_{gs} = 1.4$ and 1.8 V.

combined effect of a QD and an additional potential barrier in our devices. As argued earlier, the potential barrier may be created by an MTJ, or by a SiO_2 region in series with or underlying the dominant QD. At RT (290 K) the potential barrier has only a limited effect, creating a small threshold voltage $V_t \sim \pm 0.15$ V approximately constant with varying V_{gs} (figure 5(a)). For For $|V_{ds}| > |V_t|$, Coulomb oscillations occur in I_{ds}. At low temperature (150 K), the effect of the potential barrier is much stronger as any thermally activated current is supressed, increasing $|V_t| \sim 1$ V. I_{ds} then rises sharply beyond this, as the contact resistance of the degenerate source, drain and lead-in regions reduces. Detailed changes also occur, e.g. in this device, some oscillations are supressed at $V_{gs} > 2$ V, possibly due to a change in the QD environment. The Arrhenius plot in figure 4(d) shows thermal activation of I_{ds} from 290 to 200 K. Linear fits to the data facilitate extraction of the activation energy E_A versus V_{ds}. It is seen that as V_{ds} decreases towards zero, E_A reduces. Extrapolation of a polynomial fit to the data (figure 4(e)) shows a minimum activation energy $E_{A1} = 0.125$ eV at $V_{ds} = 0$ V. Furthermore, E_A saturates at a maximum activation energy $E_{A2} \sim 0.235$ eV at $V_{ds} = -0.5$ V. As the potential barrier dominates at low bias, $E_{A1} = 0.125$ eV may be associated with the height of this barrier. This is shown schematically in figure 4(f), where a potential barrier with height $E_{B1} \sim E_{A1}$ exists in series with and on either side of a

dominant QD. At higher bias, $V_{ds} = 0.5$ V, the potential barrier is pulled down (figure 4(g)) and Coulomb oscillations are observed. $E_{A2} \sim 0.235$ eV may then be associated with the charging energy in the QD. We observe that for this device, $E_{A1} < E_{A2}$, i.e. the potential barrier is less significant than the charging energy to the electrical characteristics.

The evolution of the Coulomb diamonds in QD3 with decreasing temperature is shown in figure 5, with characteristics taken at 275 –200 K (a)–(d). A schematic representation of the variation in the central low current region (dark blue region in (a)–(d)) is shown in figure 5(e). For $|V_{ds}| > |V_t|$, Coulomb oscillations in I_{ds}, create triangular half-diamond features on either side (e.g. figure 5(a)). Four Coulomb diamond features (associated with the QD), offset by a central threshold region (associated with the potential barrier), are observed at (a) 275 K (b) 260 K (c) 220 K and (d) 200 K. It is seen that the centre threshold regions increases in significance with reducing temperature. Additional fine structure appears along the diamond edges at 220 K. The increasingly significant potential barrier begins to supress the diamond features by 200 K, though current oscillations still persist. The higher doping level of this sample reduces the height of any potential barriers along the current path. Furthermore, the source/drain contact resistance is improved, as the degenerately doped nature of the source and drain contact regions is
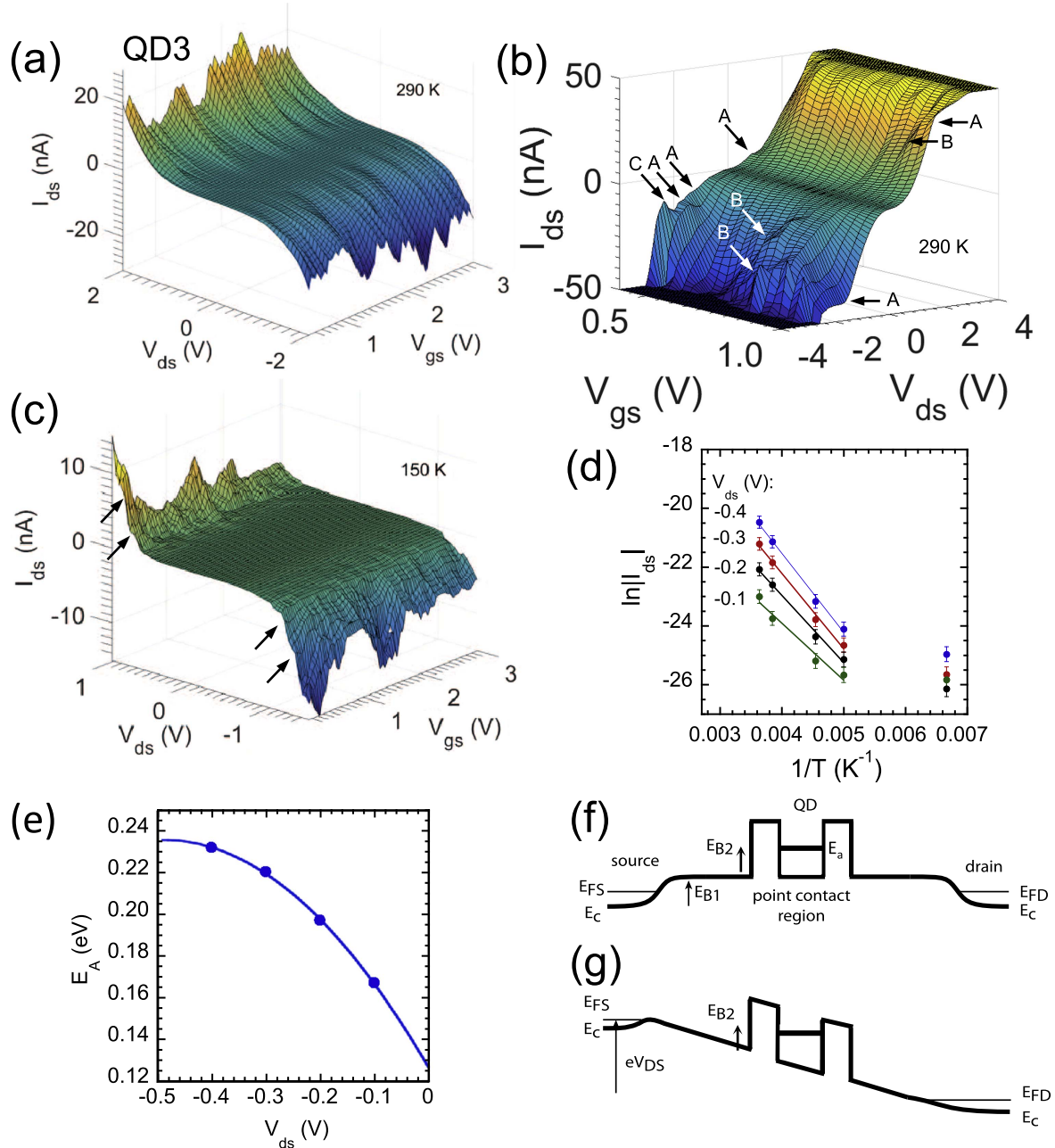
Figure 4. Temperature dependence of the electrical characteristics of QD3. (a), (b) Show the I_{ds} versus V_{ds}, V_{gs}, characteristic at 290 K and (c) at 150 K. (Further temperature dependence characteristics are shown in figure 5 where the variation of $\log|I_{ds}|$ with V_{ds}, V_{gs} is shown.) (b) Shows detail in the I_{ds}–V_{ds}, V_{gs} characteristics at 290 K (measured in a different cycle to (a)), around a region of Coulomb oscillations in I_{ds}. Coulomb staircase characteristics are observed, with arrows indicating (A) current steps, (B) lines formed along shoulders of steps and (C) current peaks. The Arrhenius plot in (d) shows thermal activation of I_{ds} from 290 to 200 K. Linear fits to the data allow extraction of the activation energy E_A as a function of V_{ds}, shown in (e). As the magnitude of V_{ds} decreases towards zero, E_A reduces and extrapolation of a polynomial fit to the data shows a minimum value of 0.125 eV at $V_{ds} = 0$ V. (f) A schematic band diagram showing the area of the point contact regions with an additional potential barrier, at zero bias, and under an applied bias (g).

maintained to a point closer to where doping concentration fluctuations become significant at the point-contact neck.

The variation of a current peak with temperature (along line 'A' in figure 5(a)), for a bias (0.4 V) at the edge of the central threshold region at 200 K is shown in figure 6(a) and at high V_{ds} bias (1 V, figure 6(b)). The thermal broadening for a current oscillation may be expressed as [19] $I/I_0 = A(\cosh^{-2}(|V_{peak} - V_{gs}|/Bk_BT))$, where V_{peak} is the peak position, $V_{peak} - V_{gs}$ indicates the offset to V_{peak}, k_B is

Boltzmann's constant, and A and B are constants. This function, plus a linear background, is used to fit the data in figures 6(a) and (b). The data predicts a linear dependence of the peak width (the denominator Bk_BT within the $\cosh^{-2}$ term above) with T, and this is seen to be the case (inset to (a)). Extrapolation of the fit suggests that in this device, the current peak would disappear by ~120 K. This implies that some of the available thermal energy at a given temperature is essential to overcome potential barriers in addition to the QD
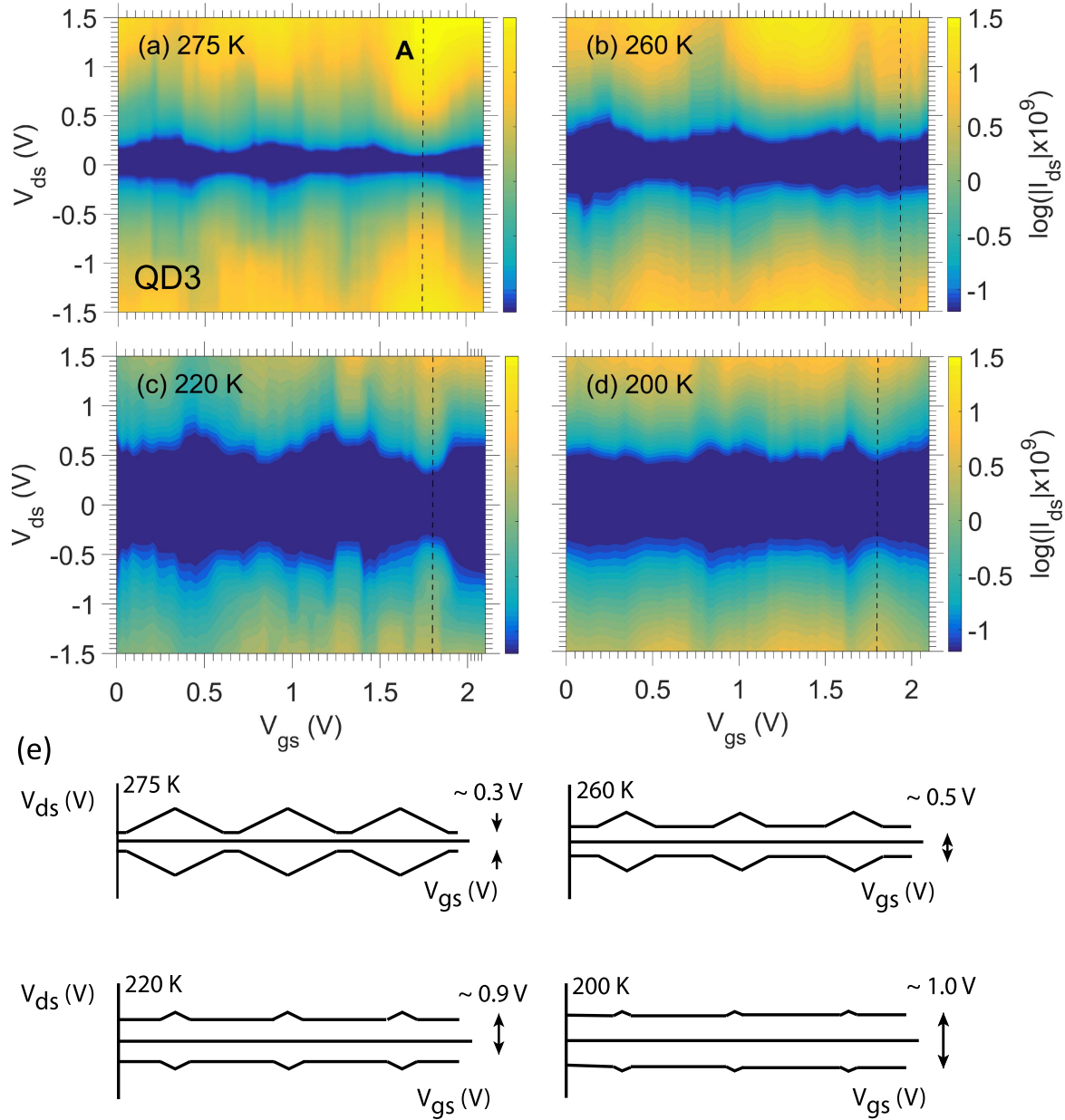
Figure 5. Temperature dependence of the electrical characteristics of QD3. The evolution with temperature of the Coulomb diamonds is shown in the colour plots of $\log|I_{ds}|$, as a function of V_{ds} and V_{gs}, at temperatures of (a) 275 K, (b) 260 K, (c) 220 K, and (d) 200 K. In addition the increasing influence of the potential barrier with decreasing temperature is shown. As a guide, (e) shows a diagrammatic representation of this effect, with the central low current region increasing in width along V_{ds} from ∼0.3 V at 275 K to ∼1.0 V at 200 K.

charging energy, supporting the model for these devices, shown in figures 4(f) and (g). In figure 6(b), for $V_{ds} = 1$ V, a current oscillation peak is still observed even for 150 K. However, this peak is broader than expected, implying a change in the parameter B associated with the bias drop across the device capacitances [19], providing further support to our observation of a change in the electrical parameters of the QD and its environment by 150 K, also seen in figure 4(c).

Data from QD1 is analysed in figure 7. Figure 7(a) shows the g_{ds} versus V_{ds}, V_{gs} plot of figure 2(d), but now overlaid with two Coulomb diamonds marked by white lines. Here, a linear plot of g_{ds} is used as the edges of the Coulomb diamonds are clearer in this, with the white lines approximately following the 2.5 pS contour. A large number of resonant

peaks create lines across the plot (e.g. indicated by dotted red lines), forming two groups lying parallel to both the left and right diamond edges. A schematic Coulomb diamond with N electrons on the QD, including resonant tunnelling through excited states, is shown in figure 7(b). The insets to the figure show the energy diagram for the QD at various points with respect to the Coulomb diamond. $E_c = e^2/C$ is the Coulomb gap in the QD, where C is the total QD capacitance. $E_a = E_{c1} + E_k$ is the QD single electron addition energy, where $E_{c1} = E_c/2 = e^2/2C$ is the energy needed to add an electron from the source to the QD, ignoring quantum confinement, and E_k the quantum confinement energy. E_a defines the ground state for the QD. E_N and E_{N+1} correspond to N and $N + 1$ electrons on the QD respectively. Excited states above
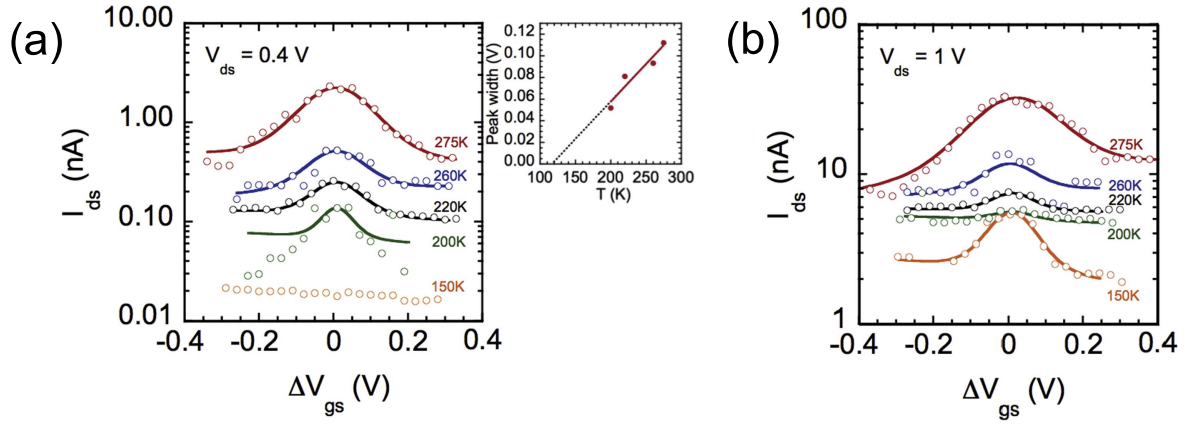
Figure 6. Temperature dependence of a current peak from 275 to 150 K. Data extracted for the peak lying along the dotted lines in figure 5. The current peak is plotted for $\Delta V_{gs} = V_{peak} - V_{gs}$, where V_{peak} is the peak centre, (a) for $V_{ds} = 0.4$ V, near the edge of the central threshold region, and (b) for $V_{ds} = 1$ V, well outside the threshold region. Data shows thermal broadening in V_{gs}, which is fitted with a $\cosh^{-2}(|\Delta V_{gs}|/Bk_BT)$ dependency [18], plus a linear function. Here, B is a constant. For (a), the peak width of this (Bk_BT) is plotted as a function of temperature in the insert, demonstrating the anticipated linear temperature dependence of the function.

and below this are shown by blue dotted and red solid lines respectively. Electron tunnelling occurs when QD states E_N, E_{N+1}, or these in combination with the excited states, lie within an energy window $E_{FS} - E_{FD} = eV_{ds}$, where E_{FS}, E_{FD} are the source, drain Fermi energies (detailed discussion in online supplementary material).

Comparison of the data (figure 7(a)) with figure 7(b) allows attribution of the g_{ds} lines to RT resonant tunnelling through excited states, and extraction of $E_a = 0.83$ eV $\sim 30k_BT$ at 290 K, a very large value (see online supplementary material). Here, lines with negative slope, e.g. α, β, *1*, correspond to excited states above the Coulomb gap (blue line, (b)) and lines with positive slope, e.g. δ, γ, η, χ, to lines below the Coulomb gap (red line, (b)). The Coulomb diamond allows measurement of E_a and the energy of the first excited state above the Coulomb gap, E_1. Furthermore, assuming a spherical QD of radius r, appropriate for our oxidised point-contact structures, it is possible to calculate E_{c1} and E_k. For Coulomb diamond B, we find $E_a = 0.83$ eV $\sim 30k_BT$ at 290 K, $E_1 = 1.3$ eV and $r = 0.8$ nm. Here, the separation of the first excited state from the ground state $\Delta E = E_1 - E_a = 0.5$ eV. E_a appears to be the largest, and r the smallest value yet reported for a QD transistor. E_a, E_{c1}, E_k and E_1 (figure 7(c)) can be extracted for the Coulomb diamonds centred at $V_{gs} = 2.3$ V, 4 V (diamond B), and 6 V (diamond A) in figure 7(a), with the corresponding QD radius in figure 7(d). As V_{gs} is reduced, r decreases from a maximum of 0.95–0.79 nm, implying that the QD can be electrically 'squeezed' [19, 21] to reduce its radius.

The nature of the few nanometre scale QDs in our devices is now considered. The central point-contact region in our device is oxidised to close to, or just at pinch-off. Here, if a crystallite Si core still remains due to incomplete pinch off by SiO_2, then given the small size of the core, it is probable that this will behave as an ultra-small QD embedded within the SiO_2. Alternatively, as the device starting material was heavily doped Si, a single or just a few donor atoms may

remain embedded within the SiO_2 region. Current transport then occurs either by direct tunnelling into a single donor atom QD, or along a path made by a few donor atoms forming an MTJ. In the later case, one of the donor atoms along the MTJ may dominate the characteristics, if this is isolated by a greater separation from its neighbours associated with donor concentration variability.

The data from 19 working RT SETs, fabricated in SOI material with 20 and 12 nm thick top Si layers is shown in figure 8. These devices were obtained from a total of 326 fabricated devices, in 4 processing runs (2 runs for each of the two SOI thicknesses). The 19 devices correspond to an overall percentage of 5.8% of the fabricated total. Here, criteria for a 'working' device were the RT observation of gate oscillations in I_{ds}, and/or the observation of a Coulomb staircase. The device I_{ds}–V_{ds}, V_{gs} characteristics were qualitatively similar to those in figures 2–4. The percentage of working devices versus the pre-oxidation point-contact cross-sectional area, from 120 nm^2 (10 nm × 12 nm) to 2000 nm^2 (20 nm × 100 nm) is shown in figure 8(a). Devices were oxidised to give a nominal SiO_2 thickness of ~5 nm (12 nm SOI) and ~10 nm (20 nm SOI). The number of fabricated devices for a given cross-section is shown in brackets at each data point. For devices larger than 400 nm^2, the point-contact width was larger than the height even in the 20 nm SOI material, implying that here, the critical minimum dimension was the SOI top Si thickness. It is seen in figure 8(a) that as the point-contact cross-sectional area increases, the percentage of working devices falls (a polynomial line is added to the plot as a guide to the eye). The highest percentage of 10.7% was observed for 200 nm^2 pre-oxidation area. There were no working devices by the 2000 nm^2 data point, and it was necessary to have an area ~700 nm^2 or less to find more than one working device. The trend seen in figure 8(a) emphasises the need to reduce the point-contact pre-oxidation cross-section to obtain an increased likelihood of working devices.

The QD radius r and addition energy $E_a = E_{c1} + E_k$ versus pre-oxidation cross-section, extracted using the model
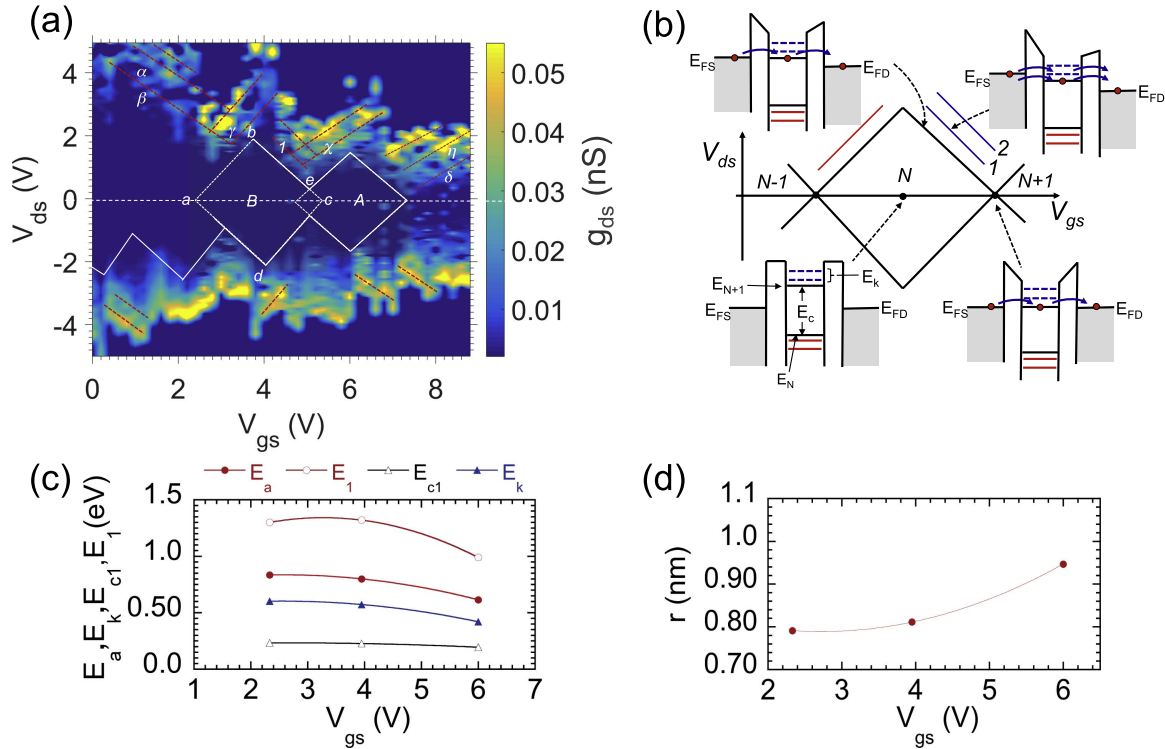
Figure 7. Analysis of the characteristics of QD1. (a) Figure 2(d) is repeated, but now the edges of the Coulomb diamonds marked by solid white lines, parallel to the g_{ds} contours. Extension of these lines (dotted orange lines) defines the Coulomb diamonds *A* and *B*, with the overlap between the diamonds at $V_{gs} = 5$ V caused by the additional potential barrier. A large number of lines in g_{ds} are observed (e.g. indicated by the dotted red lines). (b) A schematic Coulomb diamond with *N* electrons on the QD, including resonant tunnelling through excited states in the QD. Insets associated with the diamond show the energy diagram for the QD at various points with respect to the Coulomb diamond. (c) The values of E_a, E_k, $E_{c1} = E_c/2$ and E_1 extracted from the diamond and their dependence on V_{gs}. (d) The values of the QD radius, *r*, derived from these values.

of figure 7, are shown in figures 8(b) and (c) respectively. Here, data from 12 devices are shown, where the gate oscillations in I_{ds} were sufficiently clear to apply the model. It is seen that *r* lies in a relatively narrow band, $0.8 \, \text{nm} < r < 2.35 \, \text{nm}$, particularly given the single nanometre scales involved. Here, the mean and standard deviation are 1.47 nm and 0.53 nm respectively. The maximum variation in *r* corresponds to a length along only 7–11 atoms in crystalline Si, depending on the crystallographic direction. The narrow range of *r* tends to support the origin of the QD due to potential wells created by isolated donor atoms embedded within SiO_2, which would tend to be similar for different devices. Both the 12 nm and 20 nm SOI devices have similar average *r*, 1.49 nm and 1.42 nm respectively, though there is greater variation in the 20 nm SOI devices (the standard deviation in the 12 nm and 20 nm SOI is 0.46 nm and 0.67 nm respectively). The average radius across all devices is 1.47 nm. Furthermore, for both SOI thicknesses, *r* tends to reduce slightly with pre-oxidation cross-section (a linear fit is added as a guide to the eye). E_a (figure 8(c)) correspondingly increases as *r* reduces (a linear fit is added as a guide to the eye), as expected in the model.

The trends shown in figures 8(a)–(c) imply that while a reduction in point-contact size leads to increasing likelihood of working RT SETs (figure 8(a)), this does not lead to a smaller QD size (figure 8(b)). Instead, there is an unexpected

trend towards slightly larger QD radius for smaller point-contacts. Furthermore, for both 12 and 20 nm SOI, the average extracted QD radius is similar. These trends may be understood by plotting the threshold voltage V_{th} for drain–source current in the RT SETs, as a function of the cross-section area, where V_{th} corresponds to the minimum V_{ds} value at the edge of the central low current band (schematic diagram in figure 5(e)). It is seen that V_{th} increases rapidly with cross-sectional area (an exponential fit is added as a guide to the eye). As V_{th} is related to the height of additional underlying (figures 4(f) and (g)) or series potential barriers in the devices, this implies that in RT SETs obtained with a larger pre-oxidation cross-sectional area, any additional barriers are more significant. As these barriers are likely to be created by the oxidation process, RT SET characteristics observed with a larger pre-oxidation cross-section occur only if there is greater oxidation occuring in a particular device due to process variations. Furthermore, higher V_{ds} values are necessary to pull a higher and/or longer potential barrier down (see schematic in figure 4(g)). If a large QD with a smaller Coulomb gap exists, then the effect of this may be overcome as the voltage approaches V_{th}, due to the gap being pulled down well below the source Fermi energy (figure 4(g)). This behaviour would then lead to the 'self-selection' of smaller QD sizes when a working RT SET is observed at larger pre-oxidation cross-
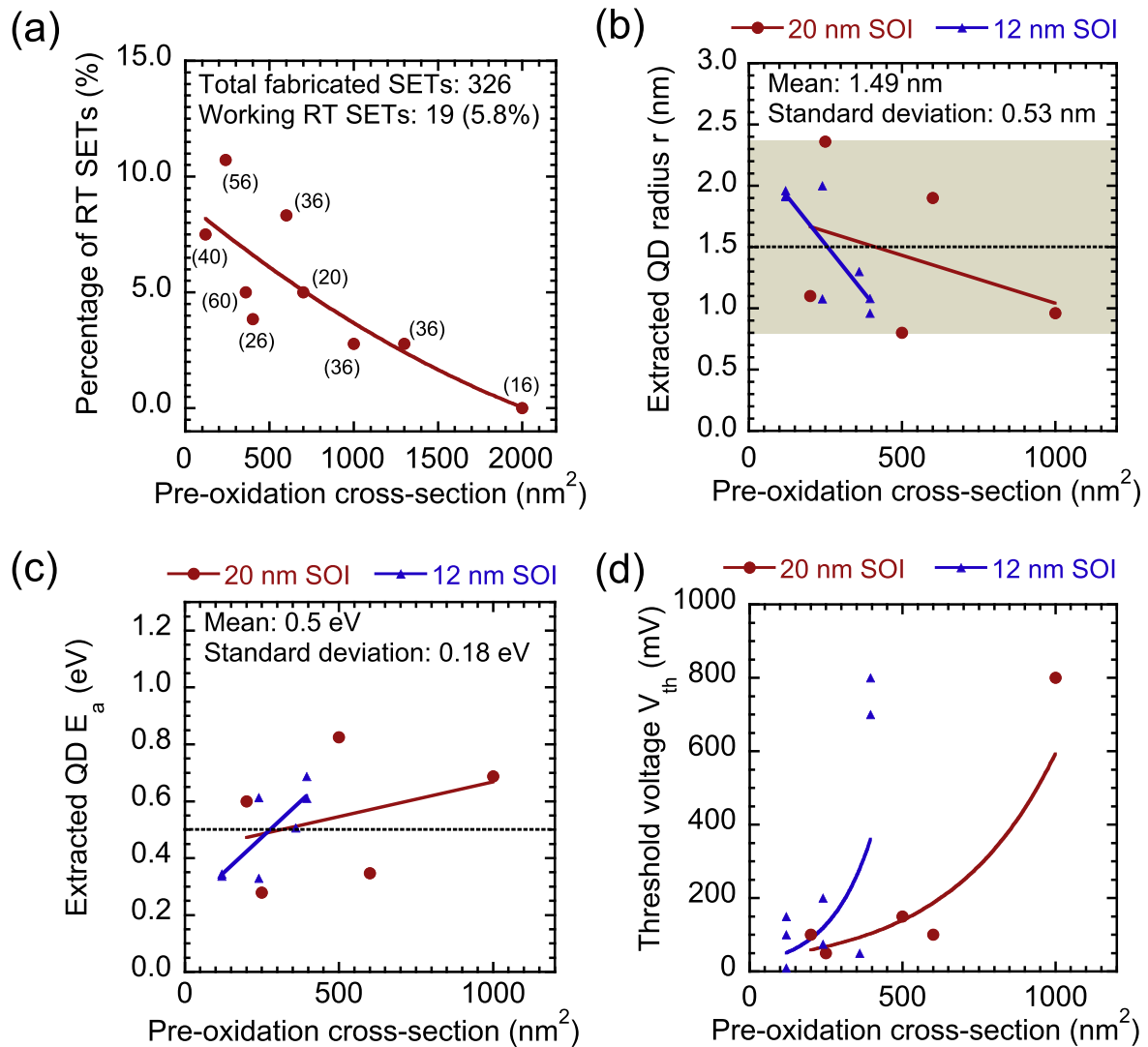
Figure 8. Analysis of working RT SET devices. (a) Percentage of working RT SETs versus pre-oxidation point-contact cross-sectional area. Nineteen working devices were measured from 326 fabricated devices, in SOI material with 20 and 12 nm thick top Si layers. Number of fabricated devices for a given cross-section is shown in brackets at each data point. (b) QD radius *r* versus pre-oxidation cross-sectional area, extracted using the model of figure 7. (c) Addition energy E_a versus pre-oxidation cross-sectional area for the RT SETs of (b), extracted using the model of figure 7. (d) Threshold voltage V_{th} in the RT SETs of (b), versus pre-oxidation cross-sectional area.

sectional area (figure 8(b)). However, the likelihood of finding such a device would be small (figure 8(a)).

In summary, we report RT operation of Si point-contact SETs, where an ultra-small, single nanometre scale QD (diameter ~1.6 nm) forms the device core. A remarkably large QD electron addition energy ~0.8 eV, and quantum confinement energy ~0.3 eV, are observed. These very large values (the highest values reported to date) enable RT observation not only of Coulomb blockade, but also of resonant tunnelling through excited states. In measurements of 19 RT SETs, the likelihood of finding one of these devices is seen to increase with reduction in point-contact size to the ~10 nm scale, and the extracted QD radius is found to lie within a narrow band, from 0.8 to 2.35 nm. At these sizes, in addition to the single-electron charging energy, the effect of quantum confinement and resonant tunnelling effects on the electrical characteristics cannot be ignored. Finally, the QD radius tends not to reduce as the point-contact dimensions are

reduced, supporting a picture where the QD is associated with the material properties such as donor atoms, rather than directly with the point-contact size. The results demonstrate that with careful control 'beyond CMOS' QD point-contact transistors, showing Coulomb blockade and resonant tunnelling through excited states, all at RT, can be produced using current 'conventional' semiconductor device fabrication techniques.

Acknowledgments

References

[1] Lee S, Lee Y, Song E B and Hiramoto T 2014 Observation of single electron transport via multiple quantum states of a silicon quantum dot at room temperature *Nano Lett.* **14** 71–7

[2] Nikonov D E and Young I A 2013 Overview of beyond-CMOS devices and a uniform methodology for their benchmarking *Proc. IEEE* **101** 2498–533

[3] Veldhorst M *et al* 2015 A two-qubit logic gate in silicon *Nature* **526** 410–4

[4] Zhang C-Y, Yeh H-C, Marcos M T and Wang T-H 2005 Single-quantum-dot-based DNA nanosensor *Nat. Mater.* **4** 826–31

[5] Urban J J 2015 Prospects for thermoelectricity in quantum dot hybrid arrays *Nat. Nanotechnol.* **10** 997–1001

[6] Pierre M, Wacquez R, Sanquer M, Vinet M and Cueto O 2009 Single-donor ionization energies in nanoscale CMOS channel *Nat. Nanotechnol.* **5** 133–7

[7] Shin S J, Lee J J, Kang H J, Choi J B, Yang S-R E, Takahashi Y and Hasko D G 2011 Room-temperature charge stability modulated by quantum effects in a nanoscale silicon island *Nano Lett.* **11** 1591–7

[8] Kitade T, Ohkura K and Nakajima A 2005 Room-temperature operation of an exclusive-OR circuit using a highly doped Si single-electron transistor *Appl. Phys. Lett.* **86** 123118

[9] Wang C, Jones M E and Durrani Z A K 2015 Single-electron and quantum confinement limits in length-scaled silicon nanowires *Nanotechnology* **26** 305203

[10] Lavieville R, Triozon F, Barraud S, Corna A, Jehl X, Sanquer M, Li J, Abisset A, Duchemin I and Niquet Y-M 2015 Quantum dot made in metal oxide silicon-nanowire field effect transistor working at room temperature *Nano Lett.* **15** 2958–64

[11] Takahashi Y, Nagase M, Namatsu H, Kurihara K, Iwdate K, Nakajima Y, Horiguchi S, Murase K and Tabe M 1994 Conductance oscillations of a Si single electron transistor at room temperature *IEDM'94* pp 938–40

[12] Ishikuro H, Fujii T, Saraya T, Hashiguchi G, Hiramoto T and Ikoma T 1996 Coulomb blockade oscillations at room temperature in a Si quantum wire metal-oxide-semiconductor field-effect transistor fabricated by anisotropic etching on a silicon-on-insulator substrate *Appl. Phys. Lett.* **68** 3585

[13] Saitoh M and Hiramoto T 2004 Extension of Coulomb blockade region by quantum confinement in the ultrasmall silicon dot in a single-hole transistor at room temperature *Appl. Phys. Lett.* **84** 3172

[14] Tan Y T, Kamiya T, Durrani Z A K and Ahmed H 2003 Room temperature nanocrystalline silicon single-electron transistors *J. Appl. Phys.* **94** 633

[15] Rafiq M A, Durrani Z A K, Mizuta H, Colli A, Servati P, Ferrari A C, Milne W I and Oda S 2008 Room temperature single electron charging in single silicon nanochains *J. Appl. Phys.* **103** 053705

[16] Rafiq M A, Masubuchi K, Durrani Z A K, Colli A, Mizuta H, Milne W I and Oda S 2012 Conduction bottleneck in silicon nanochain single electron transistors operating at room temperature *Japan. J. Appl. Phys.* **51** 025202

[17] Uchida K, Koga J, Ohba R and Toriumi A 2003 Programmable single-electron transistor logic for future low-power intelligent LSI : proposal and room-temperature operation *IEEE Trans. Electron Devices* **ED-50** 1623–30

[18] Origuchi S H, Agase M N, Hiraishi K S and Ageshima H K 2001 Mechanism of potential profile formation in silicon single-electron transistors fabricated using pattern-dependent oxidation *Japan. J. Appl. Phys.* **40** L29–32

[19] Kouwenhoven L E P, Marcus C M, Mceuen P L, Tarucha S and Robert M 1997 Electron transport in quantum dots *Mesoscopic Electron Transport* (Dordrecht: Kluwer) pp 105–214

[20] Likharev K 1999 Single-electron devices and their applications *Proc. IEEE* **87** 606–32

[21] Durrani Z 2009 *Single-Electron Devices and Circuits in Silicon* (London: Imperial College Press) pp 22–71

[22] Escott C C, Zwanenburg F A and Morello A 2010 Resonant tunnelling features in quantum dots *Nanotechnology* **21** 274018

[23] Jalil M B A, Wagner M and Ahmed H 1998 Analysis of multiple-tunnel junctions and their application to bidirectional electron pumps *J. Appl. Phys.* **84** 4617–24