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A novel 3D embedded gate field effect transistor – Screen-grid FET – Device concept and modelling

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Abstract

A novel 3D field effect transistor on SOI – screen-grid FET (SGrFET) – is proposed and an analysis of its DC behaviour is presented by means of 2D TCAD analysis. The novel feature of the SGrFET is the design of 3D insulated gate cylinders embedded in the SOI body. This novel gate topology improves efficiency and allows great flexibility in device and gate geometry to optimize DC performance. The floating body effect is avoided and the double gating row configuration controls short channel effects. The traditional intimate relationship between gate length and source-drain distance is removed, resulting in easy control of drain induced barrier lowering, improved output conductance and ideal sub-threshold slope. The separation between the gate fingers in each row is the key factor to optimize the performance, whilst downscaling of the source-drain distance and oxide thickness is not essential from an operational point of view.

The device exhibits a huge potential in low power electronics as given by an efficiency of transconductance "g_m/I_d" of 39 S/A at $V_{DS} = 100$ mV over a large gate voltage range and at a source-drain distance of 825 nm. We present the modelling results of the influence of gate cylinder distribution in the channel, channel doping, gate oxide thickness, gate finger distance and source-drain distance on the characteristics of the device.
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Keywords: Field effect transistor; SOI; TCAD

1. Introduction

One of the objectives in semiconductor industry is higher operation speed, lower power consumption and increased functional density. To that aim, in field effect transistor (FET) technology, gate lengths, oxide and SOI body thickness are aggressively scaled to deep sub-micron dimensions leading to increased leakage currents and poor output conductance. This then necessitates complex fabrication processes to counteract the short channel effects. In order to solve the different problems occurring with downscaling, novel device concepts are being investigated, examples are strained-Si, multi-gate and vertical FETs. The International Roadmap for Semiconductor Technologies [1] shows that the semiconductor industry is prepared to introduce non-classical approaches to Si MOSFETs, as illustrated by the introduction of high-k dielectrics, metal gates, etc. This is also reflected in current FET research that deviates from the traditional planar geometries in order to increase the influence of the gate compared to that of the drain in low dimensional structures. Examples are the cylinder gated FET [2] and the finFET [3]. These novel approaches are based on progress in nano-technology, introducing 2D/3D multiple gate configurations which require in general difficult or labour intensive processing and tend to change the traditional CMOS fabrication technology.

Another example of a vertical transistor proposed and realised in the past is the permeable base transistor (PBT)

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[4]. It makes use of a single grid embedded metallic gate. Notwithstanding its excellent theoretical operation characteristics, the technological difficulties associated to the embedded gate formation has hindered its use in practice.

The proposed 3D embedded-gate screen-grid FET (SGrFET) in this paper is a horizontal transistor with a multiple grid embedded gate, with drastically reduced processing complexity compatible with current SOI technology and with a gate function more similar to the tetrode in vacuum tube technology than the PBT. An additional advantage of the SGrFET is its MESFET-like transport which avoids the need for a channel near the SiO_2/Si interface. As a consequence limited surface roughness scattering can be expected. This together with an undoped body promises high mobility values.

Due to its MESFET character the initial prospective SGrFET application domain lies in low power analogue applications. The double gate row configuration also increases single device functionality for mixing and logic applications. Moreover the hole character of the gate can be exploited in ISFET technology.

The manuscript is organized as follows: in Section 2 the geometry and operation principles of the SGrFET are discussed. In Section 3 we present a discussion of the influence of the gate topology on the characteristics, followed in Section 4 by TCAD modelling of the DC performance when changing different geometrical parameters, emphasizing the threshold voltage control, sub-threshold slope, transconductance and output conductance. In Section 5 we briefly look into downscaling. Conclusions can be found in Section 6.

2. Geometry and functioning

A schematic drawing of a proposed SGrFET is given in Fig. 1. Although the SGrFET in Fig. 1 has two rows consisting each of three gate cylinders, this distribution is by no means exclusive. The SGrFET is proposed to be fabricated in Silicon-on-insulator (SOI) but can be equally fabricated in the more advanced strained-Si on insulator (sSOI) technology [5] to benefit from the improved characteristics of the strained-Si channel. The SOI body can be nominally undoped to favour elevated values of the carrier mobility. MOS gating is done via vertical gate cylinders into the SOI body perpendicular to the current flow and distributed between the source and drain. The critical character of the thickness of the Si body is relaxed as compared to the conventional PD or FD SOI technologies as the 3D gate fingers reach through the channel down to the buried oxide and thus avoid floating body effects [6]. Moreover, increasing the thickness of the Si body will improve the average mobility in the channel and increase the output current without increasing the surface area. The active area of the FET should be covered by a relatively thick deposited insulator, e.g. SiO_2 or Si_3N_4. This ensures that the parasitic surface capacitance is negligible and the gating is solely determined by the cylinders inside the channel. The

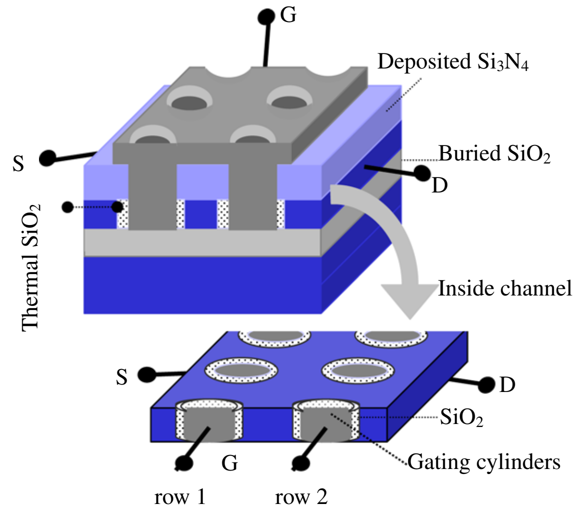

Fig. 1. Schematic configuration of a SGrFET with two gating rows, each consisting 3 gate cylinders. Top: 3D side view, bottom: channel region only. *S*, *D* indicate the start of the region of the source and drain, respectively, G the gate.

gating holes can be defined by e-beam or nano-imprint lithography with dimensions 10–200 nm into a mesa delineated by optical lithography. The cylindrical holes for the gates can be made via RIE with a controlled selective etch stop on the buried oxide of the SOI [7]. Control of the quality of the sidewalls is important but not essential as no channel is created near these gate regions. Thermal oxidation defines the gate oxides ($\leqslant$10 nm), sacrificial oxidation can be used to a certain extent to remove the sidewalls that are damaged by the ion bombardment in the RIE step. Problems encountered with the gate oxide quality as a result of the RIE step are the same as those encountered in finFET technology [8]. When downscaling, filling of the gating holes will require careful gate deposition techniques for high aspect ratio geometries, as is currently being pursued in other research fields (see e.g. [9]).

Ohmic contacts can be further defined as in standard MOSFET processing. Apart from the peculiar gating configuration of the SGrFET, the other parameter that is radically different from conventional MOSFETs is the doping in the channel. In order to create a unipolar device the doping type in the channel must be the same as in the ohmic contacts in contrast to traditional MOSFETs.

In this work a metal gate will be used, a choice consistent with the prediction in the IRST for future FET technologies. The gate metal will be inside the holes and form 3D cylinders within the channel region, standing perpendicular to the current flow. The gating action is schematically illustrated in Fig. 2 in 2D, the rectangle represents the Si channel, the dotted regions the gate metal, the grey areas the gate oxide and the shaded region the depletion region. The source and drain regions (not drawn) are heavily doped. In Fig. 2 top, for a given value of V_{GS} the semiconductor between the two gate cylinders is un-depleted and a drain current may flow as a channel exists [10].

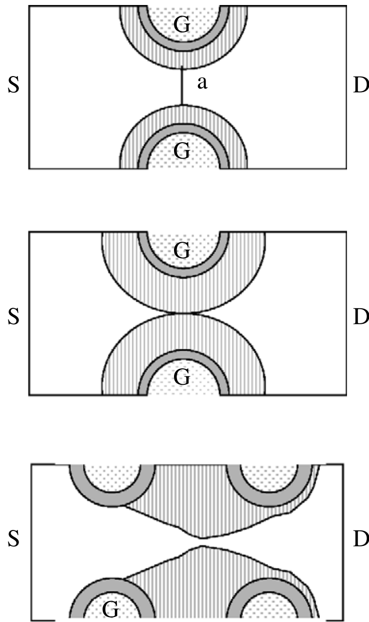

Fig. 2. Illustration of gating action between gate cylinders. Top: when $V_{GS} = 0$ V, middle: when $V_{GS} \approx V_{th}$. Bottom: result of TCAD for $V_{DS} = 0.05$ V and $V_{GS} = -0.85$ V illustrating the interaction between the gating rows.

Increasing the depletion widths by the gate potential pinches off the channel – $a = 0$ nm – and switches the channel off (Fig. 2 middle). Changing the metal of the gate both enhancement and depletion mode can be made. Introducing a second gating row, as proposed in Fig. 1, will cause an interaction between the depletion regions that are generated by the same gate potential applied to both rows as illustrated in Fig. 2 bottom [11]. Due to the interaction between the two gate rows, the pinch-off of the channel happens in between all gate fingers nearer the drain than the source. This phenomenon points towards an electrostatic shielding of the source by the gate fingers near the drain contact, as will be discussed in more detail later.

Introducing the 2-row SGrFET gate topology (Figs. 1 and 2) implies that the control of the gate and the source-to-drain (S-D) distance are decoupled. In a classical MOSFET both are related because when the S-D distance is reduced the gate length has to shorten. This scaling leads to a poorer control of the channel by the gate (the channel conductance g_d increases) and whilst increasing f_T the low-frequency voltage-gain unfortunately decreases. Unless one changes the topology of the gate, one cannot change the low-frequency gain-bandwidth product. The SGrFET can vary this product due to the novel gate topology. The influence of the gate topology on the transfer characteristics is illustrated in Fig. 3a, where five different distributions of gate fingers are considered (see Fig. 3b). As stated above, the conduction through the channel of the SGrFET does not rely on the formation of an inversion layer around the gate electrodes, therefore the carrier roughness scattering at the SiO_2/Si interface will not limit for the mobility of this device. In this sense, the transport in the SGrFET is as in a MESFET. Obviously a Monte Carlo (MC) analysis is needed in order to confirm the reduction of the impact of roughness scattering on the carrier mobility in the SGrFET. But this analysis is beyond the scope of this paper.

In this paper we present the first results of the study of the electrical DC characteristics of the SGrFET. To this aim the most suitable tool is a 2D drift-diffusion model as is made available by the commercial 2D device simulator, MEDICI™ [12]. Medici is a versatile tool for the design and development of semiconductor devices. Since the drift-diffusion model is not valid for deep-submicron devices, sufficiently large geometries are initially used to study the behaviour of the SGrFET. For the short structures presented in Section 5, we used the coupled electron hydrodynamic model together with Lombardi's surface scattering model [12]. Simulations are done on the cross-sectional plane from S to D parallel to the semiconductor surface. We assume that the channel thickness, doping and electrostatic effects in the vertical dimension (from top surface to

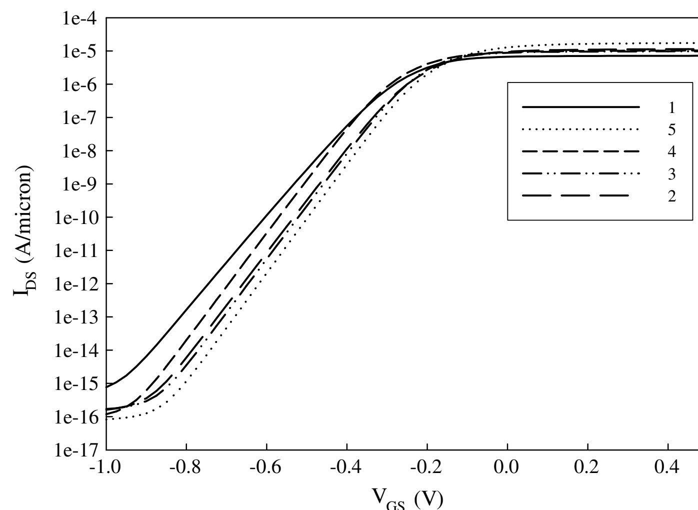

Fig. 3a. Transfer characteristics of different gating configurations. Labelling corresponds with gate geometry label given in Fig. 3b.

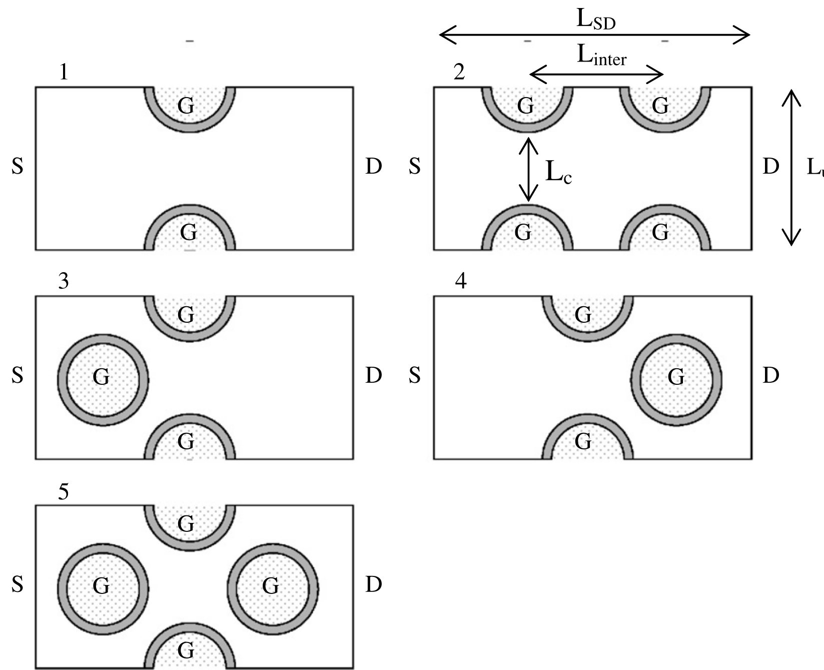

Fig. 3b. Schematic lay-out of five unit cells of different gate cylinder configurations. Important geometrical parameters are defined on geometry no. 2.

BOX) are uniform (this is reasonable if the thickness of the Si body is tens of nanometres), the validity of this approach for "large" geometries has been proven by 3D TCAD simulations. For normalization we assume the Si channel thickness to be 1 μm. The mesh needs to be carefully defined in the regions around the gate cylinders to avoid artificially introduced leakage. In order to increase the simulation speed, each gating configuration can be represented by a unit cell of a certain width with half circles at the edges and full circles within the channel region (as shown in Fig. 3b). Simulations confirm that independent of bias, the magnitude of the current of a parallel connection of N unit cells is I_{DS} (N unit cells) $= N \times I_{DS}$ (1 unit cell).

Referring to Fig. 3b, the distance between the centres of two gate cylinders in each row is called inter-electrode length (L_{inter}), the distance between centres of the gate cylinders in the same row is called the unit cell width (L_u), whereas the distance between the outer gate oxide layers in the same row is the channel width (L_c). The gate length can be seen as $L_g = L_ø + \eta \times L_{inter}$ with $0 < \eta < 1$. $L_ø$ is the gate cylinder diameter.

All SGrFETs in Fig. 3 have a source-drain distance of $L_{SD} = 825$ nm, channel doping $N_D = 10^{15}$ cm^{-3}, gate diameter $L_o = 120$ nm, oxide thickness $t_{ox} = 2$ nm, unit width $L_u = 294$ nm, inter-electrode distance $L_{inter} = 240$ nm and channel width (where appropriate) $L_c = 170$ nm. These geometrical values are chosen to be consistent with current industrial CMOS processing capabilities. The S-D distance is larger in order to allow the use of the drift-diffusion model as discussed before. Reduced S-D distances are discussed in Section 5.

The main interest of Fig. 3 is to illustrate that under the same geometrical conditions, the gate distribution influences the SGrFET characteristics, such as sub-threshold slope, on and off current, etc. Fig. 3a shows that the 2-row configurations (confs. 2,3,4,5) outperforms the single row conf. 1 and that the staggered-gate confs. (3,4,5) outperform conf. 2. Conf. 5, although with the best performance due to the reduced channel width in the diagonal inter-gate direction, requires more surface area, making it less suitable for downscaling.

Although confs. (3,4) show a better turn-off than (2), their high frequency characteristics might be influenced by the gate cylinders in the path of direct carrier flow from source to drain. Therefore a fair evaluation needs to be done using 3D TCAD AC simulations. At this initial stage the paper presents only 2D DC simulations and thus conf. 2 is used for evaluating the influence of the different parameters on the performance. Within this DC analysis it is acceptable to assume that similar dependencies can be expected for the other configurations. A report on still more gating conf. has been given in [13]. In Section 3 the 1-row and 2-row configuration are studied in more detail in order to understand the influence of the introduction of the 2nd gating row.

3. Control of drain-induced-barrier-lowering

For these simulations we take $N_D = 1 \cdot 10^{15}$ cm^{-3}, $t_{ox} = 2$ nm, $L_{SD} = 825$ nm, $L_ø = 120$ nm, $L_u = 280$ nm and $L_{inter} = 240$ nm (2-row). The gate metal is Aluminium (workfunction $\phi = 4.1$ eV). The gate configurations studied are given in Fig. 4. The main difference between the 1-row confs. is the gate position relative to the drain. The performance parameters are given in Table 1.

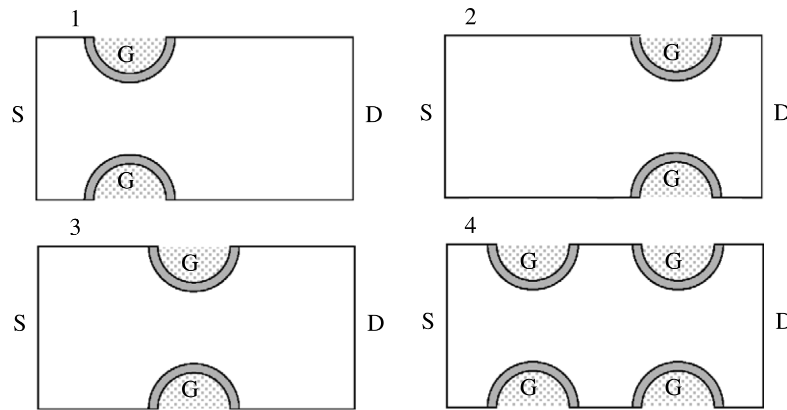

Fig. 4. Gate configurations for the comparison between the 1-row and 2-row gating effect.

Table 1
The influence of the position and number of gate row on the device characteristic parameters

Configuration no.	1	2	3	4
Position of rows	1-row near source	1-row near drain	1-row middle	2-rows
DIBL (mV/V)	60	101	80	42
S (mV/dec) @$V_{DS} = 0.1$ V	71	71	70	63
V_{th} (V) linear @$V_{DS} = 0.1$ V	−0.3	−0.3	−0.3	−0.25
g_{mmax} (μS/μm^2) @$V_{DS} = 0.1$ V	120	95	110	160
g_{dmin} (μS/μm^2) @ V_{GS}–$V_{th} = 0$ V and $V_{DS} = 2$ V	0.85	0.40	0.49	0.15

The position of the gate cylinders in the 1-row conf. relative to the drain has a direct impact on the current drive of the SGrFET. The single row conf. with gate near the source carries the highest current, reducing when shifting the gate towards the drain contact. This is a direct consequence of the efficiency of the gate in suppressing the parasitic control of the n^+–n barrier at the source-side. Obviously the efficiency of the screening of the drain potential depends on the relative position of the gate in the active region. Introducing a 2-row conf. restores the current drive to a certain extent and changes the current slope in both the triode and the pentode regions dramatically.

Table 1 summarizes the values for DIBL (drain induced barrier lowering), S (sub-threshold slope), g_{mmax} (maximum transconductance) in the triode region and g_{dmin} (minimum output conduction) for the different configurations. DIBL is calculated as follows:

$$\mathrm{DIBL} = \frac{V_{th}^{sat} - V_{th}^{lin}}{1.9}. \quad (1)$$

V_{th}^{sat} is the threshold voltage derived at $V_{DS} = 2$ V using linear extrapolation of the $\sqrt{I_{DS}^{sat}} - V_{GS}$ characteristic. V_{th}^{lin} is the threshold voltage derived at $V_{DS} = 0.1$ V using the tangential of the $I_{DS} - V_{GS}$ characteristic at V_{GS} for which g_m is maximum.

The values of conf. no. 4 indicate that the 2-row configuration has much improved gate control. This is because the second row is screening the action of the drain voltage on the potential barrier at the source and acts as a DIBL eliminator. According to the increased gate control in the 2-row conf. g_{mmax}, g_{dmin} and S are improved. Note the small impact of the single gate position on S which is in good agreement with the nature of the drain current in this regime. This 2-row gating conf. is similar to the screen grid vacuum tube (tetrode) [14] where this extra grid was introduced to electrostatically shield the anode from the control grid. The SGrFET shows similar behaviour and is therefore named "screen grid" as in tetrode technology. In this paper, we will only consider the situation when both the first and the second row are at the same bias, but as in the tetrode, the second row can be biased at a suitable constant voltage while the potential on the first row is varied. Moreover, the device can operate as a multi-gate device and a different signal can be applied to each gate-row to increase the device's functionality for analogue and logic applications.

In the following section we will study the effect of different geometrical parameters on the performance of the 2-row SGrFET.

It remains to note that increasing the channel doping N_D has a huge impact on the DC characteristics of the device. Increasing N_D makes V_{th} more negative and drastically increases S due to a weakened control of the gate cylinders on the carrier depletion. In order to optimize the SGrFET device performance, the channel doping should be kept at low as possible. This is beneficial as under these conditions the SGrFET can fully develop its potential for noise and transport (mobility).

4. Influence of geometrical parameters

The starting geometry of the SGrFET in the following simulations is: channel doping $N_D = 10^{15}\ \mathrm{cm}^{-3}$, $L_{SD} = 825$ nm, $t_{ox} = 2$ nm, $L_ø = 120$ nm, the position of the first row of gate cylinders measured from the source contact is at 525 nm and the second row is at 765 nm. This makes $L_{inter} = 240$ nm. Source and drain contacts are heavily

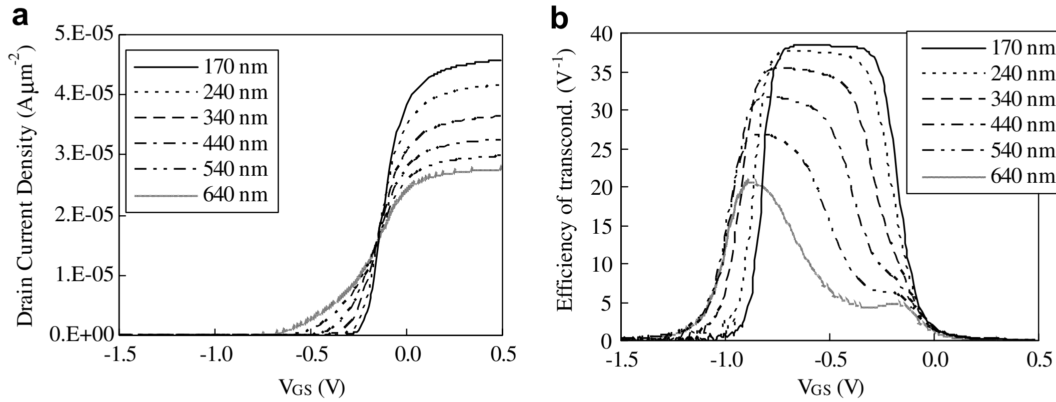

Fig. 5. Left transfer characteristics normalised to the unit width: $I_{DS}/(1\ \mu m \times L_u)$ for different values of L_u. Right: efficiency of transconductance g_m/I_{DS} as a function of gate bias for different values of L_u. Both at $V_{DS} = 100$ mV.

doped with a width of 250 nm, making the total length of the simulated devices equal to 1.325 μm.

We found that changing the inter-electrode distance between the two gating rows has a minor effect on the characteristics of the SGrFET. Nevertheless, performance improves when the second row is closer to the first. This feature allows a reduction in S-D distance by reducing L_{inter} without performance loss (see later).

The width of a unit cell, when all other geometrical parameters are kept constant, determines the distance between the gates in 1-row, L_c and thus is expected to have a major influence on the device characteristics. The influence of the unit cell width, L_u is studied by varying L_u from 170 nm to 640 nm. Table 2 summarizes the variation of some important device parameters.

Reducing L_u increases the threshold voltage towards 0 V, and reduces the sub-threshold slope to its theoretical minimum. This result is similar to Double Gated FETs (DGFETs) for reduced channel width [15]. By reducing the unit width, L_u by a factor of 2, the output conductance g_d decreases by one order of magnitude. A low output conductance is essential for large voltage gain at low frequencies: $A_v = g_m/g_d$. A minimum g_d for high gate overdrive is reached at $L_u = 190$ nm since at this electric field the device goes in accumulation. For small gate overdrive this happens at lower L_u. Decreasing L_u also decreases the drain current at the same rate. The total current drive however can be increased by increasing the number of unit cells N, thus increasing the mesa width similar to increasing the gate width in a conventional FET. This makes more efficient use of the area than fin-based multi-gate structures as discussed in Section 5. Moreover, the SGrFET topology provides an additional method to increase the drive current via an increase of the body thickness without degraded DIBL. This approach is limited by the non-zero surface capacitance for very thin body thickness and by fabrication issues that result from the large body thickness/gate-hole aspect ratio. This is unlike finFETs where an increasing fin height rapidly deteriorates the sub-threshold slope of the device [16]. Initial 3D Taurus^{TM} [12] simulation results show that S for the SGrFET for a 40 nm body is 61, whilst for a 200 nm body $S = 62$.

The source-drain current normalized by the product of the unit cell width L_u and the body thickness (1 μm) and the efficiency of transconductance: $\frac{g_m}{I_{DS}} = \frac{d\ln(I_{DS})}{dV_{GS}}$ are given in Fig. 5. g_m/I_{DS} is a quality factor of the device as it represents the amplification per dissipated power [17]. The results show an increased current density for decreasing unit widths together with improved transconductance efficiency. Increased g_m/I_{DS} ratios are found for the SGrFET in comparison with the FD SOI MOSFETs [17] at much smaller drain voltages. The maximum value of the efficiency of transconductance is close to the maximum theoretical value (35 V^{-1}) for $L_u = 170$ nm at $V_{DS} = 0.1$ V over a wide range of V_{GS}.

The influence of reducing the unit width L_u (and thus L_c) on the on/off currents can be gleaned from the transfer graphs in Fig. 5. As the threshold voltage (V_{th}) shifts as a function of L_u, the approach for determining I_{on} and I_{off} should take this shift into account. Based on the benchmarking arguments given by Chau et al. [18], I_{on} and I_{off} for the depletion mode SGrFETs can be derived from:

$$\begin{aligned} I_{on} &\rightarrow \text{at } V_{GS} = V_{CC} + 2V_{th} \quad \text{with } V_{CC} = V_{DS} \\ I_{off} &\rightarrow \text{at } V_{GS} = 2V_{th} \quad \text{with } V_{CC} = V_{DS} \end{aligned} \tag{2}$$

From Fig. 5 we see directly that decreasing L_u increases the I_{on}/I_{off} ratio.

The influence of the oxide thickness t_{ox} on the characteristics is investigated for $L_{SD} = 825$ nm, $t_{ox} = 2$ nm, $L_o =$ 120nm and $L_c = 170$ nm. Thus the unit cell width L_u has to increase accordingly: L_u changes from 294 to 310 nm for t_{ox} from 2 to 10 nm. A minimum of 2 nm gate oxide has been chosen to avoid tunnelling effects (see Table 2).

The results show the "traditional" t_{ox} effect: decreasing t_{ox} increases the gate control on the channel. The maximum transconductance, g_{mmax} at $V_{DS} = 100$ mV, is reached at the same gate voltage of $V_{GS} = -0.15$ V for all values of t_{ox} and not surprisingly g_{mmax} increases with decreasing t_{ox}. Unlike in traditional SOI/CMOS technologies, I_{on}/L_{off}

Table 2
The influence of the unit cell width L_u on the device characteristic parameters

L_u (nm)	170	190	240	290	340	390	440	490	540	590	640
S (mV/dec)	60	60	61.3	62.8	65.2	68.5	72.9	78.6	86.1	96.2	111.4
V_{th} (V)	−0.21	−0.22	−0.23	−0.25	−0.27	−0.28	−0.30	−0.31	−0.33	−0.35	−0.36
g_{dmin} (μS/μm^2) @ V_{GS}–V_{th} = 1 V	4.24	3.79	4.50	5.66	7.41	9.23	11.82	14.69	17.04	18.98	19.50
g_{dmin} (μS/μm^2) @ V_{GS}–V_{th} = 0 V	0.035	0.048	0.082	0.145	0.286	0.538	0.96	1.65	2.73	4.08	5.66
DIBL	27.5	29.5	34.2	41.6	53.5	71.1	94.3	121.1	149.1	178.7	208.6

Table 3
The influence of oxide thickness t_{ox} on the device characteristic parameters for constant channel width $L_c = 170$ nm at $V_{DS} = 0.1$ V

t_{ox} (nm)	2	4	6	8	10
S (mV/dec)	63	64	64	65	66
V_{th} (V)	−0.25	−0.25	−0.26	−0.27	−0.28
DIBL	44	46	47	50	51
g_{mmax} (μS/μm^2)	160	140	120	110	100
I_{on}/I_{off} (×10^7)	6.46	5.68	7.87	10.9	15.3

only decreases slowly when decreasing t_{ox}. This is a major property of the SGrFET: an aggressive scaling of the oxide thickness is not necessary in order to improve the electrical characteristics of the device. Notice that a reduction in t_{ox} by a factor of 5 only gives a 60% improvement in g_{mmax}, whilst imperceptibly changing both S and V_{th}. At the same time, I_{on}/I_{off} is only multiplied by a factor of 2.4, cf. Table 3. Basically the improvements are gained through the new gating topology. Conversely, the reduction of t_{ox} has little impact on the DIBL. One important consequence of Table 3 is that since large variations of the value of the oxide thickness have little impact on the main electrical parameters, this will ease its fabrication as some in-homogeneities in the oxide thickness can be tolerated.

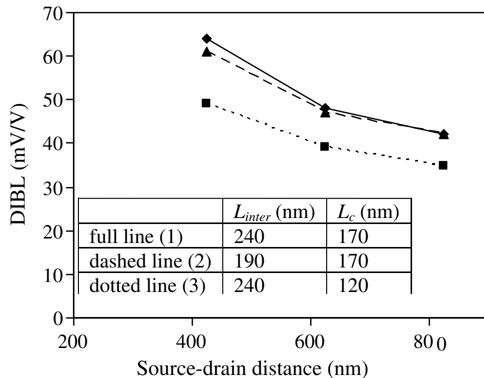

Fig. 6. Drain induced barrier lowering (DIBL) as a function of source-drain distance, demonstrating the influence of L_c and L_{inter} on the variation of DIBL.

5. Influence of reducing L_{SD}

In this section we evaluate the reduction of the source-drain distance, L_{SD} with scaling of L_{inter} and L_c. The value of the geometrical parameters of each SGrFET is given in the inset of Fig. 6. $L_o = 120$ nm and $t_{ox} = 2$ nm for all. In Fig. 6 the variation of DIBL as a function L_{SD} is given for each case.

A decrease of L_{SD} by a factor of ~2, without changing other parameters, gives an increase of DIBL by a factor 1.5, case (1). However L_c and L_{inter} can be used in order to control DIBL. Decreasing L_c reduces the DIBL increase factor to 1.4, case (3) whilst giving an overall DIBL decrease. Reducing L_{inter} hinders the DIBL increase. The interplay of these two geometrical parameters L_c and L_{inter} can therefore optimise DIBL whilst downscaling the source-drain distance.

Using this knowledge, TCAD is done on sub-100 nm L_{SD} SGrFETs and compared to a PD-SOI FET (···o···) and a DG FET (–◇–). The model used for the small devices

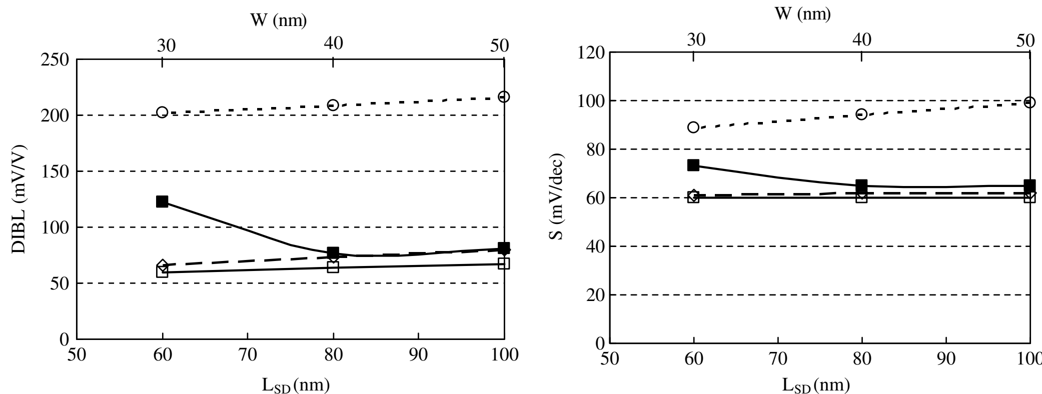

Fig. 7. The influence of a unit cell length LSD and width W on DIBL and S for the SGrFET (squares), the PD-SOI FET (circles) and the DGFET (diamonds).

is discussed in Section 1. In Fig. 7 DIBL and S are given as a function of L_{SD}(where appropriate $L_{SD} = L_g$ gate length). The corresponding unit cell width, W is given on the top horizontal axis. For the PD-SOI FET the Si body height is chosen equal to W. For the SGrFET we considered the two limiting cases: $L_u = W$ (–□–) and $L_c = W$ (–■–). The operation of the SGrFET shows results with excellent DIBL and S control when downscaling as compared to the other two technologies as long as L_u is kept close to W.

These results indicate an electrical robustness of the SGrFET to downscaling on one hand. Whilst on the other hand the multi-unit SGrFET is based on a widened mesa into which more gating holes are "drilled", preventing the loss of surface area for trenches as those needed for vertical multi-DGFET approaches [19,20]. Moreover, current drive can also be increased by increasing the mesa height within the technological limitations of etching and filling the gate holes, as previously discussed.

6. Conclusions

A novel 3D planar MOSFET structure on SOI – SGrFET – is proposed with an alternative double gating row configuration, where the second gating row efficiently screens the influence of the drain on the source-channel barrier (as in a tetrode) and adds extra functionality to the device (when each row is independently biased). The gate is an arrangement of cylinders, within an un-doped mesa, standing perpendicular to the channel current between source and drain and reach through to the buried oxide of the SOI. The SGrFET presented here is a unipolar device, functioning as a MESFET, but with an added interaction between the gating rows. We have shown that a gate topology with two rows of gate fingers allows to significantly improve the device's performance (S, DIBL, g_d, g_m/I_{DS}) due to the screening of the source-channel barrier by the drain-side row. The short channel effects associated with downscaling can be efficiently controlled by the modification of the distance between the gate fingers in both parallel and perpendicular current flow direction. Excellent electrical robustness has been demonstrated for downscaling to 60 nm.

In strong contrast with conventional bulk CMOS and SOI technologies a noticeable insensitivity of the main electrical parameters with respect to the gate oxide thickness in the range (2–10 nm) has been found.

The SGrFET bodes well for low power applications with higher g_m/I_{DS} compared to other technologies and an S robustness against an increase in body height.

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References

[1] http://public.itrs.net/Files/2003ITRS/Home2003.htm.
[2] De Meyer K, Caymax M, Collaert N, Loo R, Verheyen P. The vertical heterojunction MOSFET. Thin Solid Films 1998;336(1–2):299–305.
[3] Hisamoto D, Lee WC, Kedzierski J, Takeuchi H, Asano K, Kuo C, et al. FinFET – A self-aligned double-gate MOSFET scalable to 20 nm. IEEE Trans Electron Dev 2000;47(12):2320–5.
[4] Schuppen A, Vescan L, Marso M, Hart Avd, Luth H, Beneking H. Submicrometer silicon permeable base transistors with buried $CoSi_2$ gates. Electon Lett 1993;29(2):215–7.
[5] Langdo TA, Currie MT, Cheng ZY, Fiorenza JG, Erdtmann M, Braithwaite G. Strained Si on insulator technology: from materials to devices. Solid State Electron 2004;48(8):1357–67.
[6] Suryagandh Sushant S, Garg Mayank, Woo Jason CS. Device Design Methodology for Sub-100-nm SOC Applications Using Bulk and SOI MOSFETs. IEEE Trans Electron Dev 2004;51(7):1122–8.
[7] Saya D, Fukushima K, Toshiyoshi H, Fujita H, Hashiguchi G, Kawakatsu H. Fabrication of silicon-based filiform-necked nanometric oscillators. Jpn J Appl Phys 1 2000;39(6B):3793–8.
[8] Lindert N, Chang L, Choi Y-K, Anderson EH, Lee W-C, King T-J, et al. Sub-60-nm Quasi-Planar FinFETs Fabricated Using a Simplified Process. IEEE Electron Dev Lett 2001;22(10):487–9.
[9] McNie M, King D, Vizard C, Holmes A, Lee KW. High aspect ratio micromachining (HARM) technologies for microinertial devices. Microsystem Technol 2000;6(5):184–8.
[10] Zhao B, Biberger MA, Hoffman V, Wang SQ, Vasudev PK, Seidel TE. Low temperature and low cost planarised aluminium interconnect for sub-half micrometre VLSI circuits. Electron Lett 1997;33(3):247–8.
[11] Shur M. Physics of semiconductor devices. In: Holonyak N, editor. Solid State Physical Electronics. Prentice Hall; 1990.
[12] Ding PW, Fobelets K, Velazquez-Perez JE. "3D Modelling of the Novel nanoscale Screen-Grid FET", MRS Spring Meeting 2006, 16–21 April San Fransisco, USA.
[13] Medici and Taurus are products of Synopsis: http://www.synopsys.com/.
[14] Fobelets K, Ding PW, Velazquez-Perez JE. "A novel 3D embedded gate field effect transistor: Device concept and modelling". In: Proceedings of the 25th International Conference on Microelectronics, Serbia and Montenegro 14–17 May 2006.
[15] Tyne GFJ. In: Menkes D, Sivowitch E, editors. Saga of the Vacuum Tube. Indianapolis: H.W. Sams; 1977.
[16] Havaldar DS, Katti G, DasGupta N, DasGupta A. Subthreshold current model of finFETs based on analytical solution of 3-D Poisson's equation. IEEE Trans Electron Dev 2006;53(4):737–42.
[17] Pei G, Kedzierski J, Oldiges P, Ieong M, C-C Kan E. FinFET design considerations based on 3-D simulation and analytical modeling. IEEE Trans Electron Dev 2002;49(8):1411–9.
[18] Colinge JP. Fully – Depleted SOI CMOS for analog applications. IEEE Trans Electron Dev 1998;45(5):1010–6.
[19] Chau R, Datta S, Doczy M, Doyle B, Jin B, Kavalieros J, Majumdar A, Metz M, Radosavljevic M. Benchmarking nanotechnology for high-performance and low-power logic transistor applications. IEEE Trans Nanotechnol 2005;4(2):153–8.
[20] Choi Y, King T, Hu C. Spacer FinFET: nanoscale double-gate CMOS technology for the Terabit Era. Solid-State Electron 2002;46:1595–601.