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Pattern-generation and pattern-transfer for single-digit nano devices

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Single-electron devices operating at room temperature require sub-5 nm quantum dots having tunnel junctions of comparable dimensions. Further development in nanoelectronics depends on the capability to generate mesoscopic structures and interfacing these with complementary metal–oxide–semiconductor devices in a single system. The authors employ a combination of two novel methods of fabricating room temperature silicon single-electron transistors (SETs), Fowler–Nordheim scanning probe lithography (F-N SPL) with active cantilevers and cryogenic reactive ion etching followed by pattern-dependent oxidation. The F-N SPL employs a low energy electron exposure of 5–10 nm thick high-resolution molecular resist (Calixarene) resulting in single nanodigit lithographic performance [Rangelow *et al*., Proc. SPIE **7637**, 76370V (2010)]. The followed step of pattern transfer into silicon becomes very challenging because of the extremely low resist thickness, which limits the etching depth. The authors developed a computer simulation code to simulate the reactive ion etching at cryogenic temperatures (−120 °C). In this article, the authors present the alliance of all these technologies used for the manufacturing of SETs capable to operate at room temperatures. © *2016 American Vacuum Society*. [http://dx.doi.org/10.1116/1.4966556]

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I. INTRODUCTION

Manufacturing of single-digit electronic and optical devices requires the establishment of two fundamental technologies: lithography and pattern transfer. Here, we show that a novel future device concept benefits from a closed-loop optimization between pattern-generation and pattern-transfer—as opposed to serial optimization. Particularly, the demands of ever-shrinking feature sizes together with line edge roughness control, overlay pattern alignment (stitching), and high fidelity process control can be fulfilled.

A wide variety of single-electron transistors (SETs) have been demonstrated in crystalline silicon, using diverse techniques for defining nanoscale tunnel barriers and charging islands. These can be broadly subdivided into high resolution lithographic techniques or capitalizing on a disorder effect in a nanowire. Electron beam lithography (EBL) and RIE are most widely used fabrication processes. Usually followed by an oxidation step, they both reduce the island dimensions and passivate the silicon surface. This facilitates the placement of islands of specific size at defined locations. Silicon

SETs operating at room temperature (RT) have been fabricated using, e.g., nanocrystalline grains,[2] multiple islands,[3] a suspended nanowire,[4] or within a fin-FET structure.[5] Also, room temperature operation was shown using single holes within a MOSFET (Ref. 6) and in ultrathin silicon.[7] Today, high resolution lithographic techniques are typically linked with high capital investment in equipment. As a result, fast prototyping of novel devices is restricted. Here, we present a cost effective, fast prototyping lithography: scanning probe lithography (SPL).[8] SPL is based on Fowler–Nordheim (F-N) electron emission from a scanning proximal probe-tip.[9] This is combined with pattern transfer techniques, especially cryogenic etching enabling pattern transfer toward single digit-nano-features.[10] Patterning of SETs is carried out in a 5–20 nm thick calixarene molecular glass resist[8] by using SPL technology. We have demonstrated the application of a step-and-repeat SPL method, including optical as well as atomic force microscopy-based navigation and overlay-alignment.[8] A mix-and-match approach is used to enhance throughput capabilities.[1,15] The closed-loop lithography scheme is applied to sequentially write positive and negative tone features. Due to the integrated unique combination of read–write SPL-cycling, each lithographic feature is aligned using AFM-methods with the highest positioning accuracy. In addition, each feature is AFM-inspected with an atomic resolution by the same tip after the writing. Routinely, we can create a pattern in a step-by-step mode. Finally, we have demonstrated patterning over larger areas and practical applicability of the SPL process for lithography down to sub-5 nm patterns.[1,8,13,15] Pattern-transfer into silicon is a crucial technology in the modern manufacturing of integrated circuits (ICs) and microelectromechanical systems (MEMS). The process is largely responsible for the continuous miniaturization of semiconductor devices, allowing continuation of Moore's law and shrinkage of MEMS devices toward nanoelectromechanical systems. The plasma-based pattern transfer process is well established for moderate aspect ratios and linewidths down to 25 nm and for high aspect ratio structures in the 50–100 nm regime.[11] However, as feature sizes shrink, approaching the 5 nm regime for "Beyond CMOS" devices, feature size and profile shapes must be controlled with tolerances approaching single nanometer dimensions.[8,9]

In this article, we experimentally study for the first time a combination of scanning probe lithography based on Fowler–Nordheim electron field emission for single-digit pattern generation and reactive ion etching at cryogenic temperatures. The combination of both technologies has enabled single electron devices to be built. We report on pattern transfer of nanofeatures written with field-emission scanning probe lithography (FE-SPL) in 10-nm thin calixarene molecular resist and simulations[12,13] of cryoetching to better understand the processes.

II. EXPERIMENT

A. Fowler–Nordheim: Scanning probe lithography with active probes

Several proximity probe-based lithography techniques have emerged recently as promising alternatives to other lithography methods for a wide range of nanoelectronic and nanophotonic applications.[14] A diversity of physical and chemical methods has been used to induce changes in material in a tip–surface and have generated several proximal probe lithographic techniques. During the last three decades, different proximal probe methods with respect to their driving mechanisms have been demonstrated in the patterning process, based on thermal, electrical, mechanical, and diffusive methods. In general, proximal probes are the multitalent instrument for nanotechnology and nanofabrication.[15] They are capable of localizing tip–surface interactions at the nanoscale for metrology and imaging with high speed[16] as well as investigation of material properties and lithography at the single nanometer scale and beyond. Using an STM, atomically precise manipulation has been demonstrated.[17] With hydrogen as an atomic-resist, a selective STM-induced hydrogen desorption process under ultrahigh vacuum conditions is capable of atomically precise patterning to realize single atom transistors.[17,18] However, proximal probe techniques show an extremely low throughput, which is connected with the serial principle of operation and method of addressing the tip.[19] Vector type SPL addressing becomes a very attractive technique. Especially, using a direct development-less operation mode[8] and data splitting in *mix-and-match* provides writing speeds close to single e-beam lithography techniques.[1] The idea of the proposed scanning probe lithography experiments was carried out with a dedicated SPL-tool operated in controlled ambient conditions (40% rh ± 10% rh) and room temperature (21 ± 2 °C). The general setup for the tip-based nanolithography with two control feedback loops is presented schematically in Fig. 1. The active cantilevers are based on well-established thermomechanically actuation principles and a self-sensing scheme, demonstrated and described in more detail in Refs. 20 and 21. The deflection amplitude of the cantilever vibration as well as the static bending of the cantilever is determined by acquisition of the output signal of the integrated piezoresistive deflection sensors. These are forming an integrated Wheatstone-bridge at the point of highest internal stress.[22,23] The dynamic behavior of a cantilever depends on its resonance properties which are a function of beam geometry and material properties.[23] Cantilever displacement and oscillation can be precisely controlled by dissipated electrical power within resistors embedded in the cantilever. In this way, resonance and static cantilever deflection can be excited. An important advantage in the performance of the FE-SPL-technology arises from the fact that the same active-cantilever (Fig. 2) is used for both: direct low-energy Fowler–Nordheim electron exposure of the resist (positive-tone, development-less) using emission from the tip as well as fast noncontact AFM-imaging[16] with atomic resolution (Fig. 3) employed for pre- and postinspection and for pattern overlay alignment and stitching. A closed-loop SPL tool uses the standard dynamic mode amplitude modulation AFM feedback loop for topographic imaging—a second independently working feedback loop for SPL-lithography.

More generally, the characteristic system behavior can be described in a first approximation by maintaining a constant electric field strength at the tip apex for constant electron

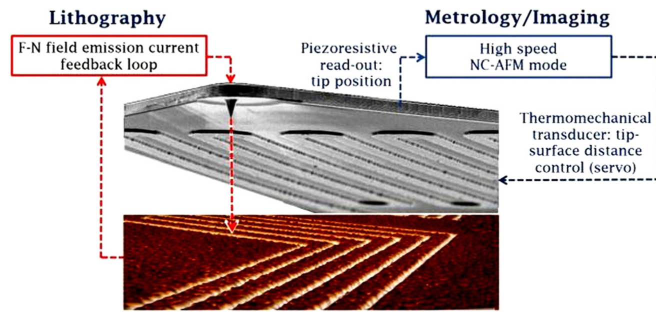

FIG. 1. (Color online) Principle setup of the lithography system incorporating an electron field-emission current feedback loop for SPL and a force feedback loop for AFM imaging. Switching between either mode (imaging and lithography) is possible. Thus, the same nanoprobe is used for both direct writing of nanofeatures using a low-energy FN-field-electron emission from nanoprobe-tip and AFM-imaging for pre- and postinspection, as well as for pattern overlay alignment (Refs. 1, 8, and 12).

emission,[24] characterized by the Fowler–Nordheim (F-N) equation. To control the electron emission current required for the lithography feedback loop, a two-stage high precision current-to-voltage (IV)-converter with subsequent amplification stage was developed. The novel preamplifier is characterized by a transfer function of 5 V/nA and 0.07 pA noise level at 1.5 kHz bandwidth. For high resolution lithography and imaging, tip shape and tip radius become crucial. In both cases, resolution is determined primarily by the sharpness of the tip. Therefore, we have developed a recipe to modify the tip asperity by electron beam induced deposition Pt-nanotips positioned on top of the silicon tip. The radius of curvature is approximately 5 nm, enhancing the resolution capability for imaging and lithography significantly.[1]

Switching between imaging and patterning modes enable (1) resist surface inspection before patterning; (2) AFM-based topology registration, stitching, and overlay alignment; (3) patterning by using proximity (noncontact) electron field emission F-N-SPL with variable exposure parameters; and (4) *in situ* inspection and metrology after each patterning cycle. Thereby, the precision of alignment is mainly determined by the measurement precision of the positioning stage itself,

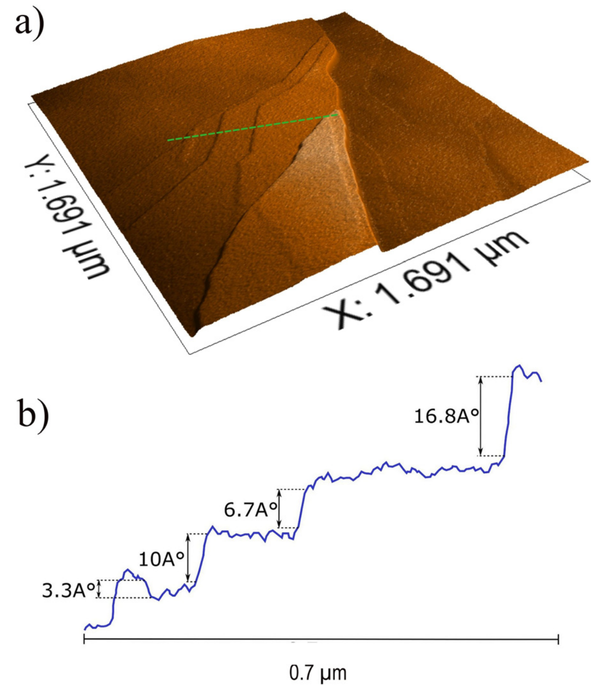

FIG. 3. (Color online) Atomic force microscope (AFM) topography image of HOPG, indicating single atomic steps obtained at ambient room conditions by thermomechanically actuated active cantilever.

which provides to subnanometer resolution capabilities.[8] A combination of three important elements provides unique nanolithography capabilities with respect to resolution and overlay precision: (1) ultra-low-energy electrons emitted from the scanning tip, (2) molecular resist, and (3) principles of proximity probes technology. In comparison to conventional electron beam lithography, advantages of SPL are as follows:

(1) Ambient condition nanolithography—neither vacuum nor a special gas environment is required.
(2) No complex electron optics is needed enabling relatively easy setups.
(3) Scanning probes provide a closed loop scheme functionality, delivering a unique set of integrated functionalities.

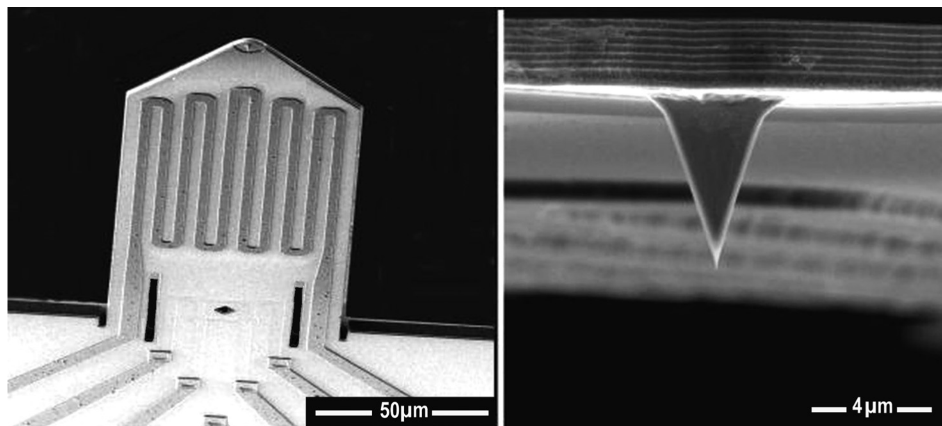

FIG. 2. Active-AFM-SPL cantilever (scale bar left: 50 μm) with integrated readout-force sensor and thermomechanical transducer and silicon tip used for electron field-emission and AFM. Right: AFM image of silicon tip used for FN-electron emission and imaging. The thermomechanical transducer is shaped in the form of meander made from Al/Mg alloy. Four piezoresistors which form a Wheatstone measurement bridge are placed at the base of the cantilever (Refs. 21–23).

(4) Less proximity effects by reduction or elimination of ultralow energy electrons and thus more sensitive sample-interaction.

An onto-cantilever integration approach for bending-readout and self-deflection for AFM is a promising alternative in next-generation scanning proximal probe technologies. Using such self-sensing and self-actuated—or so called active—cantilevers,[9,20,21] a significant speed improvement can be achieved. No complex laser optics is necessary, eliminating any need for laser adjustment and calibration for AFM operation.[16] Spacecraft instrument integration has been shown to be space-saving and thus profitable.[25] Our superior piezoresistive read-out delivered AFM images after years of space travel.[26] Aboard ESA's Rosetta/Midas mission, launched on March 2, 2004, it has spent ten years in space and reached Comet 67P/Churyumov-Gerasimenko in 2014.

Thermomechanical transduction was first reported by Wilfinger *et al.*[27] The electrical heating power into the transducer is proportional to the square of the current, while the frequency of the sine-wave voltage driver is half the cantilevers' resonant frequency.

Active cantilevers with thermomechanical transduction make it possible to build an extremely compact AFM for integration in scanning electron microscopes (SEM)[28] or for high speed wafer and mask inspection in the semiconductor industry.[19,29] Fundamental benchmarks of an active cantilever are as follows: (1) downsizing-scalability,[15] (2) routinely atomic resolution,[16] (3) very simple use, (4) high operation speed due to high bandwidth,[15] and (5) excellent preformation in any ambient. In summary, active probes are more perspective in all future developments in the scanning probe techniques expectation in comparison to passive probes using optical read-out. Instead of having to move a bulky sample stage, the more dynamic measuring head must be traveled across the sample only. This fundamentally simplifies AFM architecture, which can be newly arranged in a space-saving manner.

The FE-SPL instrument is based on a cross-beam design. As shown in Fig. 4, the system base and suspension beam are made from massive blocks of aluminum alloy, minimizing the thermal drift effects. The mechanical stability of this setup was simulated by finite element methods and optimized for a short and robust Z-loop also benefitting from the integration of a large bottom coarse positioning stage. In addition, due to the bridge setup, an increased movement area of the coarse positioning unit is created, enabling a patterning range of up to $100 \times 100\,\text{mm}^2$ and capable for upgrading to $150 \times 150\,\text{mm}^2$. The main SPL cantilever scanner unit is mounted in the center of the cross-beam. To improve the dynamics of the cantilever scanner system, the total mass was reduced significantly due to employment of the active cantilever. The use of the active cantilever allows easier system integration, higher speeds of FE-SPL and AFM modes, as well as better flexibility compared to conventional passive cantilever approaches. Two different cantilever scanners could be applied: one providing a $10 \times 10\,\mu\text{m}^2$ scan area and the other with a $200 \times 200\,\mu\text{m}^2$ scan area. The additionally integrated bottom stage enables a step-and-repeat functionality within an active area of a 4 in. wafer. The utilization of the step-and-repeat process in combination with FE-SPL shows a great potential in terms of mix-and-match lithographic strategies, which allow SPL-based patterning of the critical dimension features into the previously written large-scale structures, which were created by common lithographic methods like EBL. In step-and-repeat lithography systems, global positioning and overlay alignment is an issue. Due to FE-SPM-based pattern overlay alignment capability, the step-and-repeat method can provide excellent overlay and placement accuracy.[28] The resolution of the readout signal of the bottom wafer-stage movement is 10 nm and the average movement error measured for the set of 100 μm steps is smaller than 80 nm.

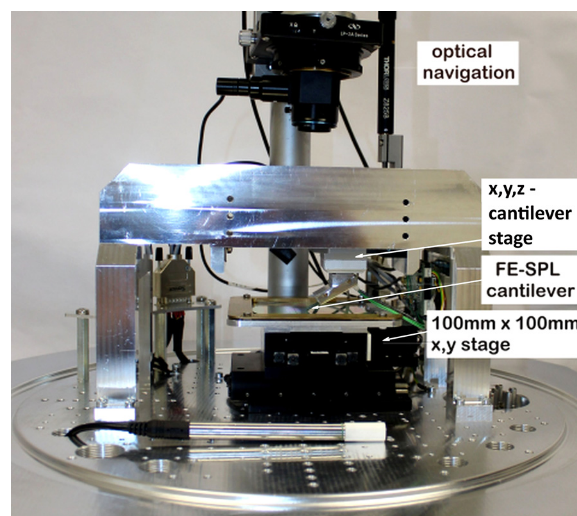

FIG. 4. (Color online) Field-emission SPL setup combining top scanner and bottom coarse positioning stages enabling a step and repeat based SPL/AFM operation.

B. Cryogenic etching

Cryogenic etching was carried out in an inductively coupled plasma (ICP) source with a liquid nitrogen cryogenically cooled stage. The tool is an ICP cryoetching tool with a 3 kW/2 MHz ICP source and a 300 W/13.56 MHz platen power generator, both having automatic impedance matching. The operating temperatures can be set in a range from −150 to 400 °C. For thermal contact, the system uses "helium backside cooling," where helium is introduced into the gap between the backside of the wafer and the thermally controlled platen. It is equipped with a 1600 l/s turbopump. The chamber is fitted with 300 mm diameter Al_2O_3 liners and equipped with a loadlock system. Eight process gases (SF_6, CF_4, Ar, O_2, He, CH_4, CHF_3, and C_4F_8) can be used. The samples have been etched in the described tool using a so-called cryoetching process. This relies on the low temperature of the substrate and the deposition of silicon oxyfluoride film at the sidewalls. To achieve an anisotropic etching profile, it is necessary to reduce the lateral etching rate compared to the vertical etching rate. In cryoetching, this is

accomplished by the deposition of a SiO_xF_y film on the sample surface. As the SiO_xF_y film is not stable at room temperature, the sample must be cooled down to low temperatures. Temperatures range from −120 to −60 °C, with typical temperatures around −100 °C. At these temperatures, the SiO_xF_y film forms at the sample surface and prohibits etching of the silicon material. To promote the etching reaction in the vertical direction, the film formation must be reduced, and any film already deposited must be removed by ion bombardment. Ions are accelerated from the plasma sheath due to a potential difference between plasma bulk and sample surface. Depending on the actual process conditions, such accelerated ions will have energies of about a few tens of electron-volt and a direction of more or less vertical. At the vertical sidewalls, the ions have a glancing angle of incidence to the surface, resulting in little or no sputtering of the protective polymer film. However, at the bottom of the etched feature, the ions have an almost 90° vertical angle of incidence; hence, the sputtering yield is high enough to effectively remove any polymer already deposited and to prohibit further polymer deposition. Therefore, the etching proceeds only in the vertical direction, and profiles with vertical sidewalls are achieved.[10,30–33] Figure 5 shows three silicon test samples (10 nm calixarene resist mask) etched using the procedures described. The main conditions are 11 W platen power, 5 mTorr pressure, SF_6: 10 sccm, O_2: 2 sccm, and −120 °C temperature. Sample SNM-B59_S1 was etched at +20 °C, SNM-B59_S5 at −120 °C, and SNM-B59_S2 at −120 °C with the process gas being a mixture of 13 sccm SF_6 and 0 sccm O_2. Note that very little amounts of oxygen may originate from the quartz sample holder. These experiments illustrate the necessity of both the low substrate temperature and particular amount of oxygen flow for obtaining anisotropic etching profiles. The plasma is monitored by optical emission spectroscopy (OES). Prior to actually etching a process sample, the process is carried out with a dummy wafer to verify the plasma conditions and the conditioning of the chamber. Spectra are shown in Fig. 6. From the variety of peaks, only the intensity of the peaks at 657, 704, and 778 nm is shown. The peak at 704 nm is very likely due to fluorine, while the peak at 778 nm is probably due to oxygen. The peak at 657 nm may originate from hydrogen. Figure 6(a) shows the time trends of the three peaks recorded during conditioning of the chamber using a dummy wafer (a blank silicon wafer). The OES optics look across the plasma chamber parallel to the wafer surface. The plasma ignition is at about 25 s (of relative time). The peaks rise to relatively high values and return to a saturation level. In the case of this experiment, the chamber was already conditioned to the process; hence, the magnitude of the peaks (or spectral lines) remains constant with time. At about 450 s, the plasma is switched off and ignited again at about 470 s. Note that the magnitude of the spectral lines return to the values before the switching off of the plasma, which indicates that the plasma chamber is in a state for reproducible processes. Immediately after plasma ignition, the intensity of the fluorine peak (704 nm) is high, as can be seen from the OES spectra. After a time of 5–10 s, the fluorine peak drops down

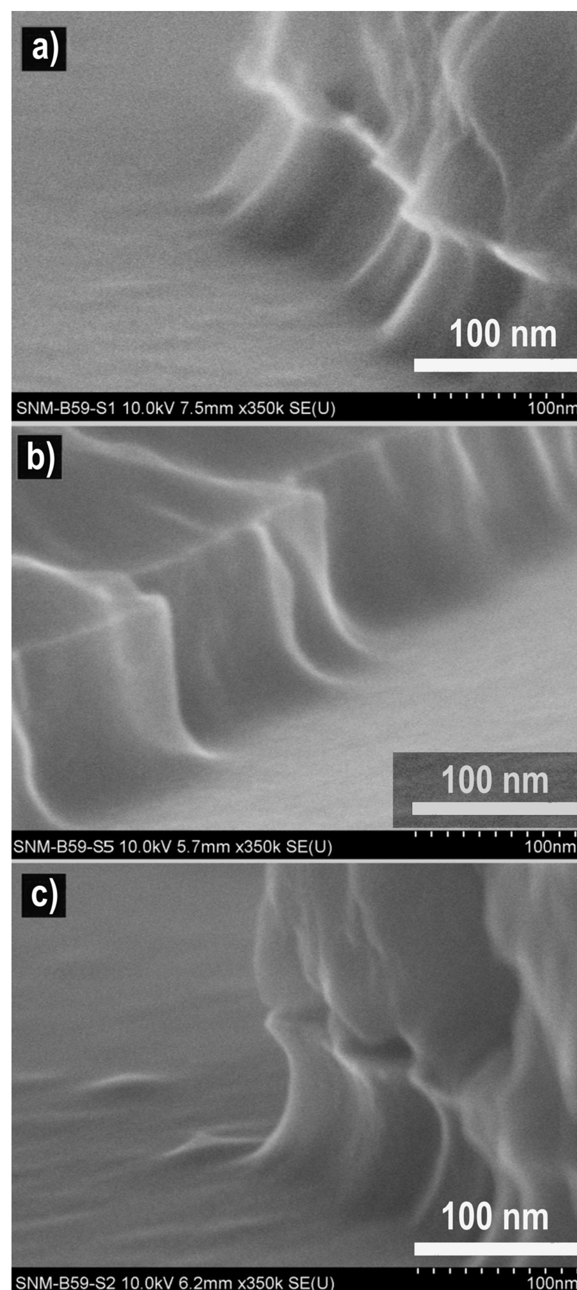

FIG. 5. Three silicon samples with calixarene resist etched at different temperatures [(a) 20 °C, (b) and (c) −120 °C] and oxygen flow rates [(a) and (b) 2 sccm, (c) 0 sccm]—(a) sample SNM-B59_S1; (b) sample SNM-B59_S5; (c)sample SNM-B59_S2. Both samples (a) and (c) show isotropic profiles, while sample (b) shows a vertical profile.

to a lower level. The other peaks show a similar behavior (immediate rise at the beginning, then a drop to a lower saturation level), however, at a different time constant or time function. The hydrogen peak (657 nm) shows a decay somewhat similar to an exponential decay, while the oxygen (778 nm) peak shows a less pronounced decay than the fluorine peak (704 nm). The oxygen peak is missing altogether for the third sample (SNM-B59_S2), which was processed with no oxygen at all. The peaks show a very similar behavior for the three samples and the dummy wafer (with the exception of sample SNM-B59_S2, where the oxygen peak

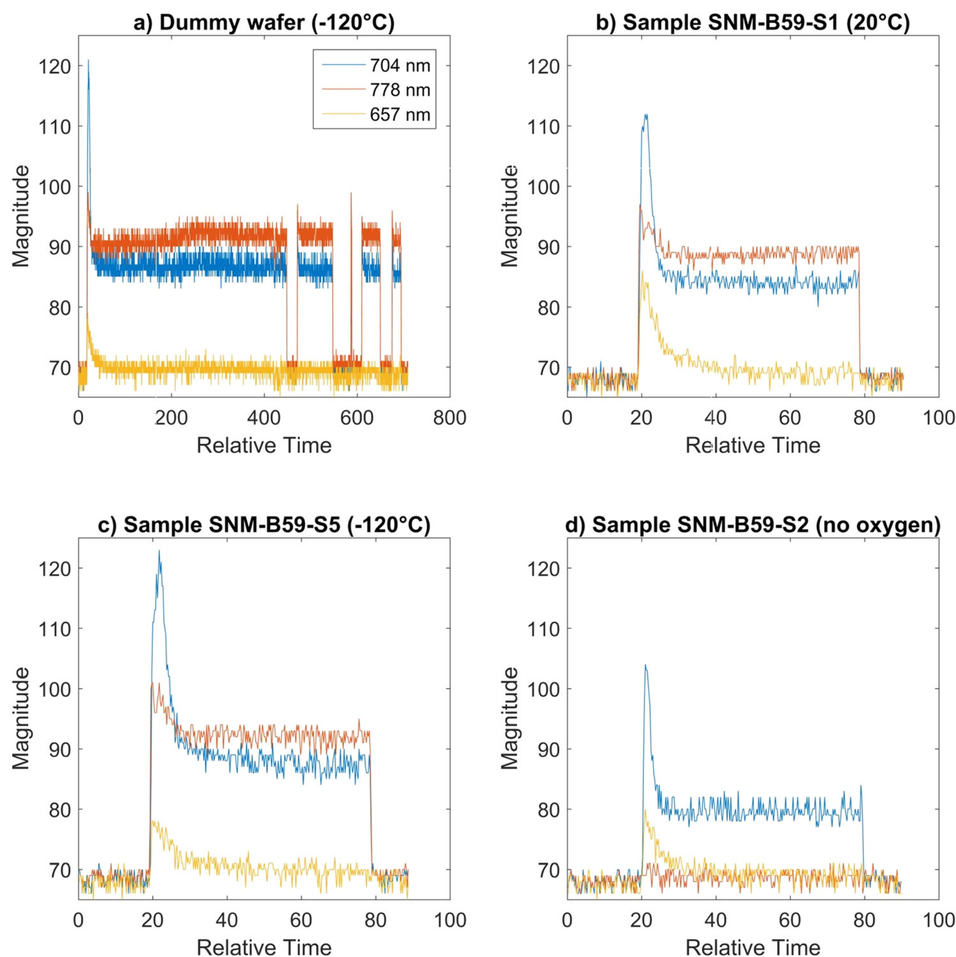

FIG. 6. (Color online) Time trends of selected plasma peaks. The "Relative Time" is in seconds, and the magnitude of the peaks is in astronomical unit, but comparable between graphs.

is missing, probably due to no oxygen in the feed gas. The reason for the behavior of the peaks immediately after plasma ignition is not yet known. It could be the layer of native oxide on the silicon surface, or adsorbates of humidity, but the exact reason is not yet known. Using the anisotropic technique, a number of samples have been processed, followed by lithography using the process described above. Etching depths of 60 nm have been achieved (Fig. 7).

III. MODELING OF CRYOGENIC ETCHING

We also employ user simulations of cryoetching in order to understand the process. For this purpose, we have recently developed a silicon cryoetching simulation model[12] and embedded it into our plasma etch profile simulation software described in more detail in Refs. 34–36. Based on previous works,[37,38] the program code supports 2D simulations, assuming that a cross-section of an infinitely long trench is being etched. The simulation procedure focuses on feature scale calculations in which the process is considered only at the distance of several microns around the feature. That is to avoid performing the plasma chemistry modeling and not to calculate the transport of the available plasma species to the sample, several assumptions are made regarding the species and their fluxes, as well as the angle and energy distribution of each species above the surface of the sample. Using these data, the feature scale module calculates the neutral and ion species transport inside the feature. Local fluxes and local angular distributions of each species can be determined at any point on the evolving surface profile. These data are then used in surface reaction models to calculate etch and deposition rates, with the calculations done sequentially, in a time loop, to model the evolving feature profile.

Feature scale simulations of SF_6/O_2 cryogenic silicon etching have been previously addressed by several groups[39–47] for etching of features predominantly in the micron scale. The simulation model presented here also uses a semiempirical approach, whereby the inputs for the species above the sample are determined by means of a calibration procedure. A more detailed description of the model can be found in Ref. 12 where the previous studies were extended in order to understand the more recent experimental work at the sub-100 nanoscale, and after full calibration, simulations were applied at the nanoscale. Here, we briefly recall the main parameters of the model. For SF_6/O_2 silicon cryoetching simulations, the model considers reactive neutrals and ions, where fluorine and oxygen atoms are the two main reactive neutrals.[40] The effective flux of fluorine atoms on

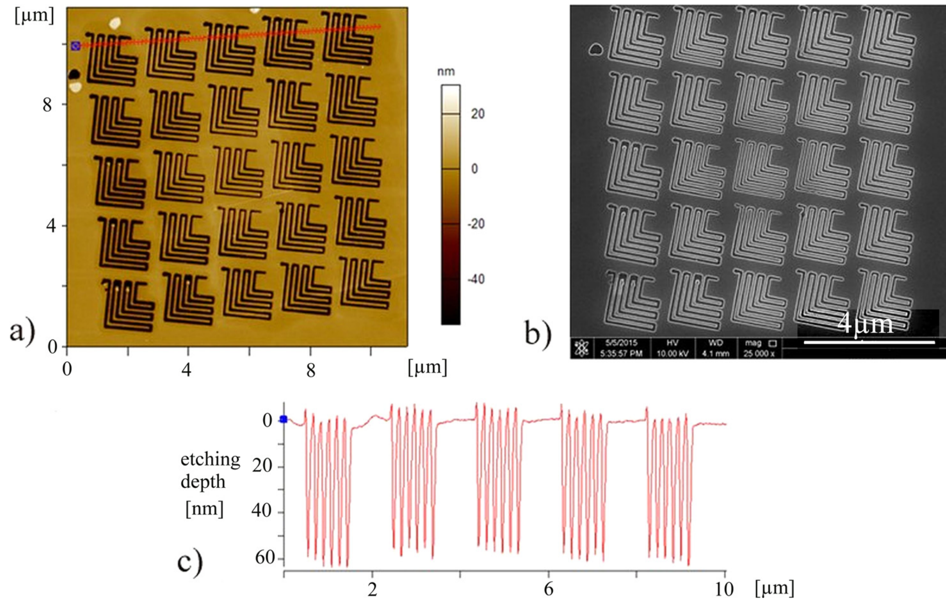

FIG. 7. (Color online) (a) AFM topography image and (b) SEM images and (c) profile graph of etched in silicon (60 nm deep) test pattern written with FE-SPL in 10-nm thin calixarene molecular resist. The patterns are written in the positive-tone lithography mode (direct removal), and the smallest feature width is 19 nm.

the surface Φ_F stands for the total flux of F atoms arriving at the surface either in an atomic form or as part of a more complicated neutral radical. The same is assumed for the effective oxygen flux Φ_O. An isotropic distribution (no angular dependence) is assumed for the fluxes Φ_F and Φ_O, whereby the energy of the appropriate species is assumed to be equal to thermal energy. SOF_3^+ is the dominant positive ion in the discharge,[43] and it represents in the model[12] all positively ionized species delivered to the surface with the total ion flux Φ_i. The fluxes Φ_F, Φ_O, and Φ_i are input parameters to the profile simulations and their values are estimated during the calibration process. The use of the low pressure regime (6 mTorr) in the all Si cryoetching experiments considered allows application of a simplified sheath model[34,35] for estimation of the ion angle and energy distributions. The average value for the energy E_{ion} of the incident ions is calculated using the DC bias value V_{DC} as measured during the plasma etching experiment being simulated. In addition, the time-averaged plasma potential V_p is such that

$$E_{ion} = e(V_{DC} + V_p), \tag{1}$$

where e is the elementary charge. The plasma sheath is considered collisionless (a more detailed description of all assumptions made for the sheath model can be found in Ref. 12); thus, the positive ions reach the sample with a very directional angle distribution, which in the model is assumed to have the form of a Gaussian distribution. Considering α as the angle of incidence of the ion approaching the sample and σ_α as the standard deviation, the ion angle distribution function (IADF) close to the sample is as follows:

$$\mathrm{IADF}(\alpha) = \frac{1}{\sigma_\alpha\sqrt{2\pi}}\exp\left\{-\frac{\alpha^2}{2\sigma_\alpha^2}\right\}. \tag{2}$$

The simulator employs transport models for each of the considered plasma species to calculate local fluxes and local angular distributions of the considered plasma species at each individual point of the simulated surface profile. The input to the calculation of species transport within the microstructure are the flux values, angle, and energy distributions of ion and neutral species previously defined at the sheath boundary above the sample. For the neutral species transport, the effects of adsorption and desorption are considered by using Langmuir adsorption kinetics. Using the adsorption of F species on silicon as an example, the adsorption rate will be

$$R_{ads} = S_F\Phi_F(1 - \Theta_F) = S_{eff}\Phi_F, \tag{3}$$

where Φ_F is the total fluorine flux consisting of two fluxes—the flux coming directly from the plasma as well as the flux of reflected species, S_F is the temperature dependent sticking coefficient of fluorine on a clean silicon surface, Θ_F is the fluorine surface coverage, and S_{eff} ($S_{eff} = S_F(1 - \Theta_F)$) is the effective sticking coefficient of fluorine. Based on the data from literature,[40] we assume the oxygen sticking coefficient S_O is unity on bare silicon at low temperature in all considered simulations, while S_F is the value estimated during the model calibration procedure. For the ion transport, also several assumptions are made.[12] First, changes to ion trajectories due to particle–particle collisions are not considered and the influence of mask surface charging was found negligible;[12] thus, the energy of the incident ions at any point of the microstructure surface is considered equal to that at the lower sheath boundary [calculated by Eq. (1)]. Furthermore, for the etching experiments currently addressed by the model, the ion reflections at the feature sidewalls are not taken into account explicitly (i.e., through Monte Carlo simulations), but are only implicitly considered in the calculations of etching yield

(the reason is explained in detail in Ref. 12). With this assumption, it is enough for the model to account only for direct line-of-sight ion shadowing to determine local ion flux and local ion angle distribution at each point of the simulated surface profile.

For simplicity, erosion of the mask and its consequences is not considered. In terms of plasma etching of silicon, the total etching rate can be expressed[48] as

$$ER_{\mathrm{tot}} = ER_{\mathrm{chem}} + ER_{\mathrm{sp}} + ER_{\mathrm{i}}, \tag{4}$$

where ER_{chem} is the pure chemical etch rate, ER_{sp} is the etch rate due to physical sputtering mechanism, and ER_{i} is the etch rate due to the ion-assisted etching. For the process conditions under consideration, the influence of the physical Si sputtering on the total etch rate is insignificant[37] and hence is neglected in the model[12] such that the total Si etching rate is given by

$$ER_{\mathrm{tot}} = \frac{1}{\rho_{\mathrm{Si}}}\left(\frac{\chi_F \sigma_{\mathrm{Si}} \Theta_{\mathrm{F}}}{4} + Y_{\mathrm{Si}} \Phi_{\mathrm{i}} \Theta_{\mathrm{F}}\right), \tag{5}$$

where the first term in the sum represents the pure chemical etching, and the second one stands for the ion-assisted chemical etching. In Eq. (5), ρ_{Si} is the silicon density, $\chi_F \sigma_{\mathrm{Si}}$ is the chemical etch reaction rate constant (χ_F is the coefficient defining the reaction frequency and σ_{Si} is the surface density of silicon atoms), and Y_{Si} is the ion-assisted etch yield. Furthermore, SiF_4 is considered the primary etch product of the F-Si chemical etch reaction.[49] The ion-assisted etch yield Y_{Si} represents the yields of all kinds of etch reactions induced by the ion bombardment of the silicon surface, which results in removing some amount of Si atoms into the gas phase. The yield depends on the energy E_{ion} and incident angle α_{in} of the impinging ions. In the model, E_{ion} is equal for any surface point and is determined by Eq. (1), while the local angular distribution of incident ions at each point of the target surface is determined by the ion transport model. Using the yield form reported by Steinbrüchel[50] and considering the yield dependence $f(\alpha_{\mathrm{in}})$ on ion angle of incidence α_{in} the form of the yield per one incident ion is given by the expression

$$Y(E_{\mathrm{ion}}, \alpha_{\mathrm{in}}) = A(\sqrt{E_{\mathrm{ion}}} - \sqrt{E_{\mathrm{th}}}) f(\alpha_{\mathrm{in}}), \tag{6}$$

where the parameter A and the sputtering threshold energy E_{th} depend on the particular projectile–target combination. In the model, the yield curve is assumed to have the form similar to that used by Marcos *et al.*[42] and Belen *et al.*[43,44] The yield is constant (1.0) near normal incidence and monotonically decreases with the angle of incidence. We use a pair of parameters θ and ψ and denote this dependence as $(\alpha_{\mathrm{in}}) = \{\theta : \psi\}$.[12] The model considers two yield dependencies, the silicon yield and the oxygen yield. Consistent with established literature values,[42,43,51] the ion incident angle dependency of the silicon yield Y_{Si} is assumed to have the form $f(\alpha_{\mathrm{in}})_{\mathrm{Si}} = \{60^\circ : 85^\circ\}$ and is kept unchanged in all simulations. To investigate how the oxygen sputtering yield from the SiO_xF_y passivating film varies as a function of oxygen flux and feature size, the model parameterizes the form of the oxygen sputtering yield dependency on the ion angle of incidence [denoted as $f(\alpha_{\mathrm{in}})_{\mathrm{O}} = \{\theta; \psi\}$]. The parameter A_{O} in the oxygen sputtering yield, Y_{O} as well as the variables ϑ and ψ of the $f(\alpha_{\mathrm{in}})_{\mathrm{O}}$ parameter in Y_{O} were fit within the simulations by matching simulated profiles with experimental results to investigate this effect. The fluorine and oxygen surface coverages Θ_{F} and Θ_{O} are determined by means of Langmuir–Hinshelwood-type surface site balances (details can be found in Ref. 12).

After the model was integrated into the simulator, it was calibrated with respect to the cryogenic plasma etch hardware[52] and processes being tested. In terms of the calibration (all details can be found in Ref. 12), a series of experiments and simulations were conducted to estimate the most critical parameters of the model. A summary of all the model parameters and which require calibration is shown in Table I.

Starting by etching features from 500 nm to 2 μm,[53] the model was calibrated and a fit made to the relevant parameters. After this, it was possible to extend the model to the deep nanoscale and to simulate silicon etching of 25 nm half-pitch lines[12] using a very thin mask derived from block copolymer lithography.[54] The model parameters obtained[12] are summarized in Table II.

Since the plasma etching recipe considered (see Table III) is very similar to the one previously addressed (see nanoscale simulation in Ref. 12), only the ratio of F to O fluxes was adjusted (F flux has decreased from 1.5×10^{18} to $0.8 \times 10^{18}\,\mathrm{cm^{-2}\,s^{-1}}$, while O flux has remained unchanged) to provide good fit of simulation profiles to the experimentally obtained data (see Fig. 8).

IV. FABRICATION OF SINGLE ELECTRON DEVICES

The reduction in CMOS device dimensions, combined with the development of new device structures, has delivered continuous improvements in the speed, complexity, and packing density of integrated circuits. However, as present CMOS device feature sizes approach the scale of 10 nm or even less, major challenges are encountered, associated with a change in the fundamental nature of the device from “classical” operation to that limited by quantum mechanical effects. A quantum-effect beyond CMOS technology, e.g., one based on SETs and quantum-dot (QD) based devices,[55,56] can require scaling in all three dimensions to $<$5 nm. These devices, unlike classical devices, inherently improve in performance with the reduction in size and additional to conventional nanoelectronic applications, may also provide building blocks for advanced quantum computation systems.[57,58]

In recent years, there have been great advances in SET devices operating at RT, where the single-electron charging energy $E_c \gg k_B T = 25$ meV at temperature $T = 290$ K. Here, the QD forming the core of the device is well below 10 nm in size and may be defined within a Si nanowire in the presence of surface roughness or doping disorder,[59,60] by (1) pattern dependent oxidation of a point contact,[61,62] (2) using Si nanocrystals,[7,63,64] or (3) ultrathin silicon.[63] In particular, in

TABLE I. Summary of the model parameters to be determined.

Parameter	Notes
Fluorine flux, Φ_F	Variation with plasma conditions is obtained from fitting during the calibration process using auxiliary data taken from literature. Absolute value is estimated by matching simulated profiles with experiments.
Oxygen flux, Φ_O	Variation with plasma conditions is obtained from fitting during the calibration process. Auxiliary data taken from literature.
Fluorine sticking coefficient on a clean Si surface, S_F	Estimated by matching simulated profiles with experiments.
Oxygen sticking coefficient on a clean Si surface, S_O	Taken from literature and kept constant (1.0).
Chemical etch rate constant, $\chi_F \sigma_{Si}$	Estimated by matching simulated profiles with experiments.
O recombination constant, $\eta_O \sigma_{Si}$	Taken from literature and kept constant ($4 \times 10^{13}\,cm^{-2}\,s^{-1}$).
Ion flux, Φ_F	Taken from literature.
Standard deviation of the ion angular distribution, σ_α	Estimated by matching simulated profiles with experiments.
Ion incident angle dependency of silicon etch yield, $f(\alpha_{in})_{Si}$	Assumed to be $f(\alpha_{in})_{Si} = \{60^\circ : 85^\circ\}$ and is kept unchanged in all simulations.
Ion incident angle dependency of oxygen sputtering yield, $f(\alpha_{in})_O$	Estimated by matching simulated profiles with experiments.
Silicon etching threshold energy, $E_{th,Si}$	Taken from literature and kept constant (15 eV).
Oxygen sputtering threshold energy, $E_{th,O}$	Taken from literature and kept constant (10 eV).

our previous work, RT SET operation with $Ec = e^2/2C = 0.5\,eV$ ($\sim 20 k_B T$) at 290 K (the QD total capacitance is C) was demonstrated using an oxidized 50×50 nm point-contact, fabricated by EBL. After heavy oxidation, it was estimated that the unoxidized QD core in this device was only $\sim$5 nm. Here, the point-contact was defined in the $\sim$30 nm thick top SiON layer of a silicon-on-insulator (SOI) wafer. Following oxidation, at the point-contact "neck" between the source and drain an island, or QD, was formed due to self-limiting of the oxidation at the point-contact center, due to increasing stress in the Si core. The FE-SPL method provides an alternative to high-resolution EBL for the fabrication of RT SETs. In particular, these methods may provide a means to define finer features, and to minimize damage or charge trapping in the sample due to high-energy electron beams. The fabrication of point-contact SETs by FE-SPL is now discussed. The devices were fabricated on SOI chips consisting of a top layer of silicon 12 nm thick and p-doped (9–15 Ω cm). This was separated from a ⟨100⟩ oriented silicon substrate, also p-doped (9–15 Ω cm) by a buried oxide (Box) layer 25 nm thick. The top silicon layer was doped by phosphorous ion implantation with a dose of $2 \times 10^{15}\,cm^{-2}$ at 2 keV, giving a maximum doping of $\sim 5\text{–}6 \times 10^{20}$ [P]-atoms/cm^3. The top silicon was first patterned by optical lithography to give arrays 4×4 device areas (30, 50, and 100 μm available), with each device area surrounded by 12 contact pads and registration marks. This pattern was etched into the top silicon fully down to the Box layer. This gave isolated areas on which to fabricate devices linked to bond pads. For this work, chip sizes of 15×15 mm were used. A resist layer of calixarene was coated to a thickness of 12–17 nm. Line exposures were made using the calixarene in a positive self development mode, which facilitated the direct removal of line widths from 200 nm for large separation lines down to 10 nm when defining the inner core of the SET device in high resolution. Using this method, the outline of the SET devices was defined. The calixarene pattern was transferred into the top silicon layer using a cryogenic plasma etching process. An SF_6/O_2 process was performed at $-120\,^\circ$C using a DC bias <100 V. The samples were passivated by thermal oxidation at 850 °C for $\sim$10 min,

TABLE II. Summary of the model parameters determined in the previous nanoscale cryoetching simulation.

Parameter	Value
Fluorine flux, Φ_F ($cm^{-2}\,s^{-1}$)	1.5×10^{18}
Oxygen flux, Φ_O ($cm^{-2}\,s^{-1}$)	1.3×10^{17}
Fluorine sticking coefficient on a clean Si surface, S_F	0.75
Oxygen sticking coefficient on a clean Si surface, S_O	1.0
Chemical etch rate constant, $\chi_F \sigma_{Si}$ ($cm^{-2}\,s^{-1}$)	3.0×10^{18}
O recombination constant, $\eta_O \sigma_{Si}$ ($cm^{-2}\,s^{-1}$)	4×10^{13}
Ion flux, Φ_F, ($cm^{-2}\,s^{-1}$)	1.1×10^{16}
Standard deviation of the ion angular distribution, σ_α	0.1
Ion incident angle dependency of silicon etch yield, $f(\alpha_{in})_{Si}$	$\{60^\circ : 85^\circ\}$
Ion incident angle dependency of oxygen sputtering yield, $f(\alpha_{in})_O$	$\{60^\circ : 85^\circ\}$
Silicon etching threshold energy, $E_{th,Si}$ (eV)	15.0
Oxygen sputtering threshold energy, $E_{th,O}$ (eV)	10.0

TABLE III. Plasma etch recipe used for high aspect ratio anisotropic cryoetching of 19 nm wide features.

Parameter	Value
Total SF_6/O_2 gas flow rate	32 sccm
SF_6 to O_2 ratio in the total gas feed	16–16 sccm
Pressure	6 mTorr
ICP power	1000 W
DC bias	−50 V
Wafer temperature	−120 °C
Etch duration	30 s

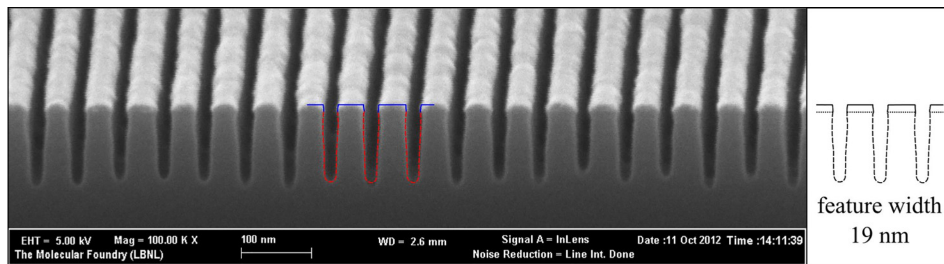

Fig. 8. (Color online) Utilization of the implemented model for simulation of cryogenic silicon etching at the nanoscale (feature width of 19 nm and mask height of 10 nm). The simulation demonstrates a very good agreement with the experiment.

resulting in the growth of ~10 nm oxide and depending on the width of the silicon neck producing a quantum dot having a diameter <5 nm. Thus, using standard tools, this process facilitated the formation of quantum dots, smaller than the lithographic limits. Contact windows were opened in this oxide to the silicon conductors and their bond pads using photolithography. Photoresist S1828 was spin-coated to form a resist layer ≈3.5 μm thick. This was baked, first on a

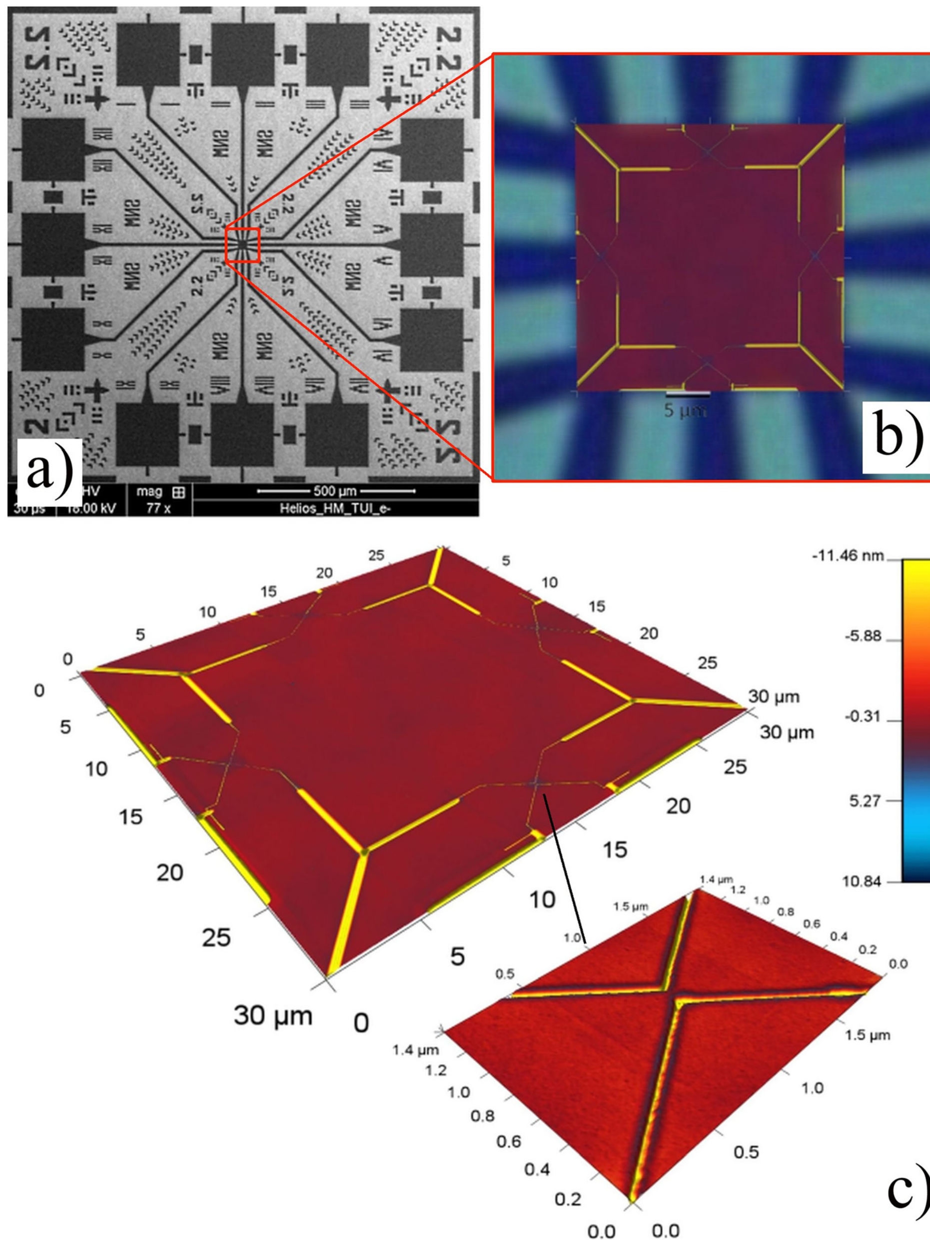

Fig. 9. (Color online) Mix and Match lithography patterning. (a) SEM-image of the optical-lithography step of circuit containing four point-contact SETs. (b) Optical image, overlaid with AFM image, of the central region for FE-SPL. Four SETs have been defined in this area. (c) High-resolution AFM image of the point-contact SET. The source/drain regions are on the left/right hand side of the device.

hotplate at 65 °C for 1 min then at 85 °C for 1 min, and finally, an oven at 115 °C was used for 1 min. A dark field mask was exposed using a power density of 5.3 mW/cm^2 for 160 s and developed in MF319 for ∼2 min followed by a descum for 3 min and a HF dip for 1 min. The same mask was used again to lift-off structure but with a slight underexposure to ensure that contact was only made to the doped silicon. A metal layer consisting of ∼20 nm Cr and ∼200 nm Al was deposited by evaporation, with the unwanted metal and resist is removed via lift-off. SOI material with an ultrathin top Si layer, ∼10 nm thick, was used as the substrate. A general layout containing four single devices, contacted to surrounding fields defined by optical lithography, is shown in Figs. 9(a) and 9(b). Figure 9(c) shows a high resolution AFM image of a device. Point-contacts with width of 60, 40, 30, and 20 nm (preoxidation) were fabricated. FE-SPL patterning was used only in the predefined center field areas (30×30–$100 \times 100\,\mu$m^2), which were surrounded by interconnect regions. Here, SPL was used to ablate a 12–17 nm thick calixarene layer, acting as a positive resist. The point contact pattern was written as lines in the resist, and following lithography, cryogenic plasma etching was used to transfer the written pattern into the top Si. Line widths of ∼20 nm after pattern transfer, with etching depths of ∼16 nm (i.e., into the buried oxide region) were achieved. Following resist removal, oxidation was used to define a QD within the point-contact, to form the SET. Optical lithography was then used to define ohmic contacts, followed by dicing and wire bonding to allow electrical characterization.

Electrical characterization was performed in a RT probe station and a CTI-Cryogenics closed cycle helium cryostat using an Agilent 4155B parameter analyzer. The measurements of the drain–source current (I_{ds}) versus drain–source voltage (V_{ds}) from a 30 nm point-contact are shown in Figs. 2(a)–2(d), as a function of temperature, from 290 to 150 K. Figures 10(e)–10(h) show the corresponding drain–source conductance (g_{ds}) characteristics. A nonlinear asymmetric I–V characteristic is seen in (a) at 290 K, with traces of a current step at $V_{ds} = \sim-0.1$ V (corresponding to a peak in the plot of g_{ds} vs V_{ds} in (b)). The current/conductance magnitude reduces as T reduces to 200 K with the g_{ds} peak becoming more prominent [(b)–(c), and (f)–(g)]. At 150 K, [(d) and (h)], the characteristics become more symmetrical, with current steps [arrowed in (h)] observed for both positive and

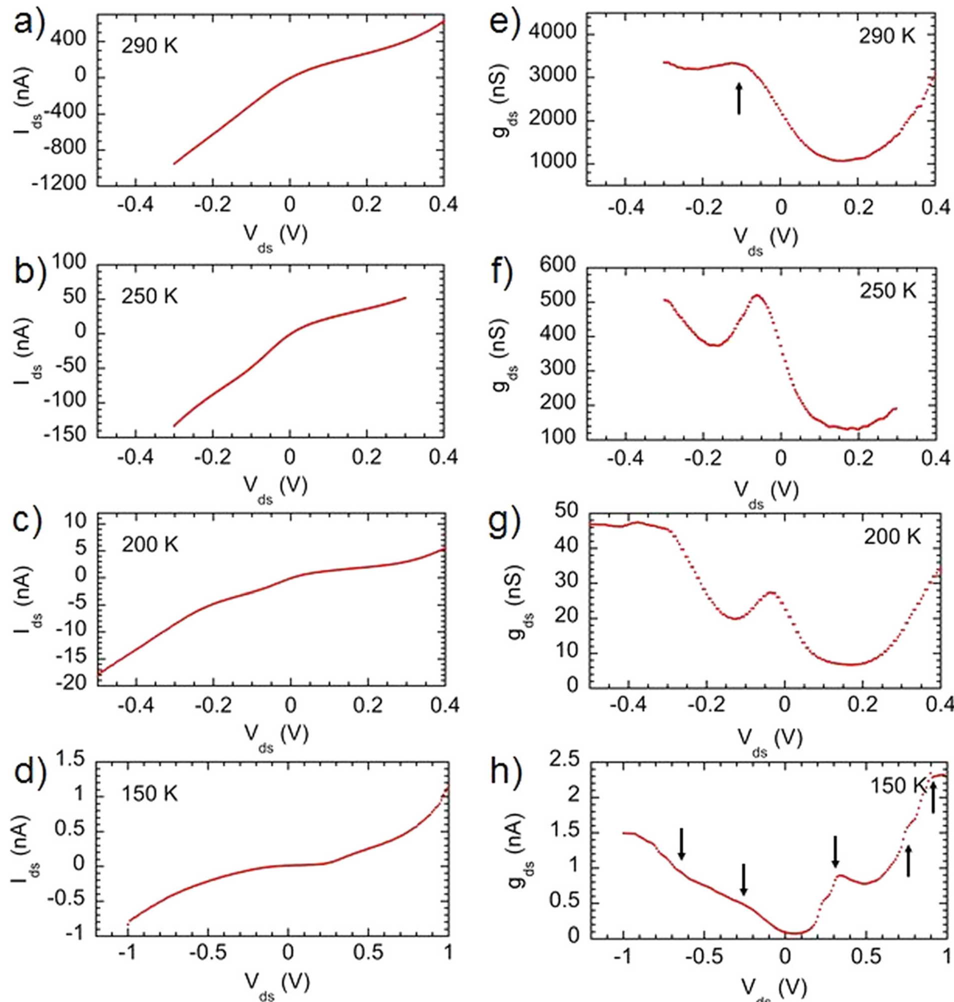

FIG. 10. (Color online) Electrical characteristics of a 30 nm wide point-contact SET. (a)–(d) show the I_{ds}–V_{ds} characteristics, and (e)–(h) show the g_{ds}–V_{ds} characteristics, from 290 to 150 K. Current steps/conductance oscillations occur at the points indicated by arrows in the 150 K plot, (h).

negative V_{ds}, creating a current staircase. The observation of multiple peaks in (h) may be attributed to single-electron charging of an island lying within the point-contact. Within this picture, by using the position of the first step, $V_t \sim 0.34$ eV, and $E_c = e2/2C = eV_t/2$, we find $Ec = 0.17$ eV, and $C = 0.47$ aF. These values are small enough for RT observation of single-electron effects and suggest that the g_{ds} peak at 290 K in (e) may indicate of RT single-electron charging.

V. SUMMARY

Cost-effective fabrication of single nanodigit devices could be the shortest economic way to get access to diverse single electron devices. SETs are playing an important role for new electronic devices, and the capabilities of SPL and RIE at cryogenic temperature become a way to overcome the fundamental size limitations without high capital investment. The use of SETs as a sensor of Q-bits in quantum computing becomes more realistic.

Using active cantilevers, direct patterning on calixarene is demonstrated through the employment of a direct, development-free techniques due to tip emitted low energy (<50 eV) electrons. The scanning probes are not only applied for lithography, but also for imaging and probing of the surface before and immediately after scanning probe patterning. They are able to routinely obtain atomic resolution at a low thermal noise floor. The active cantilever technology offers a compact, integrated system, suitable for the integration into a table-top scanning probe lithography tool. The simplicity, controllability, and reproducibility of these methods are enabling a new perspective to be opened for the easy fabrication of beyond CMOS devices, with the added attraction of not requiring a high capital investment. The technology chain presented here will help facilitate the routine manufacturing of single-electron devices.

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