.

Charge injection and trapping in TiO_2 nanoparticles decorated silicon nanowires arrays

Kamran Rasool , M. A. Rafiq, Mushtaq Ahmad, Z. Imran, S. S. Batool, Adnan Nazir, Z. A. K. Durrani, and M. M. Hasan

Citation: Appl. Phys. Lett. **106**, 073101 (2015); doi: 10.1063/1.4908569

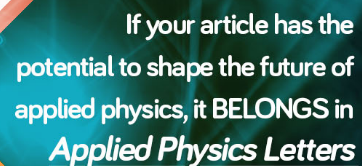
View online: http://dx.doi.org/10.1063/1.4908569

View Table of Contents: http://aip.scitation.org/toc/apl/106/7

Published by the American Institute of Physics

Articles you may be interested in

TiO_2 nanoparticles and silicon nanowires hybrid device: Role of interface on electrical, dielectric, and photodetection properties
Applied Physics Letters **101**, 253104 (2012); 10.1063/1.4772068



AIP | Applied Physics Letters

APPLIED PHYSICS LETTERS **106**, 073101 (2015)

Charge injection and trapping in TiO_2 nanoparticles decorated silicon nanowires arrays

Kamran Rasool,[1,2,3,a)] M. A. Rafiq,[1] Mushtaq Ahmad,[2] Z. Imran,[2] S. S. Batool,[2]
Adnan Nazir,[2] Z. A. K. Durrani,[3] and M. M. Hasan[1]

[1]*Micro and Nano Devices Group, Department of Metallurgy and Materials Engineering, Pakistan Institute of Engineering and Applied Sciences (PIEAS), P. O. Nilore, Islamabad 4650 Pakistan*
[2]*Department of Physics, COMSATS Institute of Information Technology, Park Road, Chak Shahzad, Islamabad 44000, Pakistan*
[3]*Department of Electrical and Electronic Engineering, Imperial College London, South Kensington Campus, London SW7 2AZ, United Kingdom*

(Received 11 September 2014; accepted 6 February 2015; published online 18 February 2015)

We investigate carrier transport properties of silicon nanowire (SiNW) arrays decorated with TiO_2 nanoparticles (NPs). Ohmic conduction was dominant at lower voltages and space charge limited current with and without traps was observed at higher voltages. Mott's 3D variable range hoping mechanism was found to be dominant at lower temperatures. The minimum hopping distance (R_{min}) for *n* and *p*-SiNWs/TiO_2 NPs devices was 1.5 nm and 0.68 nm, respectively, at 77 K. The decrease in the value of R_{min} can be attributed to higher carrier mobility in *p*-SiNWs/TiO_2 NPs than that of *n*-SiNWs/TiO_2 NPs hybrid device. © *2015 AIP Publishing LLC*.
[http://dx.doi.org/10.1063/1.4908569]

Silicon nanostructures have gained great attention in fabrication of future electronic devices such as solar cells, memory devices, photodetectors, thermoelectric devices, and biological applications.[1–4] Silicon nanowires (SiNWs) are efficient for various applications due to their superior electrical properties.[5] Surface dominated transport[6] is important in nanostructures for various device applications.[7–10] Surface passivation of nanostructures[11] by different organic and inorganic materials has been reported to tailor the sensing, optical, electrical, photodetection, and thermoelectric properties.[7,12–16] Properties of SiNWs are highly dependent on density of surface states and doping level.[17]

Oxide semiconductors are promising for many applications.[18] TiO_2 is one of the important oxide semiconductors and is proved to be suitable for photocatalytic, optical, and sensing applications.[19,20] Hybrid SiNWs and TiO_2 nanoparticles (NPs) have shown enhanced electrical and photodetection properties.[12] Other nanoparticles decorated nanostructures have also been investigated to improve electrical, dielectric, thermoelectric, and photodetection properties.[12,16,21–23]

Here, we investigate the effect of decoration of SiNW arrays with TiO_2 NPs on transport properties. As the surface of TiO_2 NPs is hydrophilic in nature, the enhancement in hydrophilic nature of SiNWs was observed due to the presence of TiO_2 NPs on SiNWs. This resulted in the enhancement of electrical current in *p*-SiNWs and reduction of current in *n*-SiNWs. Space charge limited current conduction (SCLC) is dominant conduction mechanism in both devices at intermediate voltages followed by trap free SCLC. Mott's 3D variable range hopping (VRH) mechanism was observed at lower temperatures in both devices. This type of detailed electrical transport properties and comparison between *n* and *p*-SiNWs decorated with TiO_2 NPs has rarely been investigated before.

Two separate devices "*p*-SiNWs/TiO_2 NPs" and "*n*-SiNWs/TiO_2 NPs" were prepared using *p* and *n*-type silicon (100) substrates (resistivity of 1–10 Ω cm), respectively, under similar fabrication conditions. Silicon nanowires were synthesized by metal assisted electroless chemical etching (MACE) technique.[15] Solutions of HF and $AgNO_3$ were used to form Ag particles on the silicon substrate by galvanic exchange process. H_2O_2 and HF solutions were then used for etching. Length of NWs depends upon the time of etching.[24] Synthesis of TiO_2 NPs was performed by co-precipitation method. Solution containing $TiCl_4$ (99.99%) and HCl (0.5M) was mixed under vigorous stirring. Solution of Na_2CO_3 (2.1M) in deionized (DI) water was added drop wise under continuous stirring. When the pH of solution was around ∼8, large amount of white precipitates of TiO_2 NPs were formed.[12] These precipitates were then washed with DI water several times.

For device fabrication, 200 μl DI water containing TiO_2 NPs was spun onto already grown vertical SiNW arrays in multiple spinning steps. Spinning speed was 1000 rpm for 30 s during each step. After each spinning step, sample was dried in air at 50 °C for 20 min. Finally, 10 nm Cr followed by 300 nm Au was sputtered to form metal contacts on both sides. No further heat treatment was performed. In both devices, the dimensions of prepared structures and overall device were identical, i.e., planar area (of devices), length, and diameter of SiNWs were 0.85 cm × 0.85 cm, 40 μm, and 50–300 nm, respectively.

Figure 1(a) shows the cross-sectional scanning electron microscope (SEM) image of SiNWs prepared by MACE technique. The length and diameter of SiNWs were ∼40 μm and ∼50 nm–300 nm, respectively. Figure 1(b) shows the cross-sectional SEM image of TiO_2 NPs decorated SiNWs. Here, we can clearly see the presence of TiO_2 NPs on the

a)Author to whom correspondence should be addressed. Electronic addresses: kamran.rasool@comsats.edu.pk and interest.phy@gmail.com.

 © 2015 AIP Publishing LLC

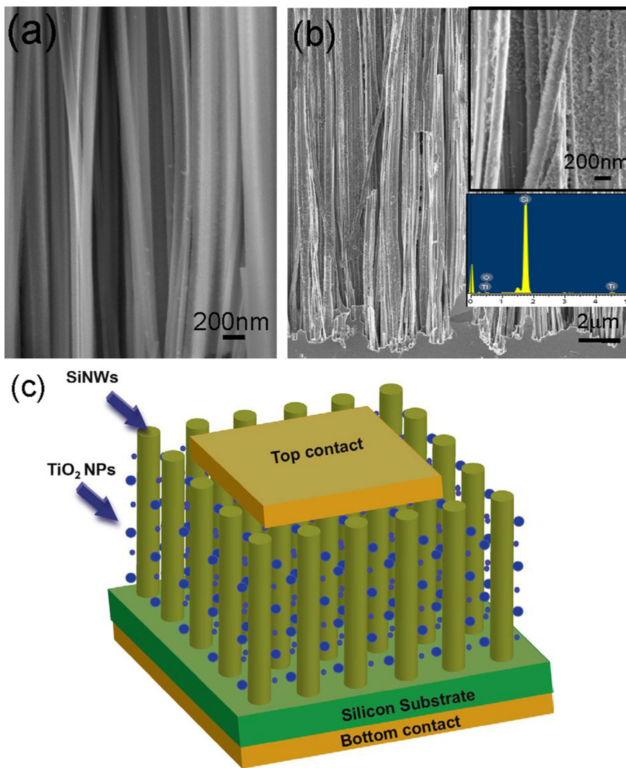


FIG. 1. (a) Cross-sectional SEM image of SiNWs arrays. (b) The Cross-sectional SEM image of SiNWs/TiO_2 NPs hybrid device and inset shows high resolution SEM image along with EDS spectra (similar images were seen for both *n* and *p* type SiNWs. (c) Schematic diagram of final fabricated SiNWs/TiO_2 NPs hybrid device with top and bottom metal contacts.

surface of SiNWs. Inset of Figure 1(b) shows high resolution cross-sectional SEM image of SiNWs/TiO_2 NPs hybrid device. The presence of TiO_2 NPs between SiNW arrays was further confirmed by energy dispersive X-ray (EDS) spectroscopy, also shown in the inset of Figure 1(b). The appeared peaks corresponding to Ti, O, and Si only confirmed the presence of TiO_2 NPs and SiNWs. Figure 1(c) shows the schematic representation of our final fabricated device having SiNWs decorated with TiO_2 NPs and having top and bottom metal contacts.

Temperature dependent current-voltage (*IV*) characteristics were performed using Agilent 4155 parameter analyzer with a probe station from 290 K to 77 K. In this section, we compare the transport properties of *n*-SiNWs/TiO_2 NPs and *p*-SiNWs/TiO_2 NPs hybrid devices. Figures 2(a) and 2(b) show the *IV* characteristics of *n*-SiNWs/TiO_2 NPs device and *p*-SiNWs/TiO_2 NPs device at 290 K and 77 K. At 290 K, *p*-SiNWs/TiO_2 NPs hybrid device shows greater current than that of *n*-SiNWs/TiO_2 NPs hybrid device. At 290 K and 1 V, the values of current density are $2.02 \times 10^3\,A/m^2$ and $42.28\,A/m^2$ for *p*-SiNWs/TiO_2 NPs device and *n*-SiNWs/TiO_2 NPs device, respectively. The *p*-SiNWs/TiO_2 NPs device shows ∼48 times enhancement in current at 290 K. At 77 K, *p*-SiNWs/TiO_2 NPs device shows ∼1.29 times enhancement in current. Therefore, the increase in current is greater at higher temperatures than at lower temperatures.

Figure 2(c) shows the schematic representation of single SiNW decorated with TiO_2 NPs. Here, the change in current upon incorporation of TiO_2 NPs between SiNWs can be explained as follows. Aged SiNWs are hydrophilic in nature. Hydrophilic surface of SiNWs attracts hydrophilic contents (O^-, O_2^-, OH^-, and H_2O) from surroundings. Increase in hydrophilic contents on the surface of SiNWs actually resulted in change in electrical conductivity. Therefore, surface of SiNWs is highly sensitive to surrounding environment. The addition of organic and inorganic materials has already been used to tailor electrical and optical properties of silicon nanostructures.[6,12,25,26] TiO_2 NPs are found in three phases, anatase, rutile, and brookite. Anatase phase is formed at low temperature ∼450 °C and rutile phase is formed at ∼650 °C. Room temperature synthesis of TiO_2 NPs in this study yielded anatase phase of TiO_2 NPs.[27,28] Usually, anatase phase is more hydrophilic in nature than rutile phase.[29] The TiO_2 NPs hydrophilic nature also enhances the

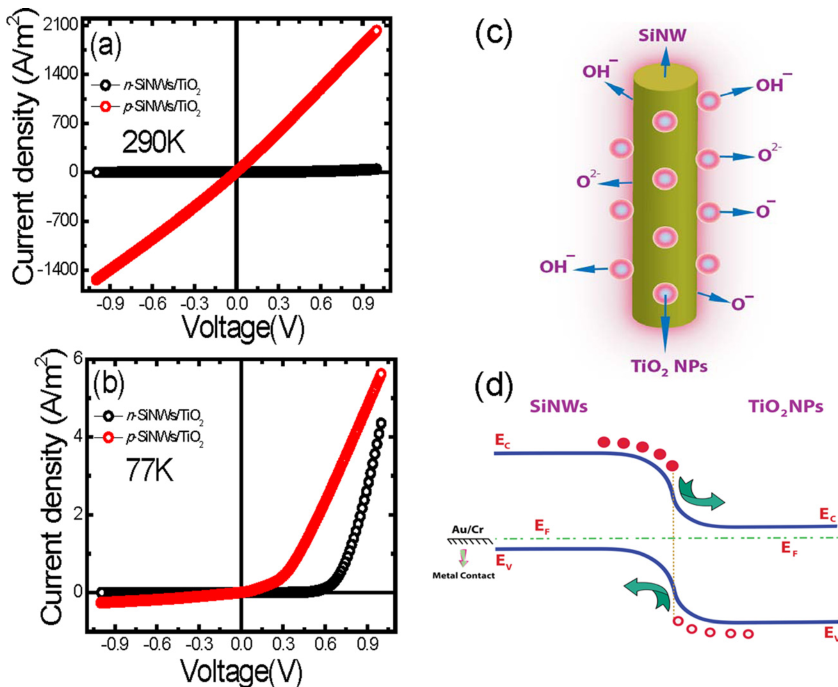


FIG. 2. Comparison of *IV* characteristics of *p*-SiNWs/TiO_2 NPs and *n*-SiNWs/TiO_2 NPs hybrid device at (a) 290 K and (b) 77 K. (c) Schematic diagram of SiNW decorated with TiO_2 NPs. (d) Schematic representation of band bending at SiNWs/TiO_2 NPs interface.

possibility of sticking of TiO_2 NPs on surface of the SiNWs. Hence with the presence of TiO_2 NPs on the surface of SiNWs, the hydrophilicity of SiNWs increases. Figure 2(d) shows the schematic representation of band bending at SiNWs/TiO_2 NPs interface. Due to the presence of TiO_2 NPs on the surface of SiNWs; an electron from the SiNW is utilized by the TiO_2 NP to form chemical bond with SiNW. Therefore, due to formation of acceptor like states at SiNW surface in presence of TiO_2 NPs, the current in *p*-SiNWs increases[30] and decreases in case of *n*-SiNWs. With the addition of TiO_2 NPs on the surface of SiNWs, hydrophobic bonds left on the surface of SiNWs may convert to hydrophilic.

Figure 3(a) shows the temperature dependent *IV* characteristics of *p*-SiNWs/TiO_2 NPs hybrid device from 290 K to 77 K. Figure 3(b) shows the *ln-ln* plot for exploring conduction mechanism occurring in our system. At higher temperatures (290 K–270 K), ohmic like conduction is dominant in the entire voltage range. This may be due to comparable work function between *p*-SiNWs and metals used for contact (Cr and Au). At lower voltages, *p*-SiNWs/TiO_2 NPs device shows ohmic like conduction in all temperature range (290 K–77 K). But at intermediate voltage, the value of slope ranges from ∼1.5 to 1.9 for 230 K–110 K. This region is referred to as charge injection region[31,32] which is characteristics of onset of SCLC conduction mechanism. At lower temperatures (110 K–77 K), the value of slope is greater than 2 and shows typical SCLC behavior with traps.

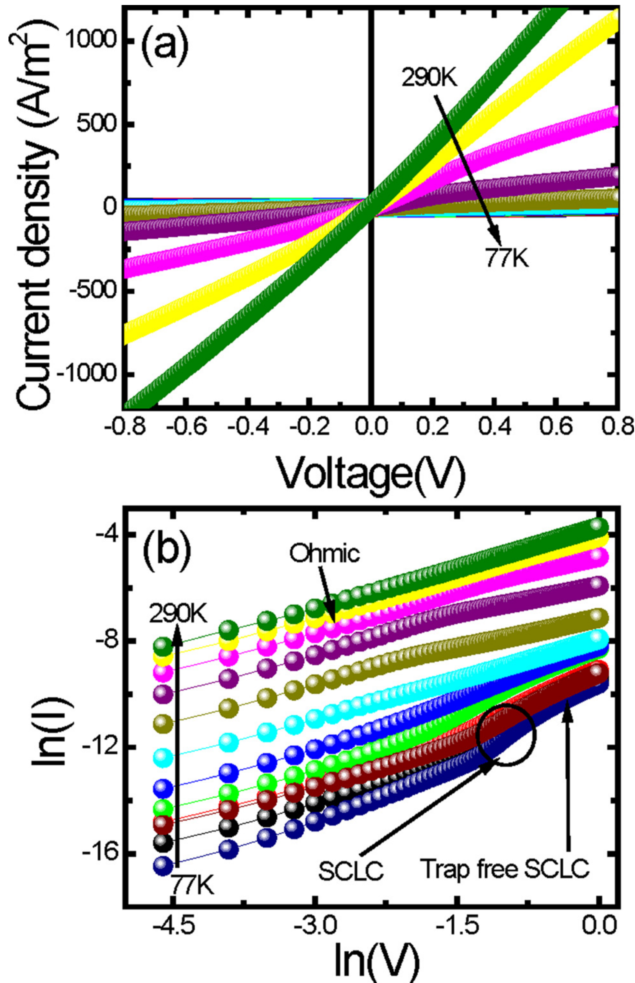


FIG. 3. (a) Temperature dependent *IV* characteristics of *p*-SiNWs/TiO_2 NPs hybrid device. (b) The *ln-ln* plot to explain conduction mechanism in all temperature range (290 K–77 K).

The *IV* characteristics are strongly dependent on various physical parameters (material, electrodes type, doping type, trap concentration, applied field, geometry, temperature, etc.). Injection of electrons and holes is usually controlled by potential barrier between interfaces and work function difference between metal electrodes and material.[33] At lower voltages, Ohm's law is dominant because injected carriers are negligible as compared to thermally generated free carriers. Under applied bias, concentration of free charge carriers can be increased. The space charge effect is attributed to the dissimilarity in concentration of injected carriers and the thermal equilibrium value.[34] Hence, injected carriers produce electric field and the current produced due to the presence of a space-charge effect is called the SCLC as indicated by the value of slope greater than 2.

Due to surface passivation with TiO_2 NPs on SiNWs, surface defects and localized traps are created. The presence of these defects can significantly hinder the passage of injected current. This observation is more prominent at lower temperatures where the captured electrons are stable as shown in our case at lower temperature (77 K).[35] When sufficient input voltage is applied, these traps are filled and get enough energy to leave the traps, known as trap free SCLC.[34]

Figure 4(a) shows temperature dependent *IV* characteristics of *n*-SiNWs/TiO_2 NPs device from 290 K to 77 K. *IV* characteristics plotted on *ln-ln* scale are shown in Figure 4(b). Ohmic like conduction is dominant at lower voltages at all temperatures for this device as well. But at intermediate voltages, SCLC is observed with slope ranging from ∼3 to 9. The higher values of slopes in comparison to the previous device show less conducting semiconductor or the presence of more traps. The difference in slopes can also be due to greater work function difference between *n*-SiNWs and metals used for electrical contacts. Since the presence of TiO_2 NPs on the surface of SiNWs creates acceptor like states (traps for electrons), therefore SiNWs become more resistive in this case and show strong SCLC. With the increase in voltage, these traps may be filled and trap free SCLC is observed.[36]

In case of SCLC with exponential distribution of traps, the current density obeys power law dependence $J \sim V^m$ given by[37]

$$J = q^{1-l}\mu N_{DOS}\left(\frac{2l+1}{l+1}\right)^{l+1}\left(\frac{l}{l+1}\frac{\varepsilon_s\varepsilon_0}{H_t}\right)^{l}\frac{V^{l+1}}{d^{2l+1}}. \quad (1)$$

Here $m = l+1$, H_t is density of traps, ε_s is dielectric constant, ε_0 is the permittivity of free space, μ is the carrier mobility, N_{DOS} is the density of states in the relevant band, and d is thickness. The *IV* curves are therefore straight lines with slope m on *ln-ln* plot. Generally, m increases with decrease in temperature. When *IV* curves are extrapolated, the curves tend to meet at single point as shown in Figure 4(c). The meeting point is referred to as cross over voltage V_c and is given by

$$V_c = \frac{qH_t d^2}{2\varepsilon_s\varepsilon_0}. \quad (2)$$

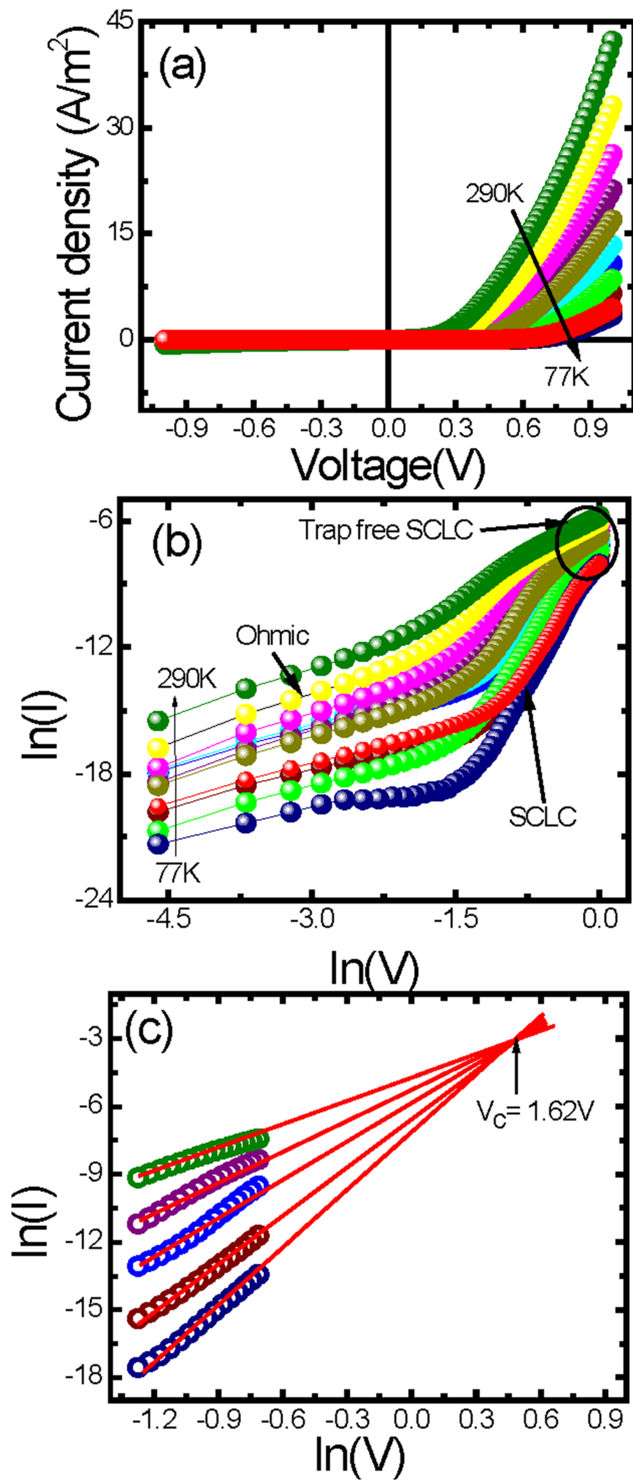


FIG. 4. (a) Temperature dependent *IV* characteristics of *n*-SiNWs/TiO_2 NPs hybrid device. (b) The *ln-ln* plot to explain conduction mechanism in all temperature range (290 K–77 K). (c) Power law fits to the data from 290 K to 77 K. The fits meet at cross over voltage $V_c = 1.62$ eV.

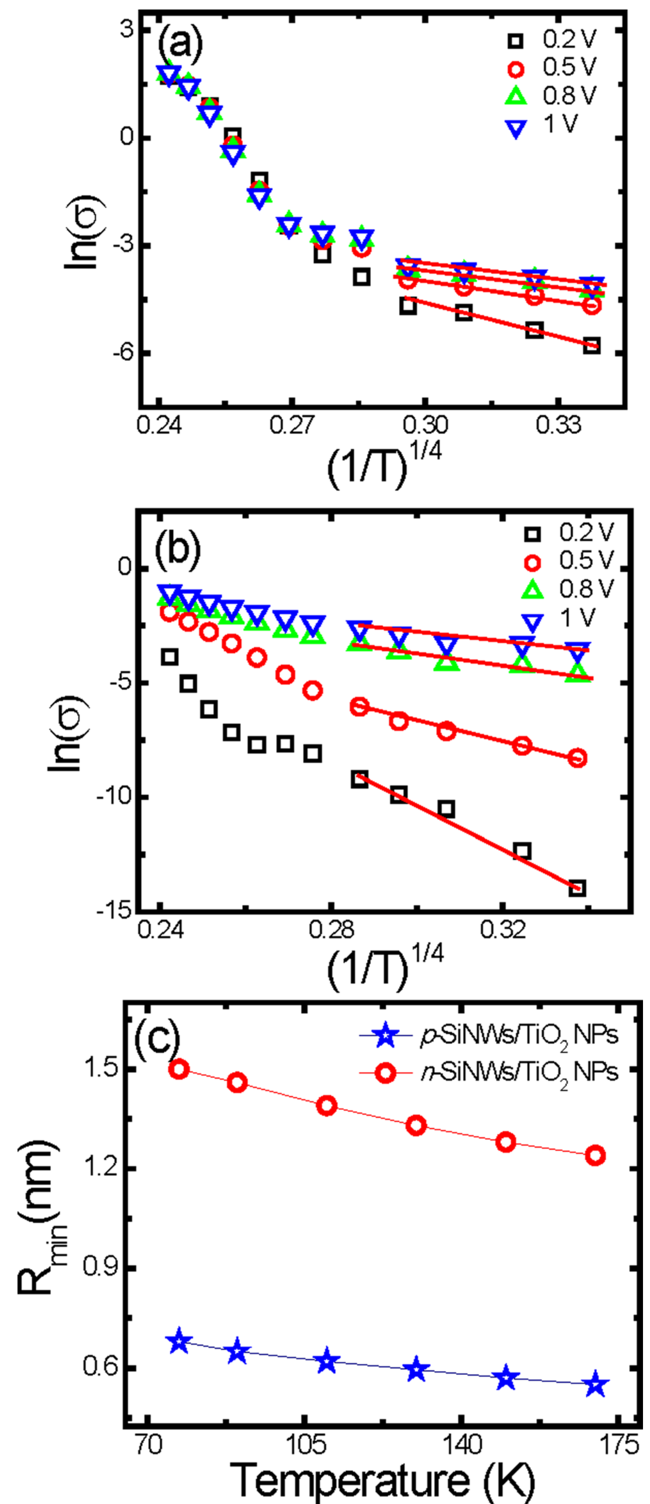


FIG. 5. (a) Plot of conductivity against inverse of temperature. Solid line shows best fit to 3D VRH mechanism for (a) *p*-SiNWs/TiO_2 NPs (b) *n*-SiNWs/TiO_2 NPs hybrid device in the temperature range (170 K–77 K). (c) Minimum hopping distance R_{min} for both *n* and *p*-SiNWs/TiO_2 NPs hybrid device in the temperature range (170 K–77 K).

The calculated value of V_c is 1.62 V as seen from Figure 4(c). Using this value, Eq. (2) gives the value of H_t to be $1.28 \times 10^{12}\,\text{cm}^{-3}$.

Conduction in nanowires at lower temperatures has been found to obey hopping mechanism[38] and depends on temperature and applied field. This is because carrier jumps to higher energy localized states facilitated by phonons or applied electric field.[39] As shown in Figures 5(a) and 5(b) below ~170 K, the data obey Mott's 3D VRH given by[38]

$$\sigma = \sigma_0 \exp\left[-\left(\frac{T_0}{T}\right)^{1/4}\right]. \tag{3}$$

Here, T_0 is the characteristic temperature and depends on density of states ($N(E_F)$) and localization length (ξ) and is given by

$$T_0 = \frac{24}{\pi k_b N(E_F)\zeta^3}. \quad (4)$$

In case of VRH conduction, a material requires many empty states and traps for hopping as indicated above. The presence of traps is already confirmed by trap limited SCLC transport in both of hybrid SiNWs devices.[40] The values of T_0 were obtained from slope of linear portion in Figures 5(a) and 5(b) and ξ are supposed to be $\sim$0.3 nm (Ref. 38) for silicon. The values of $N(E_F)$ are $8.39 \times 10^{21}\,\mathrm{eV^{-1}cm^{-3}}$ and $1.05 \times 10^{21}\,\mathrm{eV^{-1}cm^{-3}}$ for p-SiNWs/TiO_2 NPs device and n-SiNWs/TiO_2 NPs device, respectively, calculated at 0.5 V. The minimum hopping distance (R_{min}) can be calculated from the following equation:[34]

$$R_{\min} = \left[\frac{\zeta}{8\pi N(E_F)k_B T}\right]^{1/4}. \quad (5)$$

The values of R_{min} as a function of temperature are shown in Figure 5(c) for p-SiNWs/TiO_2 NPs device and n-SiNWs/TiO_2 NPs device. The values of R_{min} decrease in both devices with increasing temperature as carriers require more energy for hopping at lower temperature. As discussed earlier, our p-SiNWs/TiO_2 NPs show higher current than n-SiNWs/TiO_2 NPs. Hence, value of R_{min} for p-SiNWs/TiO_2 NPs is smaller than that of n-SiNWs/TiO_2 NPs. This decrease in the value of R_{min} shows that more energy is required for hopping electron from one state to another state in n-SiNWs/TiO_2 NPs and hence effective barrier for flow of current increases.

In conclusion, we have presented the transport properties of n and p-SiNWs/TiO_2 NPs hybrid devices. In comparison to n-SiNWs/TiO_2 NPs device, p-SiNWs/TiO_2 NPs device shows higher electrical current. Both devices show ohmic behavior at lower voltages but at intermediate voltages SCLC behavior is dominant. Mott's 3D VRH model fits the data at lower temperatures in both devices. The extracted R_{min} value is lower for p-SiNWs/TiO_2 NPs device than that of n-SiNWs/TiO_2 NPs device. This decrease in the value of R_{min} can be attributed to higher carrier mobility in p-SiNWs/TiO_2 NPs hybrid device and effective barrier for flow of current decreases.

We acknowledge the financial support of the Higher Education Commission (HEC), Pakistan. We also thank C. B. Li for useful discussion.

[1]B. Tian, X. Zheng, T. J. Kempa, Y. Fang, N. Yu, G. Yu, J. Huang, and C. M. Lieber, Nature **449**(7164), 885–889 (2007).

[2]A. I. Hochbaum, R. Chen, R. D. Delgado, W. Liang, E. C. Garnett, M. Najarian, A. Majumdar, and P. Yang, Nature **451**(7175), 163–167 (2008).

[3]H. McConnell, J. Owicki, J. Parce, D. Miller, G. Baxter, H. Wada, and S. Pitchford, Science **257**(5078), 1906–1912 (1992).

[4]A. I. Kingon, J.-P. Maria, and S. K. Streiffer, Nature **406**(6799), 1032–1038 (2000).

[5]F. Sacconi, M. P. Persson, M. Povolotskyi, L. Latessa, A. Pecchia, A. Gagliardi, A. Balint, T. Fraunheim, and A. Di Carlo, J. Comput. Electron. **6**(1–3), 329–333 (2007).

[6]S.-l. Wu, L. Wen, G.-a. Cheng, R.-t. Zheng, and X.-l. Wu, ACS Appl. Mater. Interfaces **5**(11), 4769–4776 (2013).

[7]Y. Cui, X. Duan, J. Hu, and C. M. Lieber, J. Phys. Chem. B **104**(22), 5213–5216 (2000).

[8]V. Sivakov, G. Andrä, A. Gawlik, A. Berger, J. Plentz, F. Falk, and S. Christiansen, Nano Lett. **9**(4), 1549–1554 (2009).

[9]M. V. Fernández-Serra, C. Adessi, and X. Blase, Nano Lett. **6**(12), 2674–2678 (2006).

[10]K.-Q. Peng, X. Wang, L. Li, Y. Hu, and S.-T. Lee, Nano Today **8**(1), 75–97 (2013).

[11]A. Kumatani, Y. Li, P. Darmawan, T. Minari, and K. Tsukagoshi, Sci. Rep. **3**, 1026 (2013).

[12]K. Rasool, M. Rafiq, M. Ahmad, Z. Imran, and M. Hasan, Appl. Phys. Lett. **101**(25), 253104 (2012).

[13]K.-Q. Peng, X. Wang, X.-L. Wu, and S.-T. Lee, Nano Lett. **9**(11), 3704–3709 (2009).

[14]H.-J. Kim, H. B. Bae, Y. Park, and S. H. Choi, RSC Advances **2**(33), 12670–12674 (2012).

[15]K. Rasool, M. Rafiq, C. Li, E. Krali, Z. Durrani, and M. Hasan, Appl. Phys. Lett. **101**(2), 023114 (2012).

[16]R. Chen, D. Li, H. Hu, Y. Zhao, Y. Wang, N. Wong, S. Wang, Y. Zhang, J. Hu, and Z. Shen, J. Phys. Chem. C **116**(7), 4416–4422 (2012).

[17]M. Y. Bashouti, M. Pietsch, G. Brönstrup, V. Sivakov, J. Ristein, and S. Christiansen, Prog. Photovoltaics **22**(10), 1050–1061 (2014).

[18]E. H. Nicollian and J. R. Brews, *MOS (Metal Oxide Semiconductor) Physics and Technology* (Wiley-Interscience, New York, 1982), Vol. 1, p. 920.

[19]C.-y. Wang, D. W. Bahnemann, and J. K. Dohrmann, Chem. Commun. **2000**(16), 1539–1540.

[20]J.-A. He, R. Mosurkal, L. A. Samuelson, L. Li, and J. Kumar, Langmuir **19**(6), 2169–2174 (2003).

[21]M. Ahmad, K. Rasool, M. Rafiq, and M. Hasan, Appl. Phys. Lett. **101**(22), 223103 (2012).

[22]M. Ahmad, K. Rasool, M. Rafiq, M. Hasan, C. Li, and Z. Durrani, Physica E **45**, 201–206 (2012).

[23]S. Wang, H. Li, R. Lu, G. Zheng, and X. Tang, Nanotechnology **24**(28), 285702 (2013).

[24]Z. Huang, N. Geyer, P. Werner, J. de Boor, and U. Gösele, Adv. Mater. **23**(2), 285–308 (2011).

[25]K. Fobelets, P. Ding, N. Mohseni Kiasari, and Z. A. K. Durrani, IEEE Trans. Nanotechnol. **11**(4), 661–665 (2012).

[26]D. Shao, M. Yu, J. Lian, and S. Sawyer, Appl. Phys. Lett. **102**(2), 021107 (2013).

[27]A. Di Paola, G. Cufalo, M. Addamo, M. Bellardita, R. Campostrini, M. Ischia, R. Ceccato, and L. Palmisano, Colloids Surf., A **317**(1–3), 366–376 (2008).

[28]C. Byun, J. W. Jang, I. T. Kim, K. S. Hong, and B. W. Lee, Mater. Res. Bull. **32**(4), 431–440 (1997).

[29]V. Bolis, C. Busco, M. Ciarletta, C. Distasi, J. Erriquez, I. Fenoglio, S. Livraghi, and S. Morel, J. Colloid Interface Sci. **369**(1), 28–39 (2012).

[30]K. Rasool, M. A. Rafiq, M. Ahmad, Z. Imran, and M. M. Hasan, J. Appl. Phys. **113**(19), 193703 (2013).

[31]J. Kolk and E. L. Heasell, Solid-State Electron. **23**(3), 223–228 (1980).

[32]J. Alvarez, I. Ngo, M.-E. Gueunier-Farret, J.-P. Kleider, L. Yu, P. R. Cabarrocas, S. Perraud, E. Rouvière, C. Celle, and C. Mouchet, Nanoscale Res. Lett. **6**(1), 110 (2011).

[33]R. Rurali, Rev. Mod. Phys. **82**(1), 427–449 (2010).

[34]M. A. Lampert, Phys. Rev. **103**(6), 1648–1656 (1956).

[35]H. A. Al Attar and A. P. Monkman, Adv. Funct. Mater. **16**(17), 2231–2242 (2006).

[36]J. H. Schön, C. Kloc, and B. Batlogg, Phys. Rev. B **63**(24), 245201 (2001).

[37]M. Rafiq, Y. Tsuchiya, H. Mizuta, S. Oda, S. Uno, Z. Durrani, and W. Milne, Appl. Phys. Lett. **87**(18), 182101 (2005).

[38]L. Pichon, E. Jacques, R. Rogel, A. C. Salaun, and F. Demami, Semicond. Sci. Technol. **28**(2), 025002 (2013).

[39]M. A. Rafiq, Z. A. K. Durrani, H. Mizuta, M. M. Hassan, and S. Oda, J. Appl. Phys. **104**(12), 123710 (2008).

[40]B. T. Phan, T. Choi, A. Romanenko, and J. Lee, Solid-State Electron. **75**, 43–47 (2012).