Fabrication of RF MEMS Components on CMOS Circuits

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Abstract — **Recently deep submicron and SiGe (silicon-germanium) bipolar CMOS technologies have enhanced the performance of Si-based radio frequency (RF) integrated circuits up to microwave frequencies. The integration of RF MEMS components, such as inductors and capacitors, could further improve the performance of key RF circuit blocks such as voltage controlled oscillators (VCO), low-noise amplifiers, filters, mixers, and power amplifiers. We have developed a process to integrate RF MEMS inductors with standard commercial CMOS dies. The purpose of this work is to present the integration of MEMS inductors with VCOs fabricated in a 0.18 μm standard CMOS technology.**

I. INTRODUCTION

WIRELESS systems today typically require a number of off-chip electronic devices in addition to the integrated circuits that carry most of the circuitry. External LC (inductor-capacitor) tanks and quartz reference oscillators are examples of common elements in transceiver architectures that are implemented off-chip. However, with the ongoing need for further miniaturization and higher performance, the replacement of these off-chip parts by monolithically integrated devices based on micromachining and microelectromechanical systems (MEMS) technology represents an increasingly attractive prospect, and there are many efforts in this direction [1-3]. Integrated MEMS components, such as high-Q inductors, have the potential to increase significantly the performance of key RF (radio-frequency) circuit blocks such as voltage controlled oscillators (VCO), low-noise amplifiers, filters, mixers, and power amplifiers. The performance of these blocks at high frequency is limited by resistive and dielectric losses, resonant effects, dispersion, and parasitic radiation of the inductors. Key performance parameters for integrated reactive components are the quality factor (Q) and resonant frequency. Higher Q components help minimize RF power loss, reduce noise, and lower dc power consumption of RF integrated circuits.

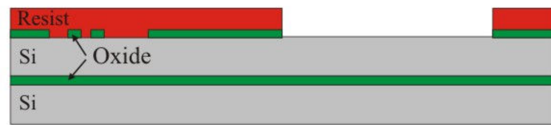
We have developed a process to integrate RF MEMS inductors with standard commercial CMOS dies. In this paper we demonstrate the integration of MEMS inductors with VCOs fabricated in a 0.18 μm standard CMOS technology [4]. The dies are embedded in device-layer cavities defined in a 100 mm-dia. BSOI (Bonded Silicon On Insulator) carrier wafer by deep reactive ion etching (DRIE). The device layer thickness is chosen to match the nominal die thickness, and the cavity depth is finely adjusted by thinning the device layer so that top surface of each die lies within ±2 um of the surface of the carrier. Once the dies have been placed, a layer of photoresist is spin-coated over the carrier [5] to fix the dies in place and planarize the top surface. Windows are opened in this layer to allow electrical and mechanical contact to the underlying dies carrying VCO circuitry. In this way, fabrication of MEMS inductors by patterned electroplating can be achieved on pre fabricated VCOs as on a bare silicon wafer. A self-assembly MEMS method for the fabrication of inductors in the vertical orientation has been used [6]. Self-assembled inductors of this type have higher Q [7] which is expected to result in lower VCO phase noise. This technology has the advantage of providing monolithic integration of state-of-the-art RF MEMS inductors with any standard CMOS technology without being constrained to particular silicon or compound-semiconductor platforms and also irrespective of wafer size.

II. DIE CARRIER PROCESS

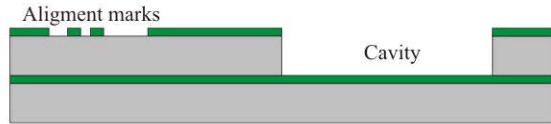
Use of a die carrier allows simultaneous processing of multiple dies, and better compatibility with process equipment and wafer handling techniques. It also has the potential to embed different types of CMOS dies, and is compatible with any wafer size. The process in this case used 100 mm-diameter BSOI starting wafers, comprising 300 μm-thick device layers and 380 μm-thick handle layers, separated by 1 μm of buried SiO_2. The key steps in the die carrier process are illustrated in Figure 1.

Firstly, alignment marks are formed, either in a thermally grown oxide layer on the top surface of the BSOI wafer, or by shallow etching of the silicon. Deep reactive ion etching (DRIE) with an STS Multiplex ICP etcher is then used to form cavities in the device layer. By adjusting the passivation and etching cycles, the DRIE process has been optimized to produce near-vertical sidewalls when stopping on the buried oxide layer. The cavity sizes are closely matched to the die dimensions to ensure placement of the dies to within ±15 μm.

Following the cavity DRIE, the dies are placed, and a thin layer of photoresist is deposited by spin-coating to fix them in place and planarize the top surface.

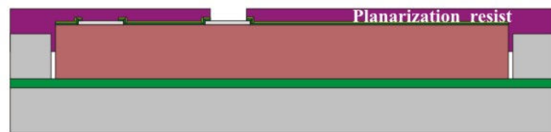


(a) Pattern oxide; spin and pattern resist

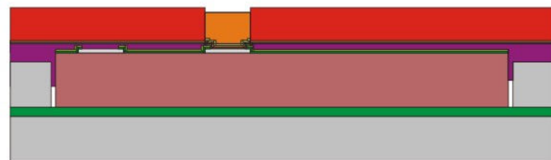


(b) Si DRIE to form cavities

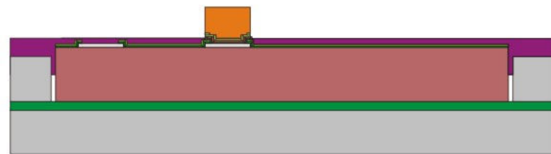
(c) Place dies



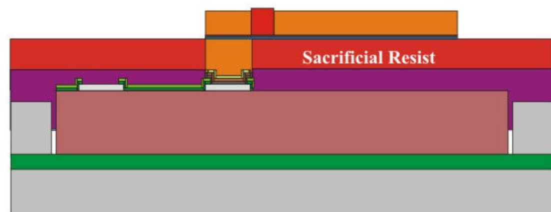
(d) Spin & pattern planarization resist



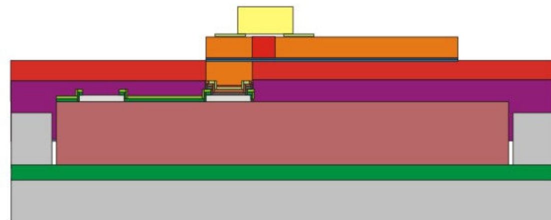
(e) Electroplate gold interface pads



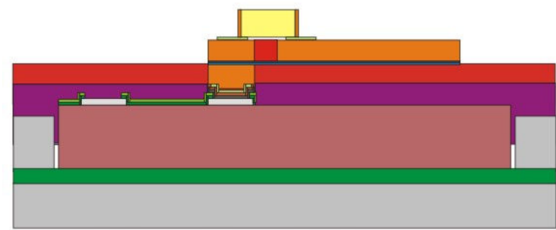
(f) Strip mould; etch seed layer



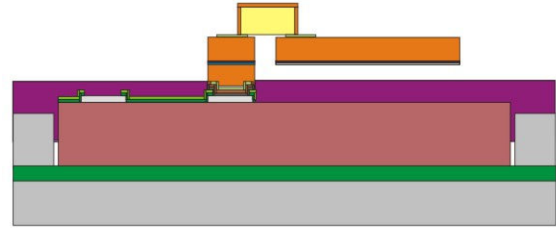
(g) Deposit sacrificial layer; electroplate inductors



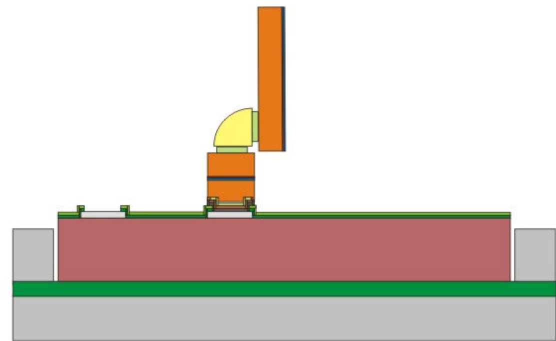
(h) Deposit hinge



(i) Overcoat hinges with gold



(j) Release structures



(k) Reflow hinges to self-assemble inductors

Fig. 1. Fabrication process flow for inductors on CMOS dies.

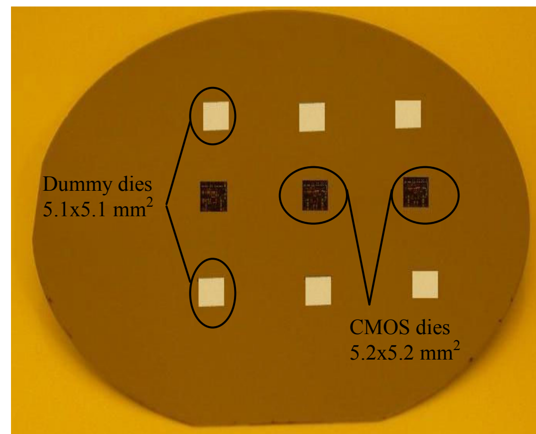


Fig. 2. BSOI carrier with embedded CMOS dies.

In this research the UMC foundry service was used for CMOS die fabrication. A 0.18 micron silicided CMOS process was chosen, with up to 6 metal layers, 1 poly layer, and a high resistance layer. Stacked contacts are supported, as are MIM capacitors (metal 5 to metal 6, 3 pF total capacitance, 55 x 55 μm^2 area). The process is for 1.8 volt bias applications, although 2.5 volt thick transistors are also available. The dies fabricated were 5200 x 5200 x 284 μm^3 in size, and carried a number of different voltage controlled oscillators for operation up to 5 GHz [4]. These were designed specifically for operation

with our self-assembled MEMS inductors. Figure 3 shows low- and high-magnification images of CMOS dies containing VCO circuits.

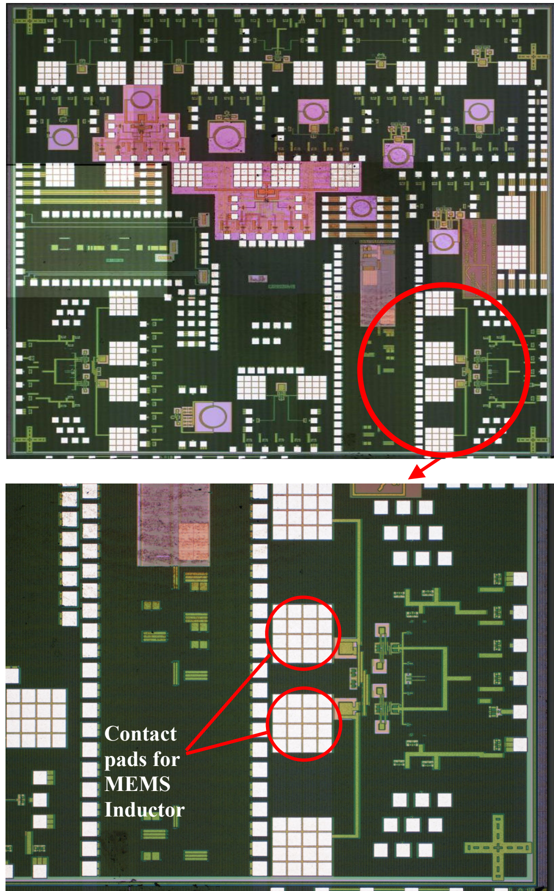


Fig. 3. CMOS die with VCO circuit.

In steps e and f of the process flow in Figure 1, metal pads are deposited on the CMOS which will form the mechanical and electrical interface to the MEMS structures. In this work gold was chosen as the material for these interface pads because the aim was to realize low-loss RF MEMS components over CMOS. The mask used to define the mould was the same as that used to open the windows in the planarization layer, so that the plated pads were formed over the CMOS contact pads. Fig 4 shows a CMOS die following these process steps.

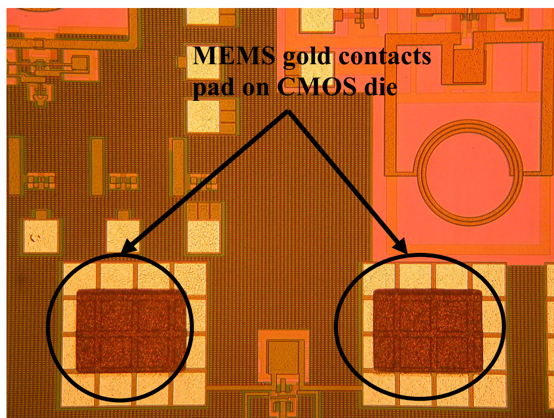


Fig. 4. Gold pads on CMOS die.

III. INTEGRATION OF SELF-ASSEMBLED INDUCTORS

Self-assembled inductors were fabricated using process steps g to k in Figure 1. First, a sacrificial resist layer was deposited and patterned using the interface pad mask. The resist height was chosen to be around 0.5 µm greater than that of the gold pads. A sputtered Ti/Cu (titanium/copper) seed layer was then deposited, and the inductors formed by gold electroplating into a mould formed in Shipley S1828 photoresist (step g). Fig 5 shows a 4 µm-thick gold electroplated inductor on a CMOS die.

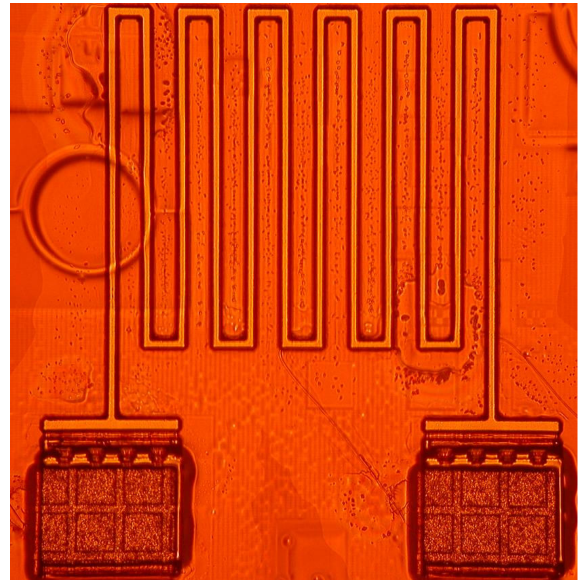


Fig. 5. MEMS inductor prior to deposition of hinge.

The meltable hinges required for the self-assembly process were formed by electrodeposition of pure tin into a new photoresist mould (step h). Prior to this step a thin nickel barrier layer or “pedestal” was deposited in the hinge region to ensure lateral containment of the Sn during reflow, and to prevent interdiffusion between the Sn and the underlying gold. The Ti/Cu seed layer was also removed from the hinge region at this stage. After plating of the hinges, a 200 nm-thick gold layer was deposited over them to protect the tin from oxidation before and during reflow (step i). Figure 6 shows low- and high-magnification images of 6 µm-thick tin hinge which is protected by a very thin layer of gold.

A shielding resist layer was deposited over the entire wafer, and the carrier wafer was diced to separate out the processed dies. Release of the inductor structures (step j) was carried out on individual dies by dry or wet etching of the photoresist layers, and wet etching of the seed Ti/Cu layer. Finally, the dies were placed in a chamber and the tin hinges were reflowed to self-assemble the inductors (step k).

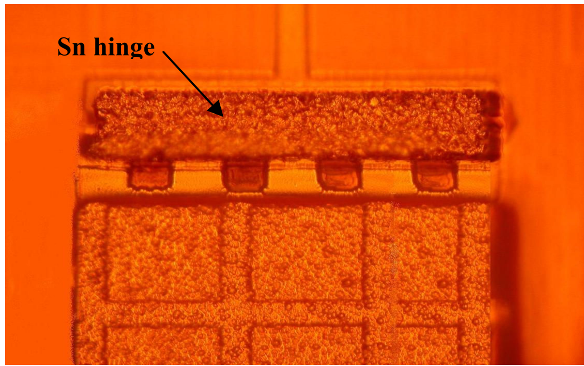


Fig. 6. Electroplated hinge for self assembled inductor.

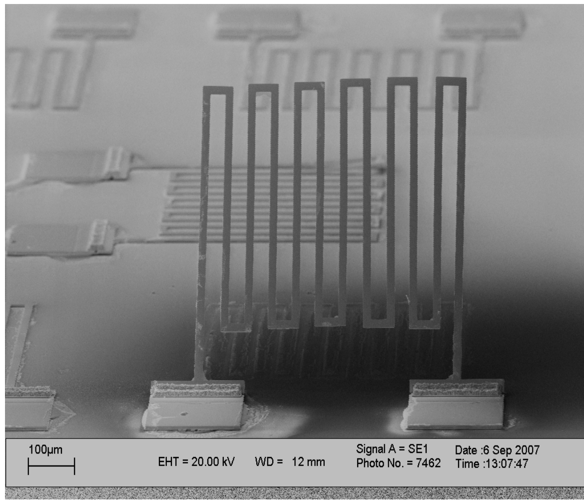


Fig. 7. Self-assembled inductor after solder reflow.

Figure 7 shows the SEM image of a self-assembled inductor, successfully released by this process. The inductor orientation is about 70° from the surface of CMOS circuit. The inductor is a meander of size 500 x 560 µm^2 with 5.5 turns and a line width of 15 µm. Some preliminary DC measurement has been performed on CMOS VCO circuit with MEMS inductors (Fig. 8). DC current consumption before and after MEMS processing is about 6 mA in both cases, indicating that the MEMS process steps do not destroy the CMOS circuits. Full electrical characterisation of inductors on RF circuits is in progress.

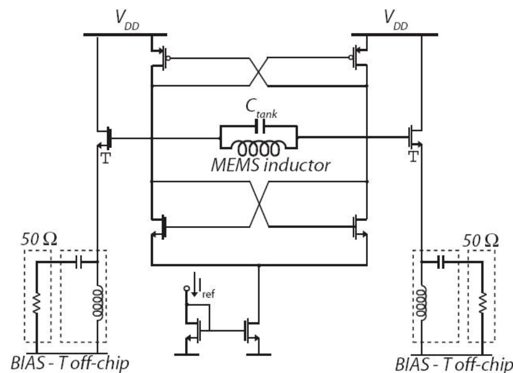


Fig. 8. VCO circuit with MEMS inductor.

IV. CONCLUSION

In this paper a new method has been introduced for die level integration of RF MEMS components with CMOS circuits. This technology has the advantage of providing monolithic integration of state-of-the-art RF MEMS components such as inductors, capacitors, and switches etc with any standard CMOS technology without any constraint of Si or compound-semiconductor platforms and also irrespective of the wafer size. This process alos offers possibilities for integration of other vertical or multi-level components or structures for RF MEMS, and for integration on multiple types of pre processed dies, including GaAs, SoI and others.

ACKNOWLEDGEMENT

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