NEMS BY MULTILAYER SIDEWALL TRANSFER LITHOGRAPHY

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ABSTRACT

This paper reports an extension of a recently demonstrated technique to fabricate nano-electro-mechanical systems (NEMS) using sidewall transfer lithography (STL). The process uses three pattern transfer steps. Each step only requires optical lithography, making the method suitable for low-cost, wafer scale fabrication. The first two involve STL and are used to form nanoscale features such as suspension beams. These may now intersect, breaking an important restriction of single-layer STL NEMS. The third involves conventional lithography and is used to form microscale features such as anchors. Current nanoscale features have a width of 100 nm and an aspect ratio of 50 : 1. The new process should allow mass parallel fabrication of complex NEMS.

INTRODUCTION

Nanoelectromechanical systems have many potential advantages over conventional MEMS, including improved sensitivity in mechanical sensors based on elastic suspensions. However, current fabrication techniques involve either an expensive direct-writing system such as electron-beam or AFM lithography to form all nanoscale features [1, 2], or a wafer-scale replication process such as soft lithography or nanoimprint lithography that itself requires nanoscale mastering [3, 4]. In each case the cost and complexity of the patterning step may prevent the translation of NEMS into practical use. Recently, a fabrication process based on sidewall transfer lithography [5-11] has been demonstrated that allows ultrathin suspensions to be combined with microscale anchors and hence form NEMS such as the electrothermal actuator in Fig. 1 [12].

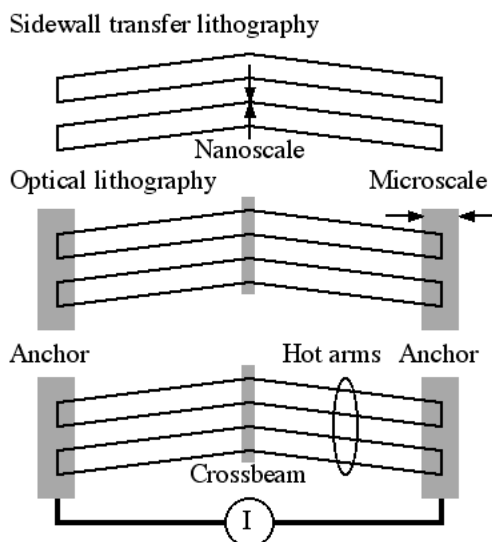

Figure 1: Single-layer STL NEMS process, for an example single-axis electrothermal stage.

Optical lithography is used to form an initial microscale pattern, which is transferred into a shallow silicon mesa. The mesa is coated with a conformal material, and etched to leave only the vertical parts of the coating (which follow the mesa perimeter, and have a width equal to the coating thickness) as a nanoscale mask. Conventional lithography is used to add any necessary micron-scale features, and the combined pattern is transferred into silicon using deep reactive ion etching (DRIE). Suspended parts are then freed to allow motion, by etching of a sacrificial oxide interlayer.

MULTILAYER STL NEMS

Sidewall transfer lithography is potentially attractive for mass production of NEMS, since it allows wafer-scale fabrication of nanoscale features using widely available equipment. However, it suffers from key topological constraints. Since the nanoscale patterns follow closed polygonal perimeters, they must have constant width, be continuous and not be self-intersecting. It is also difficult to combine nanoscale features and separations; the features currently have microscale separations. Overcoming these limitations should extend the range of possible applications. Here we demonstrate a three-layer process involving two STL steps and one additional conventional lithography step that can allow overcome one constraint, namely to allow intersecting nanoscale features, for example as required in a two-axis electro-thermal stage with intersecting suspensions (Fig. 2).

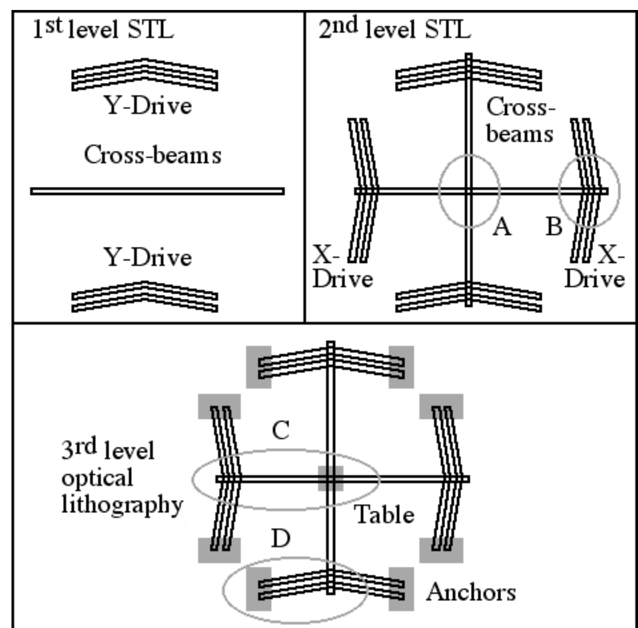

Figure 2: Multi-layer STL NEMS process, for an example two-axis electrothermal stage.

Intersecting nanoscale features can be formed using repetitions of a comparable process based on conventional lithography and reactive ion etching to form a shallow mesa, followed by common deposition of a conformal

coating whose horizontal surfaces are then removed. The remaining vertical surfaces form a sidewall mask that now follows the combined perimeter of the overlaid mesa patterns (Fig. 3). A final conventional lithography step can again be used to add microscale features such as anchors, and the whole pattern can be transferred into the silicon as before, using deep reactive ion etching.

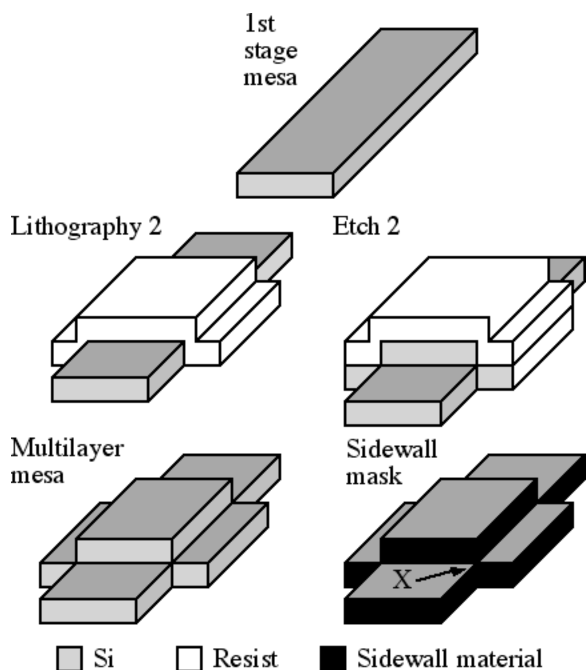

Figure 3: Detail of overlaid sidewall mask features.

The modified process still suffers from several limitations. Firstly, additional photomasks are required, since the nanoscale features must be spread over multiple layers. However, the masks contain relatively large features, and may therefore be low cost. Secondly, overlaid nanoscale features can suffer from microscale alignment errors, and it is important that these do not impact on device operation. Thirdly, overlaid features suffer a gradual degradation in separation, since a thicker resist is required to planarise mesa features formed in earlier stages. Finally, intersecting features must have shallow steps at the surface derived from the original mesa pattern. However, despite these limitations, surprisingly good results can still be obtained.

EXPERIMENTAL RESULTS

NEMS were fabricated in 100 mm diameter bare Si and bonded silicon-on-insulator (BSOI) wafers, using the process flow shown in Fig. 4. Here, for simplicity, overlaid nanoscale features are shown side by side; however, they may clearly intersect one another. The two STL steps were carried out by patterning and etching a first set of mesas (steps 1-3), and then patterning and etching a second set (steps 4, 5). A low-stress conformal metal coating was then deposited, and horizontal surfaces of this metal were removed by directional etching (steps 6, 7). The result was a surface mask defining overlaid nanoscale features. A third conventional lithography step was then carried out to add any microscale parts (step 8). The combined pattern was transferred into the silicon substrate by deep reactive ion etching (steps 9, 10). Suspended mechanical parts were freed by etching of sacrificial oxide (step 11) and metal was deposited over the entire structure to provide electrical contact (step 12).

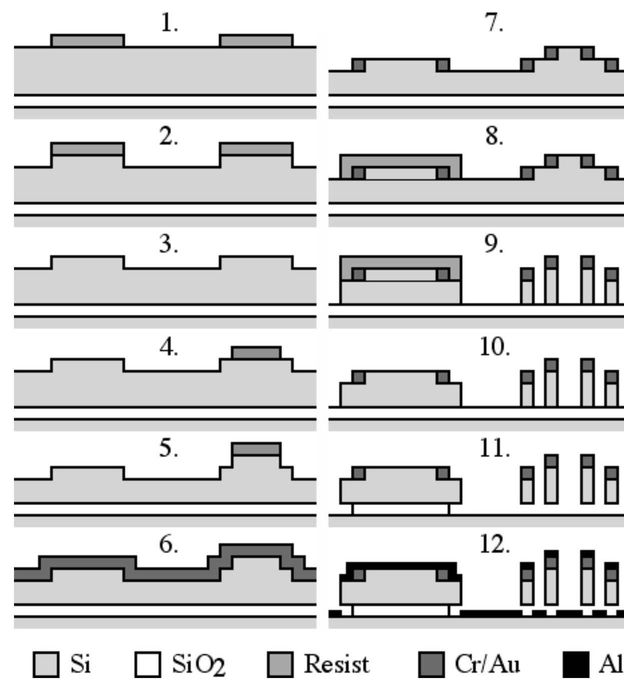

Figure 4: Multi-layer BSOI STL NEMS process.

Patterning was carried out using a Quintel Q7000 mid-UV contact mask aligner. 0.4 μm thickness of Shipley S1805 photoresist was used for patterning the first STL layer; 1.5 μm of Shipley S1813 resist was used for the second, and the same resist was used to define the anchors. Development was carried out using Microposit MF-319, followed by an O_2 plasma descum.

Mesa etching was carried out using a STS single chamber multiplex inductively coupled plasma (ICP) etcher, using a cyclic process based on SF_6 and C_4F_8. The DRIE parameters were 6.8 mTorr pressure, 350 W coil RF power, 11 W platen power and 150 V DC bias, with a 10 sec etch cycle using 50 sccm SF_6 and 5 sccm O_2 followed by a 5 sec passivation cycle using 80 sccm C_4F_8.

Sputter deposition and etching were carried out using a Nordiko RF sputter coater. A conformal layer of 10 nm Cr and 100 nm Au was first deposited, and horizontal layers of this material were then etched away by RF sputtering in Ar gas at 2 x 10^{-3} mbar pressure. The Au layer was used to form a low-stress metal sidewall mask, while the higher-stress Cr was used to ensure adhesion.

Deep silicon etching was again carried out using the ICP DRIE. However, the cycle time of the etch step was reduced to 4 sec to prevent erosion of the nanoscale beam by scalloping, while the cycle time of the passivation step was similarly reduced to maintain the width of the beam at approximately 100 nm for the full etch depth.

Fig. 5 shows scanning electron microscope photographs of structures at different stages during processing. Fig. 5a shows intersecting mesas formed by two consecutive cycles of patterning a layer of photoresist and then transferring the resulting features into the Si to a depth of 500 nm by DRIE. The terraced nature of the

compound mesa may clearly be seen. Figs. 5b and 5c show details of the mesas after deposition of Cr/Au and sputter etching. The sidewall has a stepped structure that follows the original mesa pattern. It has been eroded to roughly half the original mesa height by sputter etching, as has the edge of the Si mesa. However, continuous joints are clearly formed between the two layers of sidewall metal. Figure 5d shows high aspect ratio (HAR) nanoscale features formed after the combined pattern has been transferred into the silicon to a total depth of 5 μm by deep etching. The nanoscale features are again continuous from layer-to-layer. The remaining sidewall mask can be seen at the top of the beam. Despite this, the HAR features are not distorted by residual stress.

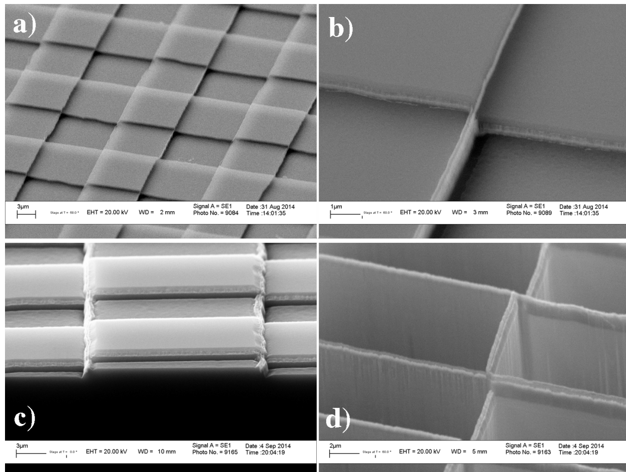

Figure 5: SEM images of a) etched multilayer mesa, b) and c) sidewall mask, d) HAR Si nanostructure.

Using this process, intersecting features such as the crossbeams at position A in the two-axis stage shown in Fig. 2 and the chevron electrothermal drive at B can easily be fabricated. Fig. 6a shows images obtained at A in a part-completed device using a SEM and a Veeco optical interferometer, while Fig. 6b shows the corresponding images obtained at B. Although the interferometer lacks sufficient resolution to visualize the nanoscale structures completely, the 3D views highlight the residual terracing at the top of the beams.

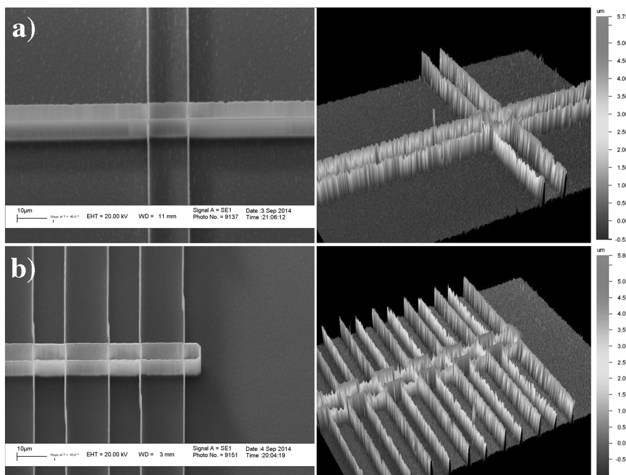

Figure 6: SEM and interferometric images of a) cross-beams (A in Fig. 2) and b) electrothermal drive (B).

We have verified that the results of multilayer sidewall processing are effectively independent of the assignment of features to the two different STL layers. For example, Fig. 7a shows the layout of a set of dies containing nested and stacked nanoscale features. In each case, two die variants are shown, with the features assigned to the two STL layers in reverse order. Figs. 7b and 7c show fabricated structures; the same result is clearly achieved in each case.

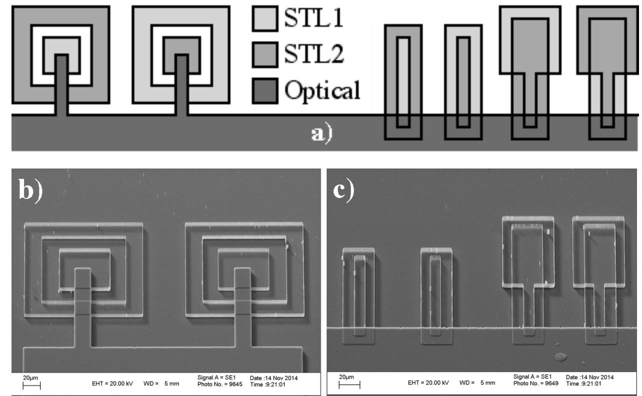

Figure 7: a) CAD layouts for nested (LH) and stacked (RH) nanoscale structures; b) and c) SEM images.

With the addition of microscale anchors, complete device structures can be realized. Fig. 8a shows details of the two-axis stage in Fig. 2 in position C, showing one chevron electrothermal actuator together with the crossbeams and central table, and Fig. 8b shows a close-up of the attachment of the actuator beams to their anchor points. The ends of the polygons defining the beam array are buried in the anchors, so these common features have no effect on the final device.

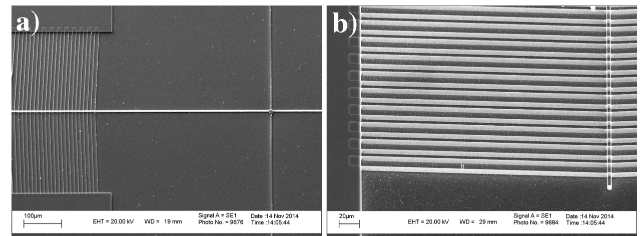

Figure 8: SEM images of a) actuator and table (region C in Fig. 2) and b) anchor (D).

We have also verified that devices may be fabricated on the same wafer using single- and double-layer STL patterning simultaneously. For example, the intersections between the crossbeams and the actuators in the x-y stage in Fig. 2 may instead be achieved using additional link-bars, as shown in Fig. 9a. Similarly, the intersections between the crossbeams and the central table may be achieved by sub-dividing the beams into non-intersecting segments that are linked by the table itself. Figs. 9b and 9c show SEM views of the resulting structures at F and G respectively. Similar static arrangements have clearly been achieved using this alternative layout; however, one disadvantage may be a reduction in dynamical performance due to the inertial mass of the additional microscale components.

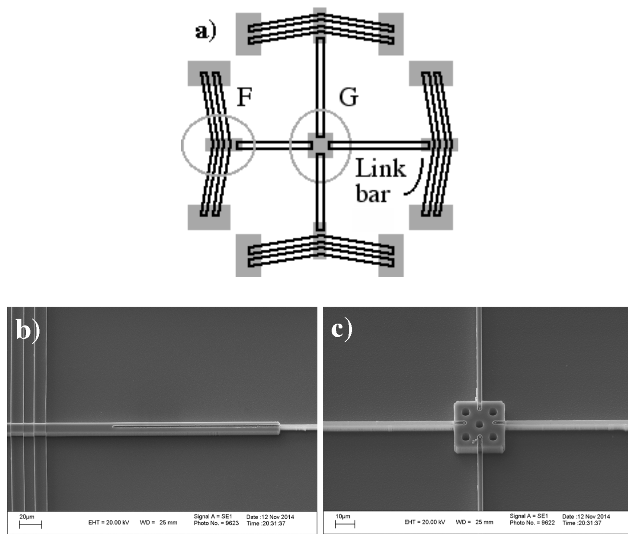

Figure 9: a) Single-layer STL NEMS X-Y stage; b) and c) SEM views at F and G.

PROCESSING ISSUES

The process suffers from several minor difficulties associated with lithography, etching and stress.

Lithography - care is needed to ensure complete planarisation of all mesas during spin coating of resist; failure to do so inevitably results in voids in the structure during DRIE. Similarly care is needed to ensure complete exposure and development of the resulting resist layers, since they must have a varying thickness.

Etching - the edge quality of first set of mesas is slightly degraded by the RIE step used to form the second set. In addition, the physical sputtering used to strip the horizontal metal surfaces does also remove some of the vertical surfaces of the sidewall mask. Generally, this is unimportant, but care is needed to avoid erosion of links between the two metal layers, for example at the point X in Fig. 3. Sputter etching can lead to re-deposition of chromium spots; however, these can be removed using a wet etch step in cerium and dilute nitric acid.

Stress - the metal sidewall mask currently remains in situ after completion of processing, and residual stress can cause some distortion of the underlying Si nanostructure. We have verified that some of these difficulties can be avoided using a SiO_2 sidewall mask, since this can be removed more easily from horizontal layers by RIE and then stripped completely by vapor-phase HF etching, for example during undercut of suspended structures.

Finally, we note that the final metal layer may be localized to the anchors by depositing and patterning the metal after step 7 in Fig. 4, before the final DRIE step.

CONCLUSIONS

A multi-layer sidewall transfer lithography process has been developed for mass parallel fabrication of NEMS. Nanoscale features are spread over multiple photomasks, and repetitive cycles of optical lithography and shallow etching are used to transfer these features into a terraced structure. The sidewalls are coated with a common layer of low stress metal whose vertical surface provides a mask for etching. The combined pattern is transferred into the silicon as a high aspect ratio nanostructure by deep reactive ion etching, together with other microscale features. Sacrificial layer processing then allows formation of movable suspended parts. Using this process, multilayer nanoscale structuring of silicon has been demonstrated with a width of 100 nm and an aspect ratio of 50 : 1.

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